Date of receipt: 09 October 2006 (09.10.2006) PCT/CN2006/002421
PCT/CN2006 / 0 0 2 4 2 1

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# An Interleaving Scheme for an LDPC Coded 16APSK System

## TECHNICAL FIELD OF THE INVENTION

**[0001]** The present invention relates to interleaving low density parity check ("LDPC") encoded bits in 16APSK modulation systems. In particular, by assigning the bits determining modulation symbols based on different bit degrees, one can efficiently find the desirable tradeoff between error performance and error floor provided by the LDPC codes in use.

## RELATED APPLICATIONS

**[0002]** This application relates to the applications titled "An Interleaving Scheme for an LDPC Coded QPSK/8PSK System" filed ####, "An Interleaving Scheme for an LDPC Coded 32APSK System" filed ####, and "A family of LDPC codes for video broadcasting applications" filed ####.

## BACKGROUND OF THE INVENTION

**[0003]** In "*Bit-Reliability Mapping in LDPC-Codes Modulation systems,*" Yan Li and William Ryan, IEEE Communications Letters, vol. 9, no. 1, January 2005, the authors studied the performance of LDPC-coded modulation systems with 8PSK. With the proposed bit reliability mapping strategy, about 0.15 dB performance improvement over a non-interleaving scheme is achieved. The authors also explain the reason for this improvement using an analysis tool called EXIT charts. In the interleaving approach, one interleaving approach is considered and has been shown to offer a better performance over non-interleaving systems, i.e., in the bit-reliability mapping scheme less reliable LDPC codes bits are mapped to the lower level modulation bits and the more reliable bits are mapped to the higher level bits.

**[0004]** Forward error control (FEC) coding is critical for communications systems to ensure reliable transmission of data across noisy communication channels. Based on Shannon's theory, these communication channels exhibit fixed capacity that can be expressed in terms of bits per symbol at certain signal to noise ratio (SNR), which is defined as the Shannon limit. One of the most important research areas in communication and coding theory is to devise coding schemes offering performance approaching the Shannon limit with reasonable complexity. It has



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been shown that LDPC codes with belief propagation (BP) decoding provide performance close to the Shannon limit with tractable encoding and decoding complexity.

[0005] LDPC codes were first described by Gallager in the 1960s. LDPC codes perform remarkably close to the Shannon limit. A binary ($N$, $K$) LDPC code, with a code length $N$ and dimension $K$, is defined by a parity check matrix H of ($N$-$K$) rows and $N$ columns. Most entries of the matrix H are zeros and only a small number the entries are ones, hence the matrix H is sparse. Each row of the matrix H represents a check sum, and each column represents a variable, e.g., a bit or symbol. The LDPC codes described by Gallager are regular, i.e., the parity check matrix H has constant-weight rows and columns.

[0006] Regular LDPC codes can be extended to irregular LDPC codes, in which the weight of rows and columns vary. An irregular LDPC code is specified by degree distribution polynomials $v(x)$ and $c(x)$, which define the variable and check node degree distributions, respectively. More specifically, let

$$v(x) = \sum_{j=1}^{d_{v\max}} v_j x^{j-1},$$

and

$$c(x) = \sum_{j=1}^{d_{c\max}} c_j x^{j-1},$$

where the variables $d_{v\max}$ and $d_{c\max}$ are a maximum variable node degree and a check node degree, respectively, and $v_j(c_j)$ represents the fraction of edges emanating from variable (check) nodes of degree $j$.

[0007] While irregular LDPC codes can be more complicated to represent and/or implement, it has been shown, both theoretically and empirically, that irregular LDPC codes with properly selected degree distributions outperform regular LDPC codes. FIG. 1 illustrates a parity check matrix representation of an exemplary irregular LDPC code of codeword length six.

[0008] LDPC codes can also be represented by bipartite graphs, or Tanner graphs. In Tanner graph, one set of nodes called variable nodes (or bit nodes) corresponds to the bits of the codeword and the other set of nodes called constraints nodes ( or check nodes) corresponds the

set of parity check constrains which define the LDPC code. Bit nodes and check nodes are connected by edges. A bit node and a check node is said to be neighbors or adjacent if they are connected by an edge. Generally, it is assumed that a pair of nodes is connected by at most one edge.

**[0009]** FIG. 2 illustrates a bipartite graph representation of the irregular LDPC code illustrated in FIG. 1. The LDPC code represented by FIG. 1 is of codeword length 6 and has 4 parity checks. As shown in FIG. 1, there are a total of 9 one's in the parity check matrix representation of the LDPC code. Therefore in the Tanner graph representation shown in FIG. 2, 6 bit nodes 201 are connected to 4 check nodes 202 by 9 edges 203.

**[0010]** LDPC codes can be decoded in various ways, such as majority-logic decoding and iterative decoding. Due to the structures of their parity check matrices, LDPC codes are majority-logic decodable. Majority-logic decoding requires the least complexity and achieves reasonably good error performance for decoding, such as for LDPC codes with relatively high column weights in their parity check matrices (e.g., Euclidean geometry LDPC and projective geometry LDPC codes), whereas iterative decoding methods have received more attentions due to their better performance versus complexity tradeoffs. Unlike majority-logic decoding, iterative decoding processes the received symbols recursively to improve the reliability of each symbol based on constraints that specify the code. In the first iteration, the iterative decoder uses the channel output as input, and generates reliability output for each symbol. Subsequently, the output reliability measures of the decoded symbols at the end of each decoding iteration are used as inputs for the next iteration. The decoding process continues until a certain stopping condition is satisfied. Then final decisions are made, based on the output reliability measures of the decoded symbols from the last iteration. According to the different properties of reliability measures used at each iteration, iterative decoding algorithms can be further divided into hard decision, soft decision and hybrid decision algorithms. The corresponding popular algorithms are iterative bit-flipping (BF), belief propagation (BP), and weighted bit-flipping (WBF) decoding, respectively. The BP algorithm has been proven to provide maximum likelihood decoding given the underlying Tanner graph is acyclic. Therefore, it realistically becomes the most popular decoding method. The invention described below, however, only discusses BP decoding of LDPC codes.

[0011] BP for LDPC codes is a kind of message passing decoding. Messages transmitted along the edges of the graph are log-likelihood ratio (LLR) $\log\frac{p_0}{p_1}$ associated with variable nodes corresponding to codeword bits. In this expression $p_0$ and $p_1$ denote the probability that the associated bit takes value 0 and 1, respectively. BP decoding has two steps, horizontal step and vertical step. In the horizontal step, each check node $c_m$ sends to each adjacent bit $b_n$ a check-to-bit message which is calculated based on all bit-to-check messages incoming to the check $c_m$ except the one from bit $b_n$. In the vertical step, each bit node $b_n$ sends to each adjacent check node $c_m$ a bit-to-check message which is calculated based on all check-to-bit messages incoming to the bit $b_n$ except the one from check node $c_m$. These two steps are repeated until a valid codeword is found or the maximum number of iterations is reached.

[0012] Because of its remarkable performance with BP decoding, irregular LDPC codes are among the best for many applications. Various irregular LDPC codes have been accepted or being considered for various communication and storage standards, such as DVB-S2/DAB, wireline ADSL, IEEE 802.11n, and IEEE 802.16 [4][5]. While considering applying irregular LDPC codes to video broadcasting systems, one often encounter a trouble called error floor.

[0013] The error floor performance region of an LDPC decoder can be described by the error performance curve of the system. The LDPC decoder system typically exhibits sharp decrease in error probability as the quality of the input signal improves. The resulting error performance curves are conventionally called waterfall curve and the corresponding region is called waterfall region. At some point, however, the decrease of error probability with input signal quality increase decreases. The resulting flat error performance curve is called error floor. FIG. 3 illustrates an exemplary FER performance curve containing waterfall region 301 and error floor region 302 of an irregular LDPC code.

SUMMARY OF THE INVENTION

[0014] The present invention discloses an interleaving approach in which for LDPC codes bits with any level of reliability, a portion of lower level modulation bits and a portion of higher level modulation bits are mapped. Given a specific structure of an LDPC code and the

modulation method, the optimal portion of lower and higher level modulation bits can be determined through a theoretical algorithm called density evolution.

[0015] In one embodiment of the invention, there is a digital communications system to interleave bits in a 16ASPK modulation system with FEC code, comprising a transmitter to generate signal waveforms across a communication channel to a receiver, the transmitter having a message source to generate a set of discrete bits which has a corresponding signal waveform; and an LDPC encoder to generate signals from alphabet to a signal mapper, wherein interleaving is a non-consecutive mapping that generates the best threshold of corresponding LDPC codes predicted by density evolution.

[0016] Using carefully selected check and bit node degree distributions and Tanner graph constructions, the LDPC codes in the present invention have good threshold which reduce transmission power for a given FER performance.

[0017] The threshold of an LDPC code is defined as the smallest SNR value at which as the codeword length tends to infinity, the bit error probability can be made arbitrarily small.

[0018] Different applications have different requirements for the thresholds and error floor of LDPC codes. Therefore it is desired to develop a method to determine the mapping scheme in 16APSK systems to provide required threshold while keeping error floor lower than specific criteria.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the corresponding drawings and in which like reference numerals refer to similar elements and in which:

[0020] FIG. 1 is a parity check matrix representation of an exemplary irregular LDPC code of codeword length six.

[0021] FIG. 2 illustrates a bipartite graph representation of the irregular LDPC code illustrated in FIG. 1.

[0022] FIG. 3 illustrates an exemplary FER performance curve including waterfall and error floor region of an irregular LDPC code.

[0023] FIG. 4 is an exemplary communications system which employs LDPC codes and interleavor/deinterleavor, according to an embodiment of the present invention.

[0024] FIG. 5 illustrates an exemplary transmitter in FIG. 4.

[0025] FIG. 6 illustrates an exemplary receiver in FIG. 4.

[0026] FIG. 7 illustrates the bit mapping block in 16APSK modulation.

[0027] FIG. 8 illustrates the bit mapping for 16APSK symbol.

DETAILED DESCRIPTION OF THE INVENTION

[0028] Referring to the accompanying drawings, a detailed description will be given of encoded bit mapping methods using LDPC codes and program for executing this method according to embodiments of the invention.

[0029] Although the present invention is described with respect to LDPC codes, it is recognized that the bit labeling approach can be utilized with other codes. Further, this approach can be implemented with uncoded systems.

[0030] FIG. 4 is a diagram of a communications system employing LDPC codes with an interleaver, according to an embodiment of the present invention. A communications system includes a transmitter 401 which generates signal waveforms across a communication channel 402 to a receiver 403. The transmitter 401 includes a message source producing a discrete set of possible messages. Each of these messages corresponds a signal waveform. The waveforms enter the channel 402 and are corrupted by noise. LDPC codes are employed to reduce the disturbances introduced by the channel 402. Given an LDPC code and the desired error floor level, an interleaver and a deinterleaver are used in the transmitter 401 and the receiver 403, respectively, based on an interleaving rule to produce a good threshold.

[0031] FIG. 5 depicts an exemplary transmitter in the communications system of FIG. 4 which employs LDPC codes and interleaver. The LDPC encoder 502 encodes information bits from source 501 into LDPC codewords. The mapping from each information block to each LDPC codeword is specified by the parity check matrix (or equivalently the generator matrix) of the LDPC code. The LDPC codeword is interleaved and modulated to signal waveforms by the interleaver/modulator 503. These signal waveforms are sent to a transmit antenna 504 and propagated to a receiver shown in FIG. 6.

[0032] FIG. 6 depicts an exemplary receiver in FIG. 4 which employs LDPC codes and a deinterleaver. Signal waveforms are received by the receiving antenna 601 and distributed to demodulator/deinterleavor 602. Signal waveforms are demodulated by demodulator and deinterleaved by deinterleavor and then distributed to a LDPC decoder 603 which iteratively decodes the received messages and output estimations of the transmitted codeword. The deinterleaving rule employed by the demodulator/deinterleaver 602 should match with the interleaving rule employed by the interleaver/modulator 503. That is to say, the deinterleaving scheme should follow an anti-rule of the interleaving scheme.

[0033] Given an LDPC code and 16APSK modulation scheme, we define the optimal interleaving as the non-consecutive mapping arrangement which generate the best threshold of the corresponding LDPC code predicted by density evolution.

[0034] As shown in FIG. 7, the 16APSK bit-to-symbol mapping circuit takes four bits ($b_{4i}$, $b_{4i+1}$, $b_{4i+2}$, $b_{4i+3}$) each time and maps them into an $I$ value and a $Q$ value, with $i$=0, 1, 2, .... The mapping logic is shown in FIG. 8.

[0035] In 16APSK, let $(\tilde{b}_i \ \tilde{b}_{i+1} \ \tilde{b}_{i+2} \ \tilde{b}_{i+3})$ be the 4 bits determining the i-th symbol, for $i \in \{i \mid 0 \le i \le N_{ldpc_bits} - 1, \text{and } i \bmod 4 = 0\}$. We specify a $N_{offset}$ to define the number of bit mapping for each code rate. Given an LDPC code and the requirement of level of error floor, there is an optimal interleaving scheme obtained through density evolution analysis. For the LDPC codes with rate 2/3, ¾, 4/5, 5/6, 13/15, and 9/10 the interleaving rule for 16APSK is:

$$\begin{cases} \tilde{b}_i = b_{\left(8\times\left\lfloor\frac{i}{1024}\right\rfloor + N_{offset} + \frac{i}{4}\bmod 8\right)\times 32 + \left\lfloor\frac{i}{32}\right\rfloor \bmod 32} \\ \tilde{b}_{i+1} = b_{\left(8\times\left\lfloor\frac{i}{1024}\right\rfloor + N_{offset} + \frac{i}{4}\bmod 8 + 120\right)\times 32 + \left\lfloor\frac{i}{32}\right\rfloor \bmod 32} \\ \tilde{b}_{i+2} = b_{\left(8\times\left\lfloor\frac{i}{1024}\right\rfloor + N_{offset} + \frac{i}{4}\bmod 8 + 240\right)\times 32 + \left\lfloor\frac{i}{32}\right\rfloor \bmod 32} \\ \tilde{b}_{i+3} = b_{\left(\frac{i}{4} + 32\times N_{offset} + 11520\right)\bmod N_{ldpc_bits} - \left(\frac{i}{4}\right)\bmod 256 + \left(\frac{i}{4}\bmod 8\right)\times 32 + \left\lfloor\frac{i}{32}\right\rfloor \bmod 32} \end{cases} \quad (3)$$

for $i \in \{i \mid 0 \le i \le N_{ldpc_bits} - 1, \text{and } i \bmod 4 = 0\}$.

**[0036]** The numbers of bit offset is summarized in Table 1: Offset values for interleaving in 16APSK.

| Rate | $N_{offset}$ |
|---|---|
| 2/3 | 80 |
| 3/4 | 88 |
| 4/5 | 96 |
| 5/6 | 104 |
| 13/15 | 112 |
| 9/10 | 120 |

**Table 1: Offset values for interleaving in 16APSK.**

**[0037]** Although the invention has been described by the way of examples of preferred embodiments, it is to be understood that various other adaptations and modifications may be made within the spirit and scope of the invention. Therefore, it is the object of the appended claims to cover all such variations and modifications as come within the true spirit and scope of the invention.

We claim:

1. A digital communications transmitter interleaving LDPC encoded bits in a 16APSK modulation system based on a rule:

$$\begin{cases} \tilde{b}_i = b_{\left(8\times\left\lfloor\frac{i}{1024}\right\rfloor+N_{offset}+\frac{i}{4}\bmod 8\right)\times 32+\left\lfloor\frac{i}{32}\right\rfloor\bmod 32} \\ \tilde{b}_{i+1} = b_{\left(8\times\left\lfloor\frac{i}{1024}\right\rfloor+N_{offset}+\frac{i}{4}\bmod 8+120\right)\times 32+\left\lfloor\frac{i}{32}\right\rfloor\bmod 32} \\ \tilde{b}_{i+2} = b_{\left(8\times\left\lfloor\frac{i}{1024}\right\rfloor+N_{offset}+\frac{i}{4}\bmod 8+240\right)\times 32+\left\lfloor\frac{i}{32}\right\rfloor\bmod 32} \\ \tilde{b}_{i+3} = b_{\left(\frac{i}{4}+32\times N_{offset}+11520\right)\bmod N_{ldpc_bits}-\left(\frac{i}{4}\right)\bmod 256+\left(\frac{i}{4}\bmod 8\right)\times 32+\left\lfloor\frac{i}{32}\right\rfloor\bmod 32} \end{cases}$$

for $i \in \{i \mid 0 \le i \le N_{ldpc_bits}-1, \text{and } i \bmod 4 = 0\}$, where $\lfloor x \rfloor$ is the floor function which returns the largest integer that is less than or equal to x, $N_{ldpc_bits} = 15360$ is the codeword length of the LDPC code in use, and $N_{Offset}$ is the offset values for different code rates which are defined as:

| Rate | $N_{offset}$ |
|---|---|
| 2/3 | 80 |
| 3/4 | 88 |
| 4/5 | 96 |
| 5/6 | 104 |
| 13/15 | 112 |
| 9/10 | 120 |

2. A digital communications receiver employing an LDPC decoder for decoding interleaved LDPC encoded bits in a 16APSK modulation system based on a rule:

$$\begin{cases} \tilde{b}_i = b_{\left(8\times\left\lfloor\frac{i}{1024}\right\rfloor+N_{offset}+\frac{i}{4}\bmod 8\right)\times 32+\left\lfloor\frac{i}{32}\right\rfloor\bmod 32} \\ \tilde{b}_{i+1} = b_{\left(8\times\left\lfloor\frac{i}{1024}\right\rfloor+N_{offset}+\frac{i}{4}\bmod 8+120\right)\times 32+\left\lfloor\frac{i}{32}\right\rfloor\bmod 32} \\ \tilde{b}_{i+2} = b_{\left(8\times\left\lfloor\frac{i}{1024}\right\rfloor+N_{offset}+\frac{i}{4}\bmod 8+240\right)\times 32+\left\lfloor\frac{i}{32}\right\rfloor\bmod 32} \\ \tilde{b}_{i+3} = b_{\left(\frac{i}{4}+32\times N_{offset}+11520\right)\bmod N_{ldpc_bits}-\left(\frac{i}{4}\right)\bmod 256+\left(\frac{i}{4}\bmod 8\right)\times 32+\left\lfloor\frac{i}{32}\right\rfloor\bmod 32} \end{cases}$$

for $i \in \{i \mid 0 \le i \le N_{ldpc_bits}-1, \text{and } i \bmod 4 = 0\}$, where $\lfloor x \rfloor$ is the floor function which returns the largest integer that is less than or equal to x, $N_{ldpc_bits} = 15360$ is the codeword length of the LDPC code in use, and $N_{Offset}$ is the offset values for different code rates which are defined as:

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| 4/5 | 96 |
| 5/6 | 104 |
| 13/15 | 112 |
| 9/10 | 120 |

3. A computer readable medium storing a computer program for performing a method specifying an interleaving scheme of LDPC encoded bits in a 16APSK modulation system base on a rule:

$$\begin{cases} \tilde{b}_i = b_{\left(8\times\left\lfloor\frac{i}{1024}\right\rfloor + N_{offset} + \frac{i}{4}\bmod 8\right)\times 32 + \left\lfloor\frac{i}{32}\right\rfloor \bmod 32} \\ \tilde{b}_{i+1} = b_{\left(8\times\left\lfloor\frac{i}{1024}\right\rfloor + N_{offset} + \frac{i}{4}\bmod 8 + 120\right)\times 32 + \left\lfloor\frac{i}{32}\right\rfloor \bmod 32} \\ \tilde{b}_{i+2} = b_{\left(8\times\left\lfloor\frac{i}{1024}\right\rfloor + N_{offset} + \frac{i}{4}\bmod 8 + 240\right)\times 32 + \left\lfloor\frac{i}{32}\right\rfloor \bmod 32} \\ \tilde{b}_{i+3} = b_{\left(\frac{i}{4} + 32\times N_{offset} + 11520\right)\bmod N_{ldpc_bits} - \left(\frac{i}{4}\right)\bmod 256 + \left(\frac{i}{4}\bmod 8\right)\times 32 + \left\lfloor\frac{i}{32}\right\rfloor \bmod 32} \end{cases}$$

for $i \in \{i \mid 0 \le i \le N_{ldpc_bits} - 1, \text{and } i \bmod 4 = 0\}$ where $\lfloor x \rfloor$ is the floor function which returns the largest integer that is less than or equal to x, $N_{ldpc_bits} = 15360$ is the codeword length of the LDPC code in use, and $N_{Offset}$ is the offset values for different code rates which are defined as:

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