CLAIMS

1. A method, comprising:

etching an inter-row trench in a substrate;

substantially or entirely filling the inter-row trench with a dielectric material; and

forming a fin and a insulating projection at least in part by etching a gate trench in the substrate, wherein the insulating projection includes at least some of the dielectric material in the inter-row trench;

filling the gate trench with a gate material; and

recessing the gate material below a top surface of the fin.

2. The method of claim 1, wherein etching the inter-row trench comprises:

forming precursor trenches in a sacrificial region on the substrate; and

forming a spacer in the precursor trenches, wherein the spacer narrows the precursor trenches.

3. The method of claim 2, comprising etching the inter-row trenches using the sacrificial region and sidewall spacers as a mask.

4. The method of claim 1, wherein etching an inter-row trench in a substrate comprises etching an inter-row trench through an upper-doped region and at least partially into a lower-doped region.

5. The method of claim 1, wherein substantially or entirely filling the inter-row trench with a dielectric material comprises:

forming a first liner in the inter-row trench; and

applying a spun-on-dielectric to the substrate.

6. The method of claim of claim 1, comprising:

masking the etch of the inter-row trench with a sacrificial material and a first sidewall spacer; and

removing the sacrificial material after substantially or entirely filling the inter-row trench with the dielectric material.

7. The method of claim 6, comprising:

forming a second sidewall spacer on a surface of the first sidewall spacer following removal of the sacrificial material; and

masking the etch of the gate trench at least in part with the second sidewall spacer.

8. The method of claim 1, wherein forming a fin and a insulating projection at least in part by etching a gate trench in the substrate comprises etching a portion of the dielectric material.

9. The method of claim 1, wherein forming a fin and a insulating projection at least in part by etching a gate trench in the substrate comprises forming a plurality of fin rows and a plurality of insulating projections generally simultaneously by etching a plurality of gate trenches.

10. The method of claim 9, wherein:

each insulating projection among the plurality of insulating projections is interposed between a pair of fin rows among the plurality of fin rows, and

a gate trench among the plurality of gate trenches is disposed on either side of each fin row among the plurality of fin rows between the fin row and an adjacent insulating projection among the plurality of insulating projections.

11. The method of claim 1, wherein:

etching an inter row-trench in the substrate comprises forming a first mask on the substrate with a photolithography step, and

forming a fin and a insulating projection at least in part by etching a gate trench in the substrate comprises forming a second mask on the substrate with a second photolithography step.

12. The method of claim 11, wherein the second mask is shifted with respect to the first mask by a distance generally equal to half of a pitch of the first mask.

13. The method of claim 12, wherein:

forming the first mask comprises forming the first mask with a first photolithographic tool;

forming the second mask comprises forming the second mask with a second photolithographic tool, wherein a resolution of the second photolithographic tool is generally as large as or larger than twice a resolution of the first photolithographic tool.

14. The method of claim 1, wherein filling the gate trench with a gate material comprises completely filling the gate trench with the material.

15. The method of claim 1, wherein the gate material is recessed less than or equal to 1000 angstroms below the top surface of the fin.

16. The method of claim 1, wherein the gate material partially overlaps the upper-doped region.

17. A device, comprising:

a semiconductor fin;

a gate trench disposed on either side of the semiconductor fin; and

a insulating projection disposed on either side of the semiconductor fin and separated at least in part from the semiconductor fin by one of the gate trenches.

18. The device of claim 17, comprising:

a gate disposed in each gate trench, wherein each gate is recessed below a top of the semiconductor fin.

19. The device of claim 17, wherein the semiconductor fin comprises two legs separated by a generally U-shaped void.

20. A method, comprising:

forming a first plurality of trenches in a substrate that are generally parallel to one another;

forming a second plurality of trenches in the substrate that are generally parallel to one another and generally perpendicular to the first plurality of trenches; and

forming a third plurality of trenches in the substrate that are generally parallel to the second plurality of trenches and misaligned with respect to the second plurality of trenches by a distance that is less than a period of the second plurality.

21. The method of claim 20, comprising at least substantially filling both the first plurality of trenches and the second plurality of trenches with a dielectric material before forming the third plurality of trenches.

22. The method of claim 20, wherein forming the third plurality of trenches comprises generally simultaneously forming a plurality of gate trenches, a plurality of insulating projections, and a plurality of fin rows.

23. The method of claim 20, comprising:

forming a conductive region disposed at least in part in the plurality of gate trenches; and

recessing the conductive region into the plurality of gate trenches.

CLAIMS

1. A method, comprising:

etching an inter-row trench in a substrate;

substantially or entirely filling the inter-row trench with a dielectric material;

forming a fin and an insulating projection at least in part by etching a gate trench in the substrate, wherein the insulating projection includes at least some of the dielectric material in the inter-row trench;

filling the gate trench with a gate material; and

recessing the gate material below a top surface of the fin.

2. The method of claim 1, wherein etching the inter-row trench comprises:

forming precursor trenches in a sacrificial region on the substrate; and

forming a spacer in the precursor trenches, wherein the spacer narrows the precursor trenches.

3. The method of claim 2, wherein the spacer narrows the trenches to a width that is less than a photolithographic-resolution limit.

4. The method of claim 2, comprising etching the inter-row trenches using the sacrificial region and sidewall spacers as a mask.

5. The method of claim 1, wherein etching an inter-row trench in a substrate comprises etching an inter-row trench through an upper-doped region and at least partially into a lower-doped region.

6. The method of claim 1, wherein substantially or entirely filling the inter-row trench with a dielectric material comprises:

forming a first liner in the inter-row trench; and

applying a spun-on-dielectric to the substrate.

7. The method of claim of claim 1, comprising:

masking the etch of the inter-row trench with a sacrificial material and a first sidewall spacer; and

removing the sacrificial material after substantially or entirely filling the inter-row trench with the dielectric material.

8. The method of claim 7, comprising:

forming a second sidewall spacer on a surface of the first sidewall spacer following removal of the sacrificial material; and

masking the etch of the gate trench at least in part with the second sidewall spacer.

9. The method of claim 1, wherein forming a fin and an insulating projection at least in part by etching a gate trench in the substrate comprises etching a portion of the dielectric material.

10. The method of claim 1, wherein forming a fin and an insulating projection at least in part by etching a gate trench in the substrate comprises forming a plurality of fin rows and a plurality of insulating projections generally simultaneously by etching a plurality of gate trenches.

11. The method of claim 10, wherein:

each insulating projection among the plurality of insulating projections is interposed between a pair of fin rows among the plurality of fin rows, and

a gate trench among the plurality of gate trenches is disposed on either side of each fin row among the plurality of fin rows between the fin row and an adjacent insulating projection among the plurality of insulating projections.

12. The method of claim 1, wherein:

etching an inter row-trench in the substrate comprises forming a first mask on the substrate with a photolithography step, and

forming a fin and an insulating projection at least in part by etching a gate trench in the substrate comprises forming a second mask on the substrate with a second photolithography step.

13. The method of claim 12, wherein the second mask is shifted with respect to the first mask by a distance generally equal to half of a pitch of the first mask.

14. The method of claim 13, wherein:

forming the first mask comprises forming the first mask with a first photolithographic tool;

forming the second mask comprises forming the second mask with a second photolithographic tool, wherein a resolution of the second photolithographic tool is generally as large as or larger than twice a resolution of the first photolithographic tool.

15. The method of claim 13, wherein forming the second mask comprising double-pitching a precursor mask.

16. A method, comprising:

forming a first plurality of trenches in a substrate that are generally parallel to one another;

forming a second plurality of trenches in the substrate that are generally parallel to one another and generally perpendicular to the first plurality of trenches; and

forming a third plurality of trenches in the substrate that are generally parallel to the second plurality of trenches and misaligned with respect to the second plurality of trenches by a distance that is less than a period of the second plurality.

17. The method of claim 16, comprising at least substantially filling both the first plurality of trenches and the second plurality of trenches with a dielectric material before forming the third plurality of trenches.

18. The method of claim 16, wherein forming the third plurality of trenches comprises generally simultaneously forming a plurality of gate trenches, a plurality of insulating projections, and a plurality of fin rows.

19. The method of claim 18, comprising:

forming a conductive region disposed at least in part in the plurality of gate trenches; and

recessing the conductive region into the plurality of gate trenches.

20. The method of claim 1, wherein filling the gate trench with a gate material comprises completely filling the gate trench with the material.

21. The method of claim 1, wherein the gate material is recessed less than or equal to 1000 angstroms below the top surface of the fin.

22. The method of claim 1, wherein the gate material partially overlaps the upper-doped region.