

CLAIMS

What is claimed is:

1. A neurosynaptic processing core with spike time dependent plasticity (STDP) learning for a spiking neural network, the neurosynaptic processing core comprising:
 - a spiking neuron block comprising a pre-synaptic block and a post-synaptic block, the pre-synaptic block comprising a plurality of pre-synaptic elements and the post-synaptic block comprising a plurality of post-synaptic elements;
 - a synapse block communicatively coupled to the spiking neuron block, the synapse block comprising a plurality of synaptic weight parameters, each synaptic weight parameter corresponding to a neuron pair comprising a pre-synaptic element of the plurality of pre-synaptic elements and a post-synaptic element of the plurality of post-synaptic elements;
 - a STDP learning block communicatively coupled to the spiking neuron block and the synapse block, the STDP learning block comprising:
 - a pre-synaptic event accumulator comprising:
 - a pre-synaptic spike event memory block comprising a plurality of pre-synaptic spike parameters corresponding to the plurality of pre-synaptic elements, respectively, each pre-synaptic spike parameter indicating a measure of one or more pre-synaptic spike events at the corresponding pre-synaptic element; and
 - a pre-synaptic spike parameter modifier configured to modify a pre-synaptic spike parameter of the plurality of pre-synaptic spike parameters based on a first pre-synaptic spike event input from the pre-synaptic block indicating a pre-synaptic spike event at the corresponding pre-synaptic element;
 - a post-synaptic event accumulator comprising:
 - a post-synaptic spike event memory block comprising a plurality of post-synaptic spike parameters corresponding to the plurality of post-synaptic elements, respectively, each post-synaptic spike parameter indicating a measure of one or more post-synaptic spike events at the corresponding post-synaptic element; and
 - a post-synaptic spike parameter modifier configured to modify a post-synaptic spike parameter of the plurality of post-synaptic spike parameters based on a first

post-synaptic spike event input from the post-synaptic block indicating a post-synaptic spike event at the corresponding post-synaptic element; and
a weight change accumulator comprising:

a weight change memory block comprising a plurality of weight change parameters corresponding to the plurality of synaptic weight parameters, respectively;
and

a weight change parameter modifier configured to modify a weight change parameter of the plurality of weight change parameters based a pre- synaptic spike parameter of the plurality of pre-synaptic spike parameters corresponding to the weight change parameter or a post-synaptic spike parameter of the plurality of post-synaptic spike parameters corresponding to the weight change parameter;

a learning error modulator configured to determine a plurality of learning errors associated with the STDP learning block for the plurality of synaptic weight parameters, respectively; and

a synaptic weight modifier communicatively coupled to the STDP learning block, the learning error modulator and the synapse block, the synaptic weight modifier being configured to modify a synaptic weight parameter of the plurality of synaptic weight parameters based on a weight change parameter of the plurality of weight change parameters corresponding to the synaptic weight parameter and a learning error of the plurality of learning errors corresponding to the synaptic weight parameter;

wherein the neurosynaptic processing core is formed by a plurality of processors.

2. The neurosynaptic processing core according to claim 1, wherein the synapse block comprises a plurality of synapse elements, each synapse element comprising a synaptic weight parameter of the plurality of synaptic weight parameters corresponding thereto and corresponds to the neuron pair corresponding to the synaptic weight parameter.

3. The neurosynaptic processing core according to claim 2, wherein the plurality of synapse elements are configured as a crossbar memory array, each synapse element being arranged at a corresponding cross-point of crossbar memory array.

4. The neurosynaptic processing core according to claim 1, wherein
 - the pre-synaptic spike parameter modifier comprises a pre-synaptic spike parameter incrementor configured to increment the pre-synaptic spike parameter based on the first pre-synaptic spike event input received from the pre-synaptic block, and
 - the post-synaptic spike parameter modifier comprises a post-synaptic spike parameter incrementor configured to increment the post-synaptic spike parameter based on the first post-synaptic spike event input received from the post-synaptic block.
5. The neurosynaptic processing core according to claim 4, wherein
 - the pre-synaptic spike parameter modifier further comprises a pre-synaptic spike parameter decrementor configured to decrement the pre-synaptic spike parameter, and
 - the post-synaptic spike parameter modifier further comprises a post-synaptic spike parameter decrementor configured to decrement the post-synaptic spike parameter.
6. The neurosynaptic processing core according to claim 5, wherein
 - said each pre-synaptic spike parameter indicates a pre-synaptic trace of the one or more pre-synaptic spike events at the corresponding pre-synaptic element, the pre-synaptic spike parameter incrementor is configured to increment the pre-synaptic spike parameter based on a first incremental value,
 - the pre-synaptic spike parameter decrementor is configured to decrement the pre-synaptic spike parameter based on a first decremental value,
 - said each post-synaptic spike parameter indicates a post-synaptic trace of the one or more post-synaptic spike events at the corresponding post-synaptic element, the post-synaptic spike parameter incrementor is configured to increment the post-synaptic spike parameter based on a second incremental value, and
 - the post-synaptic spike parameter decrementor is configured to decrement the post-synaptic spike parameter based on a second decremental value.
7. The neurosynaptic processing core according to claim 4, wherein the weight change accumulator further comprises a synaptic spike event selector configured to select the pre-synaptic spike parameter from the pre-synaptic spike event memory block for output to the

weight change parameter modifier based on a second post-synaptic spike event input from the post-synaptic block indicating the post-synaptic spike event at the corresponding post-synaptic element or select the post-synaptic spike parameter from the post-synaptic spike event memory block for output to the weight change parameter modifier based on a second pre-synaptic spike event input from the pre-synaptic block indicating the pre-synaptic spike event at the corresponding post-synaptic element.

8. The neurosynaptic processing core according to claim 7, wherein the weight change parameter modifier is configured to increment the weight change parameter based on the pre-synaptic spike parameter received from the synaptic spike event selector or decrement the weight change parameter based on the post-synaptic spike parameter received from the synaptic spike event selector.

9. The neurosynaptic processing core according to claim 1, wherein

the learning error modulator comprises:

a learning error determiner configured to determine the plurality of learning errors for the plurality of synaptic weight parameters, respectively; and

a learning error evaluator configured to determine a learning error outcome for the synaptic weight parameter based on a learning error of the plurality of learning errors corresponding to the synaptic weight parameter, and

the synaptic weight modifier is configured to modify the synaptic weight parameter of the plurality of synaptic weight parameters based on the weight change parameter received from the weight change accumulator corresponding to the synaptic weight parameter and the learning error outcome received from the learning error modulator corresponding to the synaptic weight parameter.

10. The neurosynaptic processing core according to claim 9, wherein

the learning error modulator further comprises a synaptic spike event record block comprising a plurality of post-synaptic spike event record parameters for the plurality of post-synaptic elements, respectively, each post-synaptic spike event record parameter indicating a

number of post-synaptic spike events that occurred at the corresponding post-synaptic element, and

the learning error determiner is configured to determine, for each of the plurality of synaptic weight parameters, the learning error for the synaptic weight parameter based on the post-synaptic spike event record parameter for the post-synaptic element corresponding to the synaptic weight parameter and a reference parameter for the post-synaptic element corresponding to the synaptic weight parameter.

11. The neurosynaptic processing core according to claim 1, wherein the synaptic weight modifier comprises a weight change determiner configured to determine a further weight change parameter for modifying the synaptic weight parameter based on the weight change parameter received from the weight change accumulator corresponding to the synaptic weight parameter and the learning error outcome received from the learning error modulator corresponding to the synaptic weight parameter.

12. The neurosynaptic processing core according to claim 7, wherein
the pre-synaptic event accumulator, the post-synaptic event accumulator and the weight change accumulator are each configured to be triggered based on a first trigger signal associated with a first time step iteratively during the STDP learning, and
the learning error modulator and the synaptic weight modifier are each configured to be triggered based on a second trigger signal.

13. The neurosynaptic processing core according to claim 12, wherein
the pre-synaptic spike parameter incrementor of the pre-synaptic event accumulator is configured to be triggered based on the first trigger signal to receive the first pre-synaptic spike event input from the pre-synaptic block so as to increment the pre-synaptic spike parameter based on the first pre-synaptic spike event input received,
the post-synaptic spike parameter incrementor of the post-synaptic event accumulator is configured to be triggered based on the first trigger signal to receive the first post-synaptic spike event input from the post-synaptic block so as to increment the post-synaptic spike parameter based on the first post-synaptic spike event input received,

the synaptic spike event selector of the weight change accumulator is configured to be triggered based on the first trigger signal to receive the second pre-synaptic spike event input from the pre-synaptic block so as to select the post-synaptic spike parameter from the post-synaptic spike event memory block for output to the weight change parameter modifier based on the second pre-synaptic spike event input received or to receive the second post-synaptic spike event input from the post-synaptic block so as to select the pre-synaptic spike parameter from the pre-synaptic spike event memory block for output to the weight change parameter modifier based on the second post-synaptic spike event input received.

14. The neurosynaptic processing core according to claim 1, wherein one or more of the plurality of post-synaptic elements corresponds to one or more spiking neurons in a layer of the spiking neural network.

15. The neurosynaptic processing core according to claim 1, wherein the layer is an output layer of the spiking neural network.

16. A method of operating a neurosynaptic processing core with spike time dependent plasticity (STDP) learning for a spiking neural network,

the neurosynaptic processing core comprising:

a spiking neuron block comprising a pre-synaptic block and a post-synaptic block, the pre-synaptic block comprising a plurality of pre-synaptic elements and the post-synaptic block comprising a plurality of post-synaptic elements;

a synapse block communicatively coupled to the spiking neuron block, the synapse block comprising a plurality of synaptic weight parameters, each synaptic weight parameter corresponding to a neuron pair comprising a pre-synaptic element of the plurality of pre-synaptic elements and a post-synaptic element of the plurality of post-synaptic elements;

a STDP learning block communicatively coupled to the spiking neuron block and the synapse block, the STDP learning block comprising:

a pre-synaptic event accumulator comprising:

a pre-synaptic spike event memory block comprising a plurality of pre-synaptic spike parameters corresponding to the plurality of pre-synaptic elements,

respectively, each pre-synaptic spike parameter indicating a measure of one or more pre-synaptic spike events at the corresponding pre-synaptic element; and

a pre-synaptic spike parameter modifier configured to modify a pre-synaptic spike parameter of the plurality of pre-synaptic spike parameters based on a first pre-synaptic spike event input from the pre-synaptic block indicating a pre-synaptic spike event at the corresponding pre-synaptic element;

a post-synaptic event accumulator comprising:

a post-synaptic spike event memory block comprising a plurality of post-synaptic spike parameters corresponding to the plurality of post-synaptic elements, respectively, each post-synaptic spike parameter indicating a measure of one or more post-synaptic spike events at the corresponding post-synaptic element; and

a post-synaptic spike parameter modifier configured to modify a post-synaptic spike parameter of the plurality of post-synaptic spike parameters based on a first post-synaptic spike event input from the post-synaptic block indicating a post-synaptic spike event at the corresponding post-synaptic element; and

a weight change accumulator comprising:

a weight change memory block comprising a plurality of weight change parameters corresponding to the plurality of synaptic weight parameters, respectively; and

a weight change parameter modifier configured to modify a weight change parameter of the plurality of weight change parameters based a pre-synaptic spike parameter of the plurality of pre-synaptic spike parameters corresponding to the weight change parameter or a post-synaptic spike parameter of the plurality of post-synaptic spike parameters corresponding to the weight change parameter;

a learning error modulator configured to determine a plurality of learning errors associated with the STDP learning block for the plurality of synaptic weight parameters, respectively;

a synaptic weight modifier communicatively coupled to the STDP learning block, the learning error modulator and the synapse block, the synaptic weight modifier being configured to modify a synaptic weight parameter of the plurality of synaptic weight parameters based on a weight change parameter of the plurality of weight change parameters

corresponding to the synaptic weight parameter and a learning error of the plurality of learning errors corresponding to the synaptic weight parameter, and

the method comprising:

triggering the pre-synaptic event accumulator, the post-synaptic event accumulator and the weight change accumulator based on a first trigger signal associated with a first time step iteratively during the STDP learning; and triggering the learning error modulator and the synaptic weight modifier based on a second trigger signal; and

wherein the neurosynaptic processing core is formed by a plurality of processors.

17. The method according to claim 16, wherein

the pre-synaptic spike parameter modifier comprises a pre-synaptic spike parameter incrementor configured to increment the pre-synaptic spike parameter based on the first pre-synaptic spike event input received from the pre-synaptic block,

the post-synaptic spike parameter modifier comprises a post-synaptic spike parameter incrementor configured to increment the post-synaptic spike parameter based on the first post-synaptic spike event input received from the post-synaptic block, and

the weight change accumulator comprises a synaptic spike event selector configured to select the pre-synaptic spike parameter from the pre-synaptic spike event memory block for output to the weight change parameter modifier based on a second post-synaptic spike event input from the post-synaptic block indicating the post-synaptic spike event at the corresponding pre-synaptic element or select the post-synaptic spike parameter from the post-synaptic spike event memory block for output to the weight change parameter modifier based on a second pre-synaptic spike event input from the pre-synaptic block indicating the pre-synaptic spike event at the corresponding post-synaptic element,

said triggering the pre-synaptic event accumulator comprises triggering the pre-synaptic spike parameter incrementor of the pre-synaptic event accumulator based on the first trigger signal to receive the first pre-synaptic spike event input from the pre-synaptic block so as to increment the pre-synaptic spike parameter based on the first pre-synaptic spike event input received,

said triggering the post-synaptic event accumulator comprises triggering the post-synaptic spike parameter incrementor of the post-synaptic event accumulator based on the

first trigger signal to receive the first post-synaptic spike event input from the post-synaptic block so as to increment the post-synaptic spike parameter based on the first post-synaptic spike event input received, and

said triggering the weight change accumulator comprises triggering the synaptic spike event selector of the weight change accumulator based on the first trigger signal to receive the second pre-synaptic spike event input from the pre-synaptic block so as to select the post-synaptic spike parameter from the post-synaptic spike event memory block for output to the weight change parameter modifier based on the second post-synaptic spike event input received or to receive the second post-synaptic spike event input from the post-synaptic block so as to select the pre-synaptic spike parameter from the pre-synaptic spike event memory block for output to the weight change parameter modifier based on the second pre-synaptic spike event input received.

18. The method according to claim 17, wherein the learning error modulator comprises:

a learning error determiner configured to determine the plurality of learning errors for the plurality of synaptic weight parameters, respectively;

a learning error evaluator configured to determine a learning error outcome for the synaptic weight parameter based on a learning error of the plurality of learning errors corresponding to the synaptic weight parameter; and

a synaptic spike event record block comprising a plurality of post-synaptic spike event record parameters for the plurality of post-synaptic elements, respectively, each post-synaptic spike event record parameter indicating a number of post-synaptic spike events that occurred at the corresponding post-synaptic element, and

said triggering the learning error modulator comprising triggering the learning error determiner of the learning error modulator based on the second trigger signal to determine the plurality of learning errors for the plurality of synaptic weight parameters, respectively, the learning error determiner being configured to determine, for each of the plurality of synaptic weight parameters, the learning error for the synaptic weight parameter based on the post-synaptic spike event record parameter for the post-synaptic element corresponding to the

synaptic weight parameter and a reference parameter for the post-synaptic element corresponding to the synaptic weight parameter.

19. The method according to claim 18, wherein

wherein the synaptic weight modifier comprises a weight change determiner configured to determine a further weight change parameter for modifying the synaptic weight parameter based on the weight change parameter received from the weight change accumulator corresponding to the synaptic weight parameter and the learning error outcome received from the learning error modulator corresponding to the synaptic weight parameter, and

said triggering the synaptic weight modifier comprises triggering the synaptic weight modifier based on the second trigger signal to modify the synaptic weight parameter based on the weight change parameter received from the weight change accumulator corresponding to the synaptic weight parameter and the learning error outcome received from the learning error modulator corresponding to the synaptic weight parameter.

20. A method of forming a neurosynaptic processing core with spike time dependent plasticity (STDP) learning for a spiking neural network, the method comprising:

forming a spiking neuron block comprising a pre-synaptic block and a post-synaptic block, the pre-synaptic block comprising a plurality of pre-synaptic elements and the post-synaptic block comprising a plurality of post-synaptic elements;

forming a synapse block communicatively coupled to the spiking neuron block, the synapse block comprising a plurality of synaptic weight parameters, each synaptic weight parameter corresponding to a neuron pair comprising a pre-synaptic element of the plurality of pre-synaptic elements and a post-synaptic element of the plurality of post-synaptic elements;

forming a STDP learning block communicatively coupled to the spiking neuron block and the synapse block, the STDP learning block comprising:

a pre-synaptic event accumulator comprising:

a pre-synaptic spike event memory block comprising a plurality of pre-synaptic spike parameters corresponding to the plurality of pre-synaptic elements,

respectively, each pre-synaptic spike parameter indicating a measure of one or more pre-synaptic spike events at the corresponding pre-synaptic element; and

a pre-synaptic spike parameter modifier configured to modify a pre-synaptic spike parameter of the plurality of pre-synaptic spike parameters based on a first pre-synaptic spike event input from the pre-synaptic block indicating a pre-synaptic spike event at the corresponding pre-synaptic element;

a post-synaptic event accumulator comprising:

a post-synaptic spike event memory block comprising a plurality of post-synaptic spike parameters corresponding to the plurality of post-synaptic elements, respectively, each post-synaptic spike parameter indicating a measure of one or more post-synaptic spike events at the corresponding post-synaptic element; and

a post-synaptic spike parameter modifier configured to modify a post-synaptic spike parameter of the plurality of post-synaptic spike parameters based on a first post-synaptic spike event input from the post-synaptic block indicating a post-synaptic spike event at the corresponding post-synaptic element; and

a weight change accumulator comprising:

a weight change memory block comprising a plurality of weight change parameters corresponding to the plurality of synaptic weight parameters, respectively; and

a weight change parameter modifier configured to modify a weight change parameter of the plurality of weight change parameters based a pre-synaptic spike parameter of the plurality of pre-synaptic spike parameters corresponding to the weight change parameter or a post-synaptic spike parameter of the plurality of post-synaptic spike parameters corresponding to the weight change parameter;

forming a learning error modulator configured to determine a plurality of learning errors associated with the STDP learning block for the plurality of synaptic weight parameters, respectively; and

forming a synaptic weight modifier communicatively coupled to the STDP learning block, the learning error modulator and the synapse block, the synaptic weight modifier being configured to modify a synaptic weight parameter of the plurality of synaptic weight

parameters based on a weight change parameter of the plurality of weight change parameters corresponding to the synaptic weight parameter and a learning error of the plurality of learning errors corresponding to the synaptic weight parameter;

wherein the neurosynaptic processing core is formed by a plurality of processors.