AUXILIARY WRITES OVER ADDRESS CHANNEL

RELATED APPLICATIONS

[0001] The present Application for Patent claims priority to Provisional Application No. 60/776,517 entitled "Auxiliary Writes Over Address Channel" filed February 24, 2006, and assigned to the assignee hereof and hereby expressly incorporated by reference herein.

BACKGROUND

Field

[0002] The present disclosure relates generally to processing systems, and more specifically, to systems and techniques for performing auxiliary writes over the address channel of a bus.

Background

[0003] At the heart of most modern processing systems is an interconnect referred to as a bus. The bus moves information between various processing entities in the system. Today, most bus architectures are fairly standardized. These standardized bus architectures typically have independent and separate read, write and address channels.

[0004] This type of bus architecture is often found in processing systems with one or more general purpose processors supported by memory. In these systems, the memory provides a storage medium that holds the programs and data needed by the processors to perform their functions. A processor may read or write to the memory by placing an address on the address channel and sending the appropriate read/write control signal. Depending on the state of the read/write control, the processor either writes to the memory over the write channel or reads from the memory over the read channel. In these types of processing systems, as well as many others, it is desirable to reduce the write latency and increase the write bandwidth.

SUMMARY

[0005] One aspect of a processing system is disclosed. The processing system includes a receiving device, a bus having first, second and third channels, and a sending device configured to address the receiving device on the first channel, and read a payload from the receiving device on the second channel, the sending device being further configured to select between the first and third channels to write a payload to the receiving device.

[0006] Another aspect of a processing system is disclosed. The processing system includes a receiving device, a bus having first, second and third channels, means for addressing the receiving device on the first channel, means for reading a payload from the receiving device on the second channel, and means for selecting between the first and third channels to write a payload to the receiving device.

[0007] An aspect of a method of communicating between a sending device and one or more receiving devices over a bus is disclosed. The bus includes first, second and third channels. The method includes addressing a receiving device on the first channel, reading a payload from the receiving device on the second channel, and selecting between the first and third channels to write a payload to the receiving device.

[0008] An aspect of a bus mastering device is disclosed. The bus mastering device includes a processor, and a bus interface configured to interface the processor to a bus having first, second and third channels, the bus interface being further configured to address a slave on the first channel, receive a payload from the slave on the second channel, and select between the first and third channels to send a payload to the slave.

[0009] Another aspect of a bus mastering device is disclosed. The bus mastering device includes a processor, and means for interfacing the processor to a bus having first, second and third channels, the means for interfacing the processor to the bus comprising means for addressing a slave on the first channel, means for receiving a payload from the slave on the second channel, and means for selecting between the first and third channels to send a payload to the slave.

[0010] An aspect of a slave device is disclosed. The slave device includes memory, and a bus interface configured to interface the memory to a bus having first, second and third channels, the bus interface being configured to receive a memory address and a first payload from a bus

from the bus mastering device on the second channel, and send a payload to the bus mastering device on the third channel.

[0011] Another aspect of a slave device is disclosed. The slave device includes memory, and means for interfacing the memory to a bus having first, second and third channels, the means for interfacing the memory to the bus comprising means for receiving a memory address and a first payload from a bus mastering device on the first channel, means for receiving a second payload from the bus mastering device on the second channel, and means for sending a payload to the bus mastering device on the third channel.

[0012] It is understood that other embodiments of the present invention will become readily apparent to those skilled in the art from the following detailed description, wherein various embodiments of the invention are shown and described by way of illustration. As will be realized, the invention is capable of other and different embodiments and its several details are capable of modification in various other respects, all without departing from the spirit and scope of the present invention. Accordingly, the drawings and detailed description are to be regarded as illustrative in nature and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Aspects of the present invention are illustrated by way of example, and not by way of limitation, in the accompanying drawings, wherein:

[0014] FIG. 1 is a simplified block diagram illustrating an example of two devices in a processing system communicating over a bus;

[0015] FIG. 2 is an illustration showing information flowing on the address and write channels of a bus in the processing system of FIG. 1 with the address channel providing a generic medium for addresses and payloads;

[0016] FIG. 3 is a timing diagram showing three write operations over a bus in the processing system of FIG. 1;

[0017] FIG. 4 is a simplified block diagram illustrating a sending device in communication with two receiving devices in a processing system;

[0018] FIG. 5 is an illustration showing information flowing on the address and write channels of a bus in the processing system of FIG. 4

[0019] FIG. 6 is a simplified block diagram illustrating an example of two devices in a processing system communicating over a 4-channel bus;

[0020] FIG. 7 is a timing diagram showing three write operations over a bus in the processing system of FIG. 6;

[0021] FIG. 8 is a simplified block diagram illustrating a sending device in communication with three receiving devices in a processing system; and

[0022] FIG. 9 is an illustration showing information flowing on the read and write address channels and write channels of a bus in the processing system of FIG. 8.

DETAILED DESCRIPTION

[0023] The detailed description set forth below in connection with the appended drawings is intended as a description of various embodiments of the present invention and is not intended to represent the only embodiments in which the present invention may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of the present invention. However, it will be apparent to those skilled in the art that the present invention may be practiced without these specific details. In some instances, well-known structures and components are shown in block diagram form in order to avoid obscuring the concepts of the present invention.

[0024] FIG. 1 is a simplified block diagram illustrating an example of two devices in a processing system communicating over a bus. The processing system 100 may be a collection of hardware devices that cooperate to perform one or more processing functions. Typical applications of the processing system 100 include, but are not limited to, desktop computers, laptop computers, servers, cellular phones, personal digital assistants (PDA), game consoles, pagers, modems, audio equipment, medical devices, automotive, video equipment, industrial equipment, or any other machine or device capable of processing, retrieving and storing information.

[0025] The processing system 100 is shown with a sending device 102 in communication with a receiving device 104 over a bus 106. The bus 106 includes three channels: an address channel 106a, a write channel 106b, and a read channel 106c. A "channel" is defined as a set of electrical conductors used to carry information between two devices and which has a set of

address channel is 32-bits wide, and the write and read channels are each 64-bits wide. Typically, a bus interconnect (not shown) will be used to establish a point-to-point communications path between the sending device 102 and the receiving device 104 over the bus 106. Alternatively, the bus 106 may be a dedicated bus, a shared bus, or any other type of suitable bus architecture.

[0026] The sending device 102 may be any type of bus mastering device. In this example, the sending device 102 includes a processor 108 and a bus interface 110. The processor 108 may be a general purpose processor, such as a microprocessor, a special purpose processor, such as a digital signal processor (DSP), an application specific integrated circuit (ASIC), a direct memory access (DMA) controller, a bridge, a programmable logic component, or any other entity that requires access to the bus 106. The bus interface 110 is used to drive the address and write channels 106a, 106b, as well as provide the appropriate control signals. The bus interface 110 also serves as a receiver for the read channel 106c.

[0027] The receiving device 104 may be any type of slave device. The receiving device 104 may be temporary memory, such as SDRAM, DRAM, or RAM, or a longer term storage device such as flash memory, ROM memory, EPROM memory, EEPROM memory, CD-ROM, DVD, magnetic disk, rewritable optic disk and the like. Alternatively, the receiving device 104 may be a bridge or any other device capable of retrieving and storing information. In this example, the receiving device 104 includes a bus interface 112 and memory 114. The bus interface 112 is used to drive the read channel 106c and the appropriate control signals. The bus interface 112 also serves as a receiver for the address and write channels 106a, 106b. The memory 114 may be any device whose contents can be accessed (i.e., read and written to) randomly.

[0028] In this bus architecture, the sending device 102 may read or write to the receiving device 104. When the sending device 102 performs a write operation, it sends the address to the receiving device 104 on the address channel 106a with the appropriate control signals. The payload may be sent either on the address channel 106a or the write channel 106b. The "payload" refers to the data associated with a particular read or write operation, and in this case, a write operation. When the sending device performs a read operation, it sends the address to the receiving device 104 on the address channel 106a with the appropriate control signals. In response, the receiving device 104 sends

[0029] An example of three write operations will now be described with reference to FIG. 2. FIG. 2 is an illustration showing the information flowing on the address and write channels. In this example, the sending device initiates a 32-byte write operation followed by two 8-byte write operations.

[0030] Referring to FIG. 2, on the first clock cycle 202, the sending device initiates the 32-byte write operation by sending a 4-byte address A1 to the receiving device on the address channel 106a with the appropriate control signals. During the same clock cycle 202, the sending device also sends the first 8-bytes of the first payload W1(1) to the receiving device on the write channel 106b.

[0031] The sending device initiates the next write operation during the second clock cycle 204 by sending a 4-byte address A2 to the receiving device before completion of the first write operation on the address channel 106a with the appropriate control signals. The sending device continues to transmit the first payload during the same clock cycle by sending the second 8-bytes W1(2) to the receiving device on the write channel 106b.

[0032] The sending device then uses the next two clock cycles 206 and 208 to send the second payload to the receiving device on the address channel 106a, while concurrently completing the transmission of the first payload on the write channel 106b. In particular, in the third clock cycle 206, the sending device sends to the receiving device the first 4-bytes of the second payload W2(1) on the address channel 106a and the third 8-bytes of the first payload W1(3) on the write channel 106b. On the fourth clock cycle 208, the sending device sends to the receiving device the final 4-bytes of the second payload W2(2) on the address channel 106a and the final 8-bytes of the first payload W1(4) on the write channel 106b.

[0033] The sending device initiates the third write operation on the fifth clock cycle 210 by sending a 4-byte address A3 to the receiving device on the address channel 106a with the appropriate control signals. During the same clock cycle 210, the sending device also sends the third payload W3 to the receiving device on the write channel 106b.

[0034] Two control signals may be added to the address channel 106a to create a medium to support the transmission of both addresses and payloads. The first control signal, referred to as an "Address/Data" signal is used to indicate whether the

information being transmitted on the address channel 106a is an address or a payload. In this example, when the Address/Data signal is asserted, an address is being transmitted on the address channel 106a. Conversely, when the Address/Data signal is deasserted, the payload is being transmitted on the address channel 106a. The second control signal, referred to as a "Transfer Attribute," is used when transmitting an address on the address channel 106a. When an address is being transmitted, the "Transfer Attribute" signal is used to indicate whether the payload for that address will be transmitted on the address channel 106a or the write channel 106b.

[0035] An example illustrating how these control signals may be used will now be described with reference to FIG. 3. The bus protocol for the address and write channels 106a, 106b is shown below in Table 1. This bus protocol is being used to illustrate the inventive aspects of a processing system, with the understanding that such inventive aspects may be used with other bus protocols. Those skilled in the art will readily be able to vary and/or add signals to this protocol in the actual implementation of the bus architectures described herein.

TABLE 1

Address Channel		
Signal	**Definition**	**Driven By**
Address	32-bit medium to transmit addresses and payloads.	Sending Device
Address/Data	Indicates whether the information being transmitted on the address channel is an address or a payload.	Sending Device
AValid	Indicates whether valid information is being transmitted on the address channel.	Sending Device
Transfer Attribute	Indicates whether the payload for the current address will be transmitted on the address channel or the write channel.	Sending Device

Address Channel		
Signal	**Definition**	**Driven By**
Read/Write	Indicates whether a read or write operation is being requested.	Sending Device
Payload Size	Indicates the size of the payload for the current address.	Sending Device
Address Transfer Ack	Indicates whether the receiving device has successfully received information transmitted on the address channel.	Receiving Device

Write Channel		
Signal	**Definition**	**Driven By**
Write	64-bit medium to transmit payloads.	Sending Device
WValid	Indicates whether valid information is being transmitted on the write channel.	Sending Device
Write Transfer Ack	Indicates whether the receiving device has successfully received information transmitted on the write channel.	Receiving Device

[0036] FIG. 3 is a timing diagram showing the control signaling for the same three write operations described above in connection with FIG. 2. A System Clock 306 may be used to synchronize communications between the sending and receiving devices. The System Clock 306 is shown with five clock cycles, with each clock cycle numbered sequentially.

[0037] A write operation may be initiated on the address channel 106a by the sending device during the first clock cycle 301. This operation may be achieved by

308. Concurrently, the sending device asserts the AValid, Address/Data, and Transfer Attribute signals 312, 313, 314. The asserted AValid signal 312 indicates that valid information is being transmitted on the address channel 106a, the asserted Address/Data signal 313 indicates that the information is an address A1, and the asserted Transfer Attribute signal 314 indicates that the payload for the address A1 will be transmitted on the write channel 106b. The sending device also deasserts the Read/Write signal 316 to request a write operation. The Payload Size 318 signal may be used to indicate the size of the payload, which in this case is 32-bytes.

[0038] During the same first clock cycle 301, the sending device uses the Write medium 320 to transmit the first 8-bytes of the first payload W1(1). The sending device also asserts the WValid signal 324 to indicate that valid information is being transmitted on the write channel 106b.

[0039] At the end of the first clock cycle 301, the sending device checks for an asserted Address Transfer Ack signal 310 to confirm the successful delivery of the address A1 over the address channel 106a to the receiving device. The sending device also checks for an asserted Write Transfer Ack signal 322 to confirm the successful delivery of the first 8-bytes of the first payload W1(1) over the write channel 106b to the receiving device.

[0040] On the second clock cycle 302, the sending device transmits the address A2 for the second write operation on the 32-bit Address medium 308 before the first write operation completes. The sending device asserts the AValid signal 312 to indicate that valid information is being transmitted on the address channel 106a. The sending device also asserts the Address/Data signal 313 to indicate that the information is an address A2. The Transfer Attribute 314 is deasserted to indicate that the payload for the address A2 will be transmitted on the address channel 106a. The sending device also deasserts the Read/Write signal 316 to request a write operation. The Payload Size 318 signal may be used to indicate the size of the payload, which in this case is 8-bytes.

[0041] During the same second clock cycle 302, the sending device uses the Write medium 320 to send the second 8-bytes of the first payload W1(2). The sending device also asserts the WValid signal 324 to indicate that valid information is being transmitted on the write channel 106b.

[0042] At the end of the second clock cycle 302, the sending device checks for an asserted Address Transfer Ack signal 310 to confirm the successful delivery of the address A2 over the address channel 106a to the receiving device. The sending device also checks for an asserted Write Transfer Ack signal 322 to confirm the successful delivery of the second 8-bytes of the first payload W1(2) over the write channel 106b to the receiving device.

[0043] On the third clock cycle 303, the sending device transmits the first 4-bytes of the second payload W2(1) on the 32-bit Address medium 308. The sending device asserts the AValid signal 312 to indicate the valid information is being transmitted on the address channel 106a and deasserts the Address/Data signal 313 to indicate that the information is part of a payload. The state of the Transfer Attribute signal 314, Read/Write signal 316, and Payload Size 318 signal can be ignored during this clock cycle. In FIG. 3, the states for these signals remain unchanged, but could be set to any state.

[0044] During the same third clock cycle 303, the sending device uses the Write medium 320 to send the third 8-bytes of the first payload W1(3). The sending device also asserts the WValid signal 324 to indicate that valid information is being transmitted on the write channel 106b.

[0045] At the end of the third clock cycle 303, the sending device checks for an asserted Address Transfer Ack signal 310 to confirm the successful delivery of the first 4-bytes of the second payload W2(1) over the address channel 106a to the receiving device. The sending device also checks for an asserted Write Transfer Ack signal 322 to confirm the successful delivery of the third 8-bytes of the first payload W1(3) over the write channel 106b to the receiving device.

[0046] On the fourth clock cycle 304, the sending device transmits the final 4-bytes of the second payload W2(2) on the 32-bit Address medium 308. The sending device asserts the AValid signal 312 to indicate the valid information is being transmitted on the address channel 106a and deasserts the Address/Data signal 313 to indicate that the information is part of a payload. The state of the Transfer Attribute signal 314, Read/Write signal 316, and Payload Size 318 signal can be ignored during the payload tenure.

[0047] During the same fourth clock cycle 304, the sending device uses the Write medium 320 to send the final 8-bytes of the first payload W1(4). The sending device continues to assert the WValid signal 324 to indicate that valid information is being transmitted on the write channel 106b.

[0048] At the end of the fourth clock cycle 304, the sending device checks for an asserted Address Transfer Ack signal 310 to confirm the successful delivery of the final 4-bytes of the second payload W2(2) over the address channel 106a to the receiving device. The sending device also checks for an asserted Write Transfer Ack signal 322 to confirm the successful delivery of the final 8-bytes of the first payload W1(4) over the write channel 106b to the receiving device.

[0049] On the fifth clock cycle 305, the sending device transmits the address A3 for the third write operation on the 32-bit Address medium 308. The sending device asserts the AValid signal 312 to indicate that valid information is being transmitted on the address channel 106a. The sending device also asserts the Address/Data signal 313 to indicate that the information being transmitted on the address channel 106a is an address A3. The Transfer Attribute signal 314 is also asserted by the sending device to indicate that the payload for the address A3 will be transmitted on the write channel 106b. The Read/Write signal 316 remains deasserted to request a write operation. The Payload Size 318 signal may be used to indicate the size of the payload, which in this case is 8-bytes.

[0050] During the same fifth clock cycle 305, the sending device uses the Write medium 320 to send the payload W3. The sending device also asserts the WValid signal 324 to indicate that valid information is being transmitted on the write channel 106b.

[0051] At the end of the fifth clock cycle 305, the sending device checks for an asserted Address Transfer Ack signal 310 to confirm the successful delivery of the address A3 over the address channel 106a to the receiving device. The sending device also checks for an asserted Write Transfer Ack signal 322 to confirm the successful delivery of the third payload W3 over the write channel 106b to the receiving device.

[0052] FIG. 4 is a simplified block diagram illustrating a sending device 402 in communication with two receiving devices 404a, 404b through a bus interconnect 416 in a processing system 400. In this example, the sending device 402 can write to both

receiving devices 404a, 404b concurrently using the 32-bit address channel 406a as a medium for transmitting addresses and payloads to the bus interconnect 416. The bus interconnect 416 can then use the 32-bit address channels $406a_1$, $406a_2$ to address the receiving devices 404a, 404b and the 64-bit write channels $406b_1$, $406b_2$ to transmit the payloads. In the case where the bus interconnect 416 needs to perform multiple write operations to one or both receiving devices 404a, 404b, the address channels $406a_1$, $406a_2$ may also be used as media to transmit both addresses and payloads.

[0053] An example will now be described with reference to FIG. 5. FIG. 5 is an illustration showing the information flowing on the address and write channels. In this example, the bus interconnect 416 will provide point-to-point connections that allow each transmission from the sending device 402 to reach one of the receiving devices 404a, 404b in the same clock cycle. In practice, however, the bus interconnect 416 may be a clocked device with buffering (see FIG. 4).

[0054] Referring to FIG. 5, the sending device initiates a 32-byte write operation followed by an 8-byte write operation. On the first clock cycle 502, the sending device initiates the 32-byte write operation by sending an address A1 to the bus interconnect on the address channel 406a with the appropriate control signals. During the same clock cycle 502, the sending device also sends the first 8-bytes of the first payload W1(1) to the bus interconnect on the write channel 406b. The bus interconnect transmits the address A1 to the first receiving device 404a on the first receiving device's address channel $406a_1$, and transmits the first 8-bytes of the first payload W1(1) to the first receiving device 404a on the first receiving device's write channel $406b_1$.

[0055] On the second clock cycle 504, the sending device initiates the next write operation by sending an address A2 to the bus interconnect on the address channel 406a with the appropriate control signals. During the same clock cycle 504, the sending device also sends the second 8-bytes of the first payload W1(2) to the bus interconnect on the write channel 406b. The bus interconnect 416 transmits the address A2 to the second receiving device 404b on the second receiving device's address channel $406a_2$, and transmits the second 8-bytes of the first payload W1(2) to the first receiving device 404a on the first receiving device's write channel $406b_1$.

[0056] On the third and fourth clock cycles 506, 508, the sending device sends the remainder of the first payload W1(3), W1(4) through the bus interconnect to the first

receiving device 404a on the write channels 406b, 406b$_1$. During the same third and fourth clock cycles 506, 508, the sending device transmits the second payload W2(1), W2(2) to the bus interconnect on the address channel 406a. The second payload W2(1), W(2), being only 8-bytes, may be transmitted in the third and fourth clock cycles 506, 508 by the bus interconnect to the second receiving device over half the byte lanes on the second receiving device's write channel 406b$_2$. Alternatively, the bus interconnect can transmit the entire payload during the fourth clock cycle 508 on the 64-bit write channel 406b$_2$ for the second receiving device, as shown.

[0057] FIG. 6 is a simplified block diagram illustrating an example of two devices in a processing system 600 communicating over a 4-channel bus. A separate and independent address channel is provided for each of the read and write channels. In this example, each channel is 32-bits wide, but may be any width in practice depending upon the particular application and overall design constraints. A write operation over the 4-channel bus may be performed in the same way described earlier in connection with the 3-channel bus. That is, the sending device 602 transmits address on the write address channel 606a and payloads on both the write address channel 606a and the write channel 606b. The difference between the two bus architectures is the manner in which the read operation is performed. A read operation over the 4-channel bus is performed by sending to the receiving device 604 the address on a read address channel 606d. In response, the receiving device 604 sends the payload to the sending device 602 on the read channel 606c.

[0058] An example will now be described with reference to FIG. 7. The bus protocol for the address and write channels 606a, 606b, 606d is listed below in Table 2. This bus protocol is being used to illustrate the inventive aspects of a processing system, with the understanding that such inventive aspects may be used with other bus protocols. Those skilled in the art will readily be able to vary and/or add signals to this protocol in the actual implementation of the bus architectures described herein.

TABLE 2

Write Address Channel		
Signal	**Definition**	**Driven By**
Write Address	32-bit medium to transmit	Sending Device

Write Address Channel		
Signal	**Definition**	**Driven By**
	payloads.	
Write Address/Data	Indicates whether the information being transmitted on the write address channel is a write address or a payload.	Sending Device
Transfer Attribute	Indicates whether the payload for the current address will be transmitted on the write address channel, read address channel or the write channel.	Sending Device
Write AValid	Indicates whether valid information is being transmitted on the write address channel.	Sending Device
Write Payload Size	Indicates the size of the payload for the current write address.	Sending Device
Write Address Transfer Ack	Indicates whether the receiving device has successfully received information transmitted on the write address channel.	Receiving Device

Read Address Channel		
Signal	**Definition**	**Driven By**
Read Address	32-bit medium to transmit read addresses and payloads.	Sending Device
Read Address/Data	Indicates whether the information being transmitted on the read address channel is a read address or a payload.	Sending Device

Read Address Channel		
Signal	**Definition**	**Driven By**
Read AValid	Indicates whether valid information is being transmitted on the read address channel.	
Read Payload Size	Indicates the size of the payload for the current read address.	Sending Device
Read Address Transfer Ack	Indicates whether the receiving device has successfully received information transmitted on the read address channel.	Receiving Device

Write Channel		
Signal	**Definition**	**Driven By**
Write	32-bit medium to transmit payloads.	Sending Device
WValid	Indicates whether valid information is being transmitted on the write channel.	Sending Device
Write Transfer Ack	Indicates whether the receiving device has successfully received information transmitted on the write channel.	Receiving Device

[0059] The protocol for the Transfer Ack signal on the write address channel is shown below in Table 3.

TABLE 3

Transfer Attribute	Definition
000	Payload for the current address will be transmitted on the write channel.
001	Payload for the current address will be transmitted on the write address channel.

010	Payload for the current address will be transmitted on the read address channel.
011	Reserved

[0060] FIG. 7 is a timing diagram showing the control signaling for a 16-byte write operation followed by a 12-byte write operation and then a 4-byte write operation. A System Clock 706 may be used to synchronize communications between the sending and receiving devices. The System Clock 706 is shown with four clock cycles, with each clock cycle numbered sequentially.

[0061] A write operation may be initiated on the address channel 606a by the sending device during the first clock cycle 701. This operation may be achieved by transmitting the address A1 for the first write operation on the 32-bit Write Address medium 708. During the same clock cycle 701, the sending device asserts the Write AValid signal 712 to indicate that valid information is being transmitted on the write address channel 606a. The sending device also asserts the write Address/Data signal 713 to indicate that the information is an address A1. The sending device also sets the Transfer Attribute signal 714 to "000" to indicate that the payload for the address A1 will be transmitted on the write channel 606b. The Payload Size 718 signal may be used to indicate the size of the payload, which in this case is 16-bytes.

[0062] During the same first clock cycle 701, the sending device uses the Write medium 720 to transmit the first 4-bytes of the first payload W1(1). The sending device also asserts the WValid signal 724 to indicate that valid information is being transmitted on the write channel 606b.

[0063] At the end of the first clock cycle 701, the sending device checks for an asserted Write Address Transfer Ack signal 710 to confirm the successful delivery of the address A1 over the address channel 606a to the receiving device. The sending device also checks for an asserted Write Transfer Ack signal 722 to confirm the successful delivery of the first 4-bytes of the first payload W1(1) over the write channel 606b to the receiving device.

[0064] On the second clock cycle 702, the sending device transmits the address A2 for the second write operation on the 32-bit Address medium 708 before the first write operation completes. The sending device asserts the Write AValid signal 712 to

The sending device also asserts the Address/Data signal 713 to indicate that the information is an address A2. The sending device sets the Transfer Attribute signal 714 to "010" to indicate that the payload for the address A2 will be transmitted on the read address channel 606d. The Payload Size 718 signal may be used to indicate the size of the payload, which in this case is 12-bytes.

[0065] During the same second clock cycle 702, the sending device uses the Write medium 720 to transmit the second 4-bytes of the first payload W1(2), and asserts the WValid signal 724 to indicate that valid information is being transmitted on the write channel 606b. The sending device uses the Read Address medium 730 to send the first 4-bytes of the second payload W2(1), and asserts the Read AValid signal 728 to indicate that valid information is being transmitted on the read address channel 606d. The sending device deasserts the Read Address/Data signal 729 to indicate that the information being transmitted on the read address channel 606d is payload data.

[0066] At the end of the second clock cycle 702, the sending device checks for an asserted Write Address Transfer Ack signal 710 to confirm the successful delivery of the address A2 over the address channel 606a to the receiving device. The sending device also checks for asserted Write Transfer Ack and Read Address Transfer Ack signals 722, 726 to confirm the successful delivery of the payload data over the write and read address channels 606b, 606d.

[0067] On the third clock cycle 703, the sending device asserts the Write AValid signal 712 to indicate that valid information is being transmitted on the write address channel 606a. The sending device also asserts the Address/Data signal 713 to indicate that the information is an address A3. The sending device sets the Transfer Attribute signal 714 to "001" to indicate that the payload for the address A3 will be transmitted on the write address channel 606a. The Payload Size 718 signal may be used to indicate the size of the payload, which in this case is 4-bytes.

[0068] During the same third clock cycle 703, the sending device uses the Write medium 720 to transmit the third 4-bytes of the first payload W1(3), and asserts the WValid signal 724 to indicate that valid information is being transmitted on the write channel 606b. The sending device uses the Read Address medium 730 to send the second 4-bytes of the second payload W2(2), and asserts the Read AValid signal 728 to indicate that valid information is being transmitted on the read address channel 606d.

The sending device deasserts the Read Address/Data signal 729 to indicate that the information being transmitted on the read address channel 606d is payload data.

[0069] At the end of the third clock cycle 703, the sending device checks for an asserted Write Address Transfer Ack signal 710 to confirm the successful delivery of the address A3 over the address channel 606a to the receiving device. The sending device also checks for asserted Write Transfer Ack and Read Address Transfer Ack signals 722, 726 to confirm the successful delivery of the payload data over the write and read address channels 606b, 606d.

[0070] On the fourth clock cycle 704, the sending device uses the Write medium 720 to send the final 4-bytes of the first payload W1(4), and the Read Address medium 730 to send the final 4-bytes of the second payload W2(3). The sending device asserts the WValid and Read AValid signals 724, 728 to indicate that valid information is being transmitted on the write and read address channels 606b, 606d. The sending device deasserts the Read Address/Data signal 729 to indicate that the information being transmitted on the read address channel 606d is payload data.

[0071] The sending device uses Write address medium 708 to send the third payload W3, and asserts the Write AValid signal 712 to indicate that valid information is being sent on the write address channel 606a. The sending device deasserts the Address/Data signal 713 to indicate that the information transmitted on the write address channel 606a is payload data. The state of the Transfer Attribute signal 714 and Payload Size 718 signal may ignored.

[0072] FIG. 8 is a simplified block diagram illustrating a sending device 802 in communication with three receiving devices 804a-804c through a bus interconnect 816 in a processing system 800. In this example, the sending device 802 can write to all three receiving devices 804a-804c concurrently using the read and write address channels 806d, 806a as media for transmitting addresses and payloads. The bus interconnect 816 can then use the write address channels $806a_1$, $806a_2$, $806a_3$ to address the receiving devices 804a, 804b, 804c and the write channels $806b_1$, $806b_2$, $806b_3$ to transmit the payloads. In the case where the bus interconnect 816 needs to perform multiple write operations to one or more receiving devices 804a, 804b, 804c, the read and write address channels $806d_1$, $806d_2$, $806d_3$, $806a_1$, $806a_2$, $806a_3$ may also be used as generic media to transmit both addresses and payloads.

[0073] An example of will now be described with reference to FIG. 9. FIG. 9 is an illustration showing the information flowing on the address and write channels. In this example, the bus interconnect 816 will provide point-to-point connections that allow each transmission from the sending device 802 to reach one of the receiving devices 804a, 804b, 804c in the same clock cycle. In practice, however, the bus interconnect 816 may be a clocked device with buffering (see FIG. 8).

[0074] Referring to FIG. 9, on the first clock cycle 902, the sending device initiates the 16-byte write operation by sending an address A1 to the bus interconnect on the address channel 806a with the appropriate control signals. During the same clock cycle 902, the sending device also sends the first 4-bytes of the first payload W1(1) to the bus interconnect on the write channel 806b. The bus interconnect transmits the address A1 to the first receiving device 804a on the first receiving device's address channel $806a_1$, and transmits the first 4-bytes of the first payload W1(1) to the first receiving device 804a on the first receiving device's write channel $806b_1$.

[0075] On the second clock cycle 904, the sending device initiates the next write operation by sending an address A2 to the bus interconnect on the address channel 806a with the appropriate control signals. During the same clock cycle 904, the sending device also sends the second 4-bytes of the first payload W1(2) to the bus interconnect on the write channel 806b and the first 4-bytes of the second payload W2(1) to the bus interconnect on the read address channel 806d. The bus interconnect 816 transmits the address A2 to the second receiving device 804b on the second receiving device's address channel $806a_2$, transmits the second 4-bytes of the first payload W1(2) to the first receiving device 804a on the first receiving device's write channel $806b_1$, and transmits the first 4-bytes of the second payload W2(1) to the second receiving device 804b on the second receiving device's write channel $806b_2$.

[0076] On the third clock cycle 906, the sending device initiates the next write operation by sending an address A3 to the bus interconnect on the address channel 806a with the appropriate control signals. At the same time, the sending device also sends the third 4-bytes of the first payload W1(3) to the bus interconnect on the write channel 806b, and the second 4-bytes of the second payload W2(2) to the bus interconnect on the read address channel 806d. The bus interconnect 816 transmits the address A3 to the third receiving device 804c on the third receiving device's address channel $806a_3$,

on the first receiving device's write channel $806b_1$, and transmits the second 4-bytes of the second payload W2(2) to the second receiving device 804b on the second receiving device's write channel $806b_2$.

[0077] On the fourth clock cycle 908, the sending device sends the final 4-bytes of the first payload W1(4) to the bus interconnect on the write channel 806b, the final 4-bytes of the second payload W2(3) to the bus interconnect on the read address channel 806d, and the third payload W3 to the bus interconnect on the write address channel 806a. The bus interconnect 816 transmits the final 4-bytes of the first payload W1(4) to the first receiving device 804a on the first receiving device's write channel $806b_1$, transmits the final 4-bytes of the second payload W2(3) to the second receiving device 804b on the second receiving device's write channel $806b_2$, and transmits the third payload W3 to the third receiving device 804c on the third receiving device's write channel $806b_3$.

[0078] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic component, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing components, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0079] The methods or algorithms described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. A storage medium may be coupled to the processor such that the processor can read information from, and write information to, the storage medium. In

the storage medium may reside in an ASIC. The ASIC may reside in the sending and/or receiving component, or elsewhere. In the alternative, the processor and the storage medium may reside as discrete components in the sending and/or receiving component, or elsewhere.

[0080] The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

CLAIMS

1. A processing system, comprising:

a receiving device;

a bus having first, second and third channels; and

a sending device configured to address the receiving device on the first channel, and read a payload from the receiving device on the second channel, the sending device being further configured to select between the first and third channels to write a payload to the receiving device.

2. The processing system of claim 1 wherein the sending device is further configured to write the payload to a first address of the receiving device on the first channel and write a second payload to a second address of the receiving device on the third channel.

3. The processing system of claim 1 further comprising a second receiving device, and wherein the sending device is further configured to write the payload to the receiving device on the first channel and write a payload to the second receiving device on the third channel.

4. The processing system of claim 1 wherein the bus further comprises a fourth channel, the sending device being further configured to address the receiving device on the first channel for write operations and address the receiving device on the fourth channel for read operations, and wherein the sending device is further configured to select between the first, third and fourth channels to write the payload to the receiving device.

5. The processing system of claim 4 wherein the sending device is further configured to write the payload to a first address of the receiving device on one of the first, third and fourth channels and write a second payload to a second address of the receiving device on another one of the first, third and fourth channels.

6. The processing system of claim 4 wherein the sending device is further configured to write the payload to a first address of the receiving device on the first channel, write a second payload to a second address of the receiving device on the third channel, and write a third payload to a third address of the receiving device on the fourth channel.

7. The processing system of claim 4 further comprising a second receiving device, and wherein the sending device is further configured to write the payload to the receiving device on one of the first, third and fourth channels and write a second payload to the second receiving device on another one of the first, third and fourth channels.

8. The processing system of claim 4 further comprising second and third receiving devices, and wherein the sending device is further configured to write the payload to the receiving device on the first channel, write a second payload to the second receiving device on the third channel, and write a third payload to the third receiving device on the fourth channel.

9. The processing system of claim 1 wherein the sending device is further configured to provide a control signal to the receiving device indicating whether the first channel is currently being used to address the receiving device or write the payload to the receiving device.

10. The processing system of claim 1 wherein the sending device is further configured to provide a control signal to the receiving device while addressing the receiving device, the control signal indicating whether a payload for the address will be written to the receiving device on the first or third channel.

11. A processing system, comprising:

a receiving device;

a bus having first, second and third channels;

means for addressing the receiving device on the first channel;

means for reading a payload from the receiving device on the second channel; and

means for selecting between the first and third channels to write a payload to the receiving device.

12. A method of communicating between a sending device and one or more receiving devices over a bus, the bus comprising first, second and third channels, the method comprising:

addressing a receiving device on the first channel,

reading a payload from the receiving device on the second channel; and

selecting between the first and third channels to write a payload to the receiving device.

13. The method of claim 12 further comprising writing the payload to a first address of the receiving device on the first channel and writing a second payload to a second address of the receiving device on the third channel.

14. The method of claim 12 further comprising writing the payload to the receiving device on the first channel and writing a second payload to a second receiving device on the third channel.

15. The method of claim 12 wherein the bus further comprises a fourth channel, and wherein the receiving device is addressed on the first channel for a write operation, the method further comprising addressing the receiving device on the fourth channel for a read operation, wherein the selection of which channel to write the payload to the receiving device further comprises selecting between the first, third and fourth channels to write the payload to the receiving device.

16. The method of claim 15 further comprising writing the payload to a first address of the receiving device on one of the first, third and fourth channels and writing a second payload to a second address of the receiving device on another one of the first, third and fourth channels.

17. The method of claim 15 further comprising writing the payload to a first address of the receiving device on the first channels and writing a second payload to a

second address of the receiving device on the third channel and writing a third payload to a third address of the receiving device on the fourth channel.

18. The method of claim 15 further comprising writing the payload to the receiving device on one of the first, third and fourth channels and writing a second payload to a second receiving device on another one of the first, third and fourth channels.

19. The method of claim 15 further comprising writing the payload to the receiving device on the first channel and writing a second payload to a second receiving device on the third channel and writing a third payload to a third receiving device on the fourth channel.

20. The method of claim 12 further comprising providing a control signal to the receiving device indicating whether the first channel is currently being used to address the receiving device or write a payload to the receiving device.

21. The method of claim 12 further comprising providing a control signal to the receiving device while addressing the receiving device, the control signal indicating whether a payload for the address will be written to the receiving device on the first or third channel.

22. A bus mastering device, comprising:

a processor; and

a bus interface configured to interface the processor to a bus having first, second and third channels, the bus interface being further configured to address a slave on the first channel, receive a payload from the slave on the second channel, and select between the first and third channels to send a payload to the slave.

23. The bus mastering device of claim 22 wherein the bus interface device is further configured to send the payload to a first address of the slave on the first channel and send a second payload to a second address of the slave on the third channel.

24. The bus mastering device of claim 22 wherein the bus interface is further configured to send the payload to the slave on the first channel and send a payload to a second slave on the third channel.

25. The bus mastering device of claim 22 wherein the bus further comprises a fourth channel, and wherein the bus interface is further configured to address the slave on the first channel for write operations and address the slave on the fourth channel for read operations, and wherein the sending device is further configured to select between the first, third and fourth channels to write the payload to the slave.

26. The bus mastering device of claim 25 wherein the bus interface is further configured to send the payload to a first address of the slave on one of the first, third and fourth channels and send a second payload to a second address of the slave on another one of the first, third and fourth channels.

27. The bus mastering device of claim 25 wherein the bus interface is further configured to send the payload to a first address of the slave on the first channel, send a second payload to a second address of the slave on the third channel, and send a third payload to a third address of the slave on the fourth channel.

28. The bus mastering device of claim 25 wherein the bus interface is further configured to send the payload to the slave on one of the first, third and fourth channels and send a second payload to a second slave on another one of the first, third and fourth channels.

29. The bus mastering device of claim 25 further comprising second and third slaves, and wherein the bus interface is further configured to send the payload to the slave on the first channel, send a second payload to a second slave on the third channel, and send a third payload to a third slave on the fourth channel.

30. The bus mastering device of claim 22 wherein the bus interface is further configured to provide a control signal to the slave indicating whether the first channel is currently being used to address the slave or send the payload to the slave.

31. The bus mastering device of claim 22 wherein the bus interface is further configured to provide a control signal to the slave while addressing the slave, the control signal indicating whether a payload for the address will be sent to the slave on the first or third channel.

32. A bus mastering device, comprising:

a processor; and

means for interfacing the processor to a bus having first, second and third channels, the means for interfacing the processor to the bus comprising means for addressing a slave on the first channel, means for receiving a payload from the slave on the second channel, and means for selecting between the first and third channels to send a payload to the slave.

33. A slave device, comprising:

memory; and

a bus interface configured to interface the memory to a bus having first, second and third channels, the bus interface being configured to receive a memory address and a first payload from a bus mastering device on the first channel, receive a second payload from the bus mastering device on the second channel, and send a payload to the bus mastering device on the third channel.

34. The slave device of claim 33 wherein the bus interface is further configured to receive the first and second payloads.

35. The slave device of claim 33 wherein the bus further comprises a fourth channel, wherein the memory is further configured to be addressed through the bus interface by the sending the device on the first channel for write operations and on the fourth channel for read operation, the bus interface being further configured to receive a third payload from the bus mastering device on the fourth channel.

36. The slave device of claim 35 wherein the bus interface is further configured to receive the first, second and third payloads.

37. The slave device of claim 34 wherein the bus interface is further configured to receive a control signal from the bus mastering device indicating whether the first channel is currently being used to address the memory or send the first payload.

38. The slave device of claim 22 wherein the bus interface is further configured to receive a control signal from the bus mastering device while the memory is being addressed, the control signal indicating whether a payload for the address will be received on the first or third channel.

39. A slave device, comprising:

memory; and

means for interfacing the memory to a bus having first, second and third channels, the means for interfacing the memory to the bus comprising means for receiving a memory address and a first payload from a bus mastering device on the first channel, means for receiving a second payload from the bus mastering device on the second channel, and means for sending a payload to the bus mastering device on the third channel.