ELECTROSTATIC CHUCK FOR WAFERS

FIELD OF THE INVENTION

The present invention relates to an electrostatic chuck for wafers and especially to a mobile, transportable electrostatic chuck where the chuck keeps clamping a thin wafer after charging (application of a clamping voltage) without permanent connection to an external power supply unit for transportation or other process steps up to several hours.

BACKGROUND OF THE INVENTION

Mobile, transportable electrostatic chucks (Transfer-ESC) are used as mechanical support carriers for thin substrates. This technology is applied to the manufacturing of integrated circuits (IC's) within the semiconductor industry. The tendency to thinner chips or wafers is evident in RFID-Chip products as well as for Power-Chips and many different other applications. These support carriers allow safe manipulation of thin, brittle wafers on existing production equipment because the size and thickness of the clamped substrate on the mobile, transportable electrostatic chuck is similar in size, thickness and shape to a standard wafer. An advantage of the support carrier technique is the reversible clamping of the transport substrates outside the production equipment. Besides, after charging the Transfer-ESC, there is no need for additional, external current or voltage power supply for a long period of time. For this reason the package of Transfer-ESC and thin wafer can be handled as a normal thick wafer. The existing transport and process equipment (grinding, etching or polishing equipment, implanting, PVD, sputtering or CVD tools - see DE 20311625 U1 can be employed. After a completed process step, the

thin wafer or the separated chips can be taken off the Transfer-ESC after deactivating the electrostatic clamping force or it can be recharged again. The Transfer-ESC is reusable. Similar problems as described are found in other industrial branches such as the medicine, solar or display industry. As used herein, "wafer" encompasses any of the various types of substrates that can be held on a chuck, including semiconductor wafers, glass or ceramic plates, or any of various other suitable substrates.

State of the art for 150 µm thin wafers is the use of polymer protection foils for mechanical stabilisation. This support technique seems applicable to a wafer thickness down to 100 µm. The attached/glued protection foils must be peeled off mechanically after later process steps. This can lead to a breakage of the brittle, sensitive wafers. The disadvantage of this technique is that the foils are not reusable and are not resistant to higher temperatures. Their application is limited to process steps where the temperature is less than 150 degree Celsius.

Alternatively, Transfer-ESC can be employed as stabilising carriers instead of foils. The connection of a thin wafer and the Transfer-ESC is carried out by applying a clamping voltage (typically 300 V to 3000 V). An electrostatic field is created between the electrode structure within the Transfer-ESC and the wafer. The resulting clamping force is similar to the Coulomb force of a plate capacitor. After clamping the Transfer-ESC with the attached wafer, it can be transported or processed without any further connection to a voltage or current supply system. After a couple of hours, another recharging of the Transfer-ESC is necessary, because the leakage currents of the capacitor structure (typically < 5 nA at room temperature)

discharge with time and the clamping forces are reduced. This can lead to detaching of the clamped wafer.

In EP 1217655 A1 a method of manipulating thin wafers is described, which uses the term "Transfer-ESC" the first time for transportable, electrostatic chucks. US 2004/0037692 A1 Landesberger et al describes electrodes, which are arranged in a matrix. By providing the electrode structure in the form of a matrix, individual chips can be removed "pixelwise" by reversing the polarity of respective electrodes of the matrix. Landesberger et al describes in Fig. 2 a round structure, which consists of quarter-circular-segment electrodes. Each two of the electrodes are connected to each other and once activated they are at a positive (+) or negative (-) potential. For de-chucking a chip, the appropriate electrode structure is deactivated using the matrix structure and by reversing the polarity of at least two of the electrodes the chip can be taken off.

By contrast to mobile, transportable electrostatic chucks, stationary electrostatic chucks (ESC) have been used to clamp wafers in manufacturing tools for the chip industry for decades. Stationary ESC as well as end effectors differ in that they are permanently connected to a power supply unit and thus are not mobile. For this reason leakage current in respect of an insufficient power supply has been of less concern. These ESC are mostly modified to achieve fast chucking and de-chucking cycle times. In addition, many different designs for electrode structures have been developed. Some examples for unipolar, bipolar and multipolar electrode structures are found in US 4551192, US 4480284, US 4184188, US 4384918, US 4692836, US 4724510, US 5572398, US 5151845, US 6174583, EP 0692814, EP 0460955 and EP 1070381. In EP 0880818 B1 a low voltage

electrostatic clamp is described. The clamping force not only depends on the applied voltage, but is also significantly influenced by the structure of the electrodes. The formula for calculating the value of Coulomb forces for unipolar and bipolar chucks is known from analogous considerations of plate capacitors. By using two differently charged elongated serpentine-like electrodes with a width of < 100 µm and a spacing between the electrodes of less than 100 µm it was found that clamping forces are improved and higher than expected. It is argued that a non-uniform electric field is created. This non-uniform electric field has an additional force component. A dielectric object (wafer) can be electrostatically clamped by immersing the object in a non-uniform electric field. The non-uniform electric field produces a force which tends to pull the dielectric object into the region of the strongest electric field. For this reason the same clamping force is achieved with a reduced applied clamping voltage. By using a flat-panel-display (AMLCD) manufacturing technology, the smallest width of the electrodes in an array of electrodes is 20 µm and the deposited dielectric layer has a thickness of 5 µm. The clamping voltage required is less than 1 kV. State of the art types of stationary ESC have widths of the electrodes of about 3 mm and the spacing between the electrodes is about 1 mm. Typically they work with clamping voltages in the range of 1 kV to 3 kV. The thickness of the dielectric layer is in the range of 10 µm to 500 µm. Different thick-film technologies are applied to produce stationary ESC.

EP 805487 A2 describes the use of fuses to electrically disconnect a failed electrode from an output terminal. This application is related to a stationary ESC permanently connected to a power supply unit. The resistor fuses are constructed from resistive materials such as nickel-phosphorous, nickel-chromium or the like with a length of up to 5 mm. The

disadvantage of these types of fuses is that they are not able to be integrated using a suitable thin-film technology.

The proposed solutions do not fulfil technical and commercial requirements with respect to mobile, transportable electrostatic chucks. Although the risk of breakage of thin (< 150 µm) and ultra thin (< 50 µm) substrates is drastically reduced by using Transfer-ESC during the manufacturing and transport of wafers, the clamping power is still problematic for some process steps. Those process steps are CVD, metallization and annealing processes, which are carried out at temperatures up to 750 degree Celsius. The clamping force of Coulomb chucks is proportional to the square of the applied clamping voltage (U), the dielectric constant (ε_r) of the insulator layer, and is inversely proportional to the square of the thickness of the insulator layer (d). Thus, a strong electrostatic holding force is obtained by having a high clamping voltage (U > 1000 V) with a high dielectric constant of the material (ε_r is 3.5 to 9) and a very small thickness of the insulation layer. Most of the typically used dielectric materials, as described in the patents above, exhibit a significant decrease in their insulation behaviour at elevated temperatures of about 250 degree Celsius. This leads to high leakage currents and thus only a short clamping time. A major drawback is also that a single defect of the dielectric layer can cause total failure of the Transfer-ESC.

BRIEF SUMMARY OF THE INVENTION

In view of the shortcomings described above, the object of the invention is to produce mobile, transportable electrostatic chucks (Transfer-ESC) at a reasonable cost which work at elevated temperatures with low leakage current, create a high, preferably increased clamping force and are still able to work if there are defects within the dielectric layer.

According to the invention the solution of a new type of mobile, transportable electrostatic chucks is described in claim 1. Each cluster is preferably connected to at least one integrated fuse, which disconnects defective clusters.

In order to create a large number of the cells, thin-film techniques known from the manufacturing process of integrated circuits (chips) are applied. Each cell comprises an inner electrode tip, a lateral insulator layer, an outer electrode surround and a top dielectric layer. It is known that SiO_2 has a high breakdown voltage of up to 1000 V per µm. In addition, it is possible to create very pure and defect-free silicon dioxide layers which generate only small amounts of leakage currents at 300 degree Celsius. Taking into account that breakdown voltages from 200 V to 2000 V are needed, the width of the lateral insulating layer is preferably 2 µm, which separates the inner electrode tip from the outer electrode surround.

Quadratic or hexagonal shapes of cells enable the highest density of cells on a surface. Currently, a line width of 0.5 µm and below is widely used for IC manufacturing. Taking

this into account, a quadratic cell preferably has an inner electrode tip of 0.5µm * 0.5µm, the lateral insulator layer a width of 2 µm and the outer electrode surround a width of 0.5 µm. Using these dimensions, a lattice constant of 5µm of a quadratic cell can be calculated. If, by example, 6 * 6 cells are combined into a cluster, each cluster would have a surface area of 30 * 30 μm^2. Each cluster is preferably connected to at least one fuse. This fuse will disconnect the electrical connection from the cluster if the current density is too high. This, for instance, can be created by a defect within the top dielectric layer. A typical defect size during the IC manufacturing process is in the range of 1 µm or smaller. This defect can cause an elevated leakage current, i.e. an electric shock current, which is much higher than the normal leakage current. This leakage current can be as high as a few mA and melts the fuse, because the current density of the fuse material is above the critical limit for a short period of time. Therefore the contact with the cluster will be disconnected. The electrodes can each be formed by a plurality of these clusters and for this reason the functionality of an electrode will not be seriously affected by a local defect. The integrated fuses are designed so that the charging and discharging procedure of a Transfer-ESC is not influenced. Experience shows that a defect will be recognized during the charging procedure of the Transfer-ESC. The charging of a Transfer-ESC is carried out with a rising clamping voltage, but with a limitation of the charging current from 30 to 300 µA. This small and tightly controlled charging current, distributed by a bus-system to a large number of integrated fuses (up to one million or more), enables a technical solution for the use of fuses within a thin-film technology and thus a complete integration in the manufacturing process, known from semiconductor IC technologies. If one cluster is destroyed

during the charging procedure, the Transfer-ESC, using a million of those clusters, retains its functionality. Considering a cell construction with a 5 µm lattice, the resulting cluster density is 1,000 clusters per square millimetre. Applied to a 150 mm Transfer-ESC, it means that there are more than 500,000,000 individual active cells.

BRIEF DESCRIPTION OF THE DRAWINGS

A preferred embodiment of the invention is explained below referring to the accompanying drawings, in which:

Figs. 1a and 1b are top views of quadratic and hexagonal electrode cells respectively;

Fig. 2 is a top view of a cluster of cells;

Fig. 3 is a top view of an integrated fuse, the positioning of the cluster being indicated by dotted lines;

Fig. 4 is a top view of a section of a bus system;

Fig. 5 is a cross-sectional view of a cell with an integrated fuse in the second level and as part of the bus system; and

Fig. 6 is a cross-sectional view of cells with additional integrated capacitors, embedded in the base-material of the Transfer-ESC, and a process-wafer to be clamped thereon, as well as rear side contacts for charging and discharging of the electrodes and separate contacts for capacitors.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1a shows a quadratic and **Fig. 1b** a hexagonal shape of an electrode cell (10). It is constructed from an inner electrode peak (1), a lateral insulator layer (2), an outer electrode surround (3) and a top dielectric layer (8). The preferred material for the electrode tip (1) and the electrode surround (3) is electrically conductive metal such as copper, aluminium or tungsten, but highly-doped poly silicon or amorphous silicon can be employed. The material for the layers (2,8) is typically thermal, CVD or plasma oxide, nitride or other suitable non-conductive layer materials or material combinations. By joining the electrode cells (10) to each other, a complete coverage of the surface, as seen in **Fig. 2**, is achieved. In this case a cluster (4) of 6 * 6 cells (10) is described.

As normal for IC manufacturing technologies, many different functional levels can be arranged one above the other. Thus, an integrated fuse (5) can be positioned directly below each cluster (4). **Fig. 3** shows an integrated fuse (5) with a serpentine-like track (6). The conductive track (6) is designed to achieve a length-to-width ratio of typically 300 to 1. The resistance of the integrated fuse (5) in this embodiment is designed to reach more than 10,000 Ohm. This is achieved by using amorphous or poly crystalline silicon tracks with an appropriate doping, but the use of a thin metal layer is also possible. In Fig. 3 a 125 µm long conductive track (6) is shown, which melts and cuts off the contact of the cluster (4) with a bus system (7) in case of an electric shock current. Individual integrated fuses (5) are connected by a bus system (7) to each other, as seen in **Fig. 4**.

Fig. 5 shows an electrode cell (10) and its electric field. Here the cross-sectional view of the cell (10) with integrated fuse (5) in a second level and as part of a bus system (7) is shown. In this embodiment the bus system (7) is linked via the integrated fuse (5) to the cluster (4), which is built up from 36 electrodes tips (1). All these parts have the same electrical potential, in this case negative (-). The electrode surround (3) has a positive potential (+), as shown in Fig. 2. In order to highlight the non-uniform electric field, arrowed lines running from (+) to (-) indicate the field lines. This inhomogenity of the electric field is very strong, especially in close proximity to - only a few µm away - the top dielectric layer (8). The shape of the non-uniform electric field is created especially by the use of the electrode tips (1). The density of the field lines is higher close to the electrode tip (1) than in the area near the electrode surround (3). Although the area of the electrode surround (3) is about 10 times that of the area of the electrode tip, and for this reason the probability of a defective top dielectric layer (8) appears higher, in this embodiment the integrated fuse (5) is electrically connected in series with the electrode tip (1). In another embodiment the fuse (5) could also be electrically connected in series with the electrode surround (3). Even a few 10 µm apart from the surface (8a)of the Transfer-ESC, which is in direct contact with a clamped wafer (12) (Fig.6), the field lines are nearly parallel to the surface and are nearly homogeneous. This is why the effect that a dielectric object, i.e. the process-wafer (12), can be electrostatically clamped by immersing the object in a non-uniform electric field, where the non-uniform electric field produces a force which tends to pull the dielectric object into the region of the highest electric field, is only effective in a close proximity to the surface (8a)

Fig. 6 shows a more general cross-sectional overview than Fig. 5, with the elements described above, but also a base material (11) of the Transfer-ESC and the process wafer (12) to be clamped thereon. The base material (11) of a Transfer-ESC is a semiconductor wafer itself, preferably a silicon wafer. External contacts (13) for charging and discharging of the electrodes are typically located on the underside of the Transfer-ESC, as described in DE 102004041049 A1 or DE 102004030723 A1. For the additional storage of energy (current), capacitors (9) are incorporated in the base material (11) and arranged perpendicularly to the surface (8a). The capacitors (9) can be created by deep-trench techniques and enable a longer clamping time of the Transfer-ESC by supplying extra energy to the electrodes. Details of the connections of the electrodes and the capacitors (9) do not need to be shown here, because they are well known from IC manufacturing design and processing. The use of silicon wafers gives an opportunity to integrate common semiconductor-components, such as measurement or control units, processors or data storage units, because the clamping means - electrode cells (10), bus system (7) and integrated fuses (5) - required for the Transfer-ESC are located in layers on top of the base material (11). Active and passive components such as transistors, diodes and resistors are preferably integrated in the base material (11). However, the application temperature of such semiconductor components is typically limited to lower temperatures (< 120 degree Celsius). The current and voltage supply of these active and passive components is self-sufficient, using self-sufficient capacitors (9), batteries or accumulators. This self-sufficient power supply is not coupled, or is coupled only for measurement or control purposes, to the electrodes of the Transfer-ESC. These dedicated capacitors (9) or accumulators are charged using separate contacts (14) of the Transfer-ESC. Integrated active

and passive components can be designed to store relevant process parameters such as time, temperature or process flow during the manufacturing of the clamped thin wafer (12). Parameters can be read out using special data ports, which also can be used for programming. The interface for the data ports is not shown in detail here. By using an integrated control unit, it is possible to switch on or off electrodes of the Transfer-ESC. High-voltage DMOS transistors, which can be completely dielectrically insulated, or other appropriate types of bipolar or MOS transistors, work as solid state switches and can be triggered using the bus system (7), driven by an integrated control unit. An application for this kind of controlled switching of electrodes is the pick and placing of chips. Electrodes can be programmed to be "on" or "off", which can influence and regulate the clamping force, for certain areas of the Transfer-ESC, for the clamping process wafer (12). Switching off electrodes in the centre of the Transfer-ESC will relatively increase the force at the edge. Combined with the clamping voltage of the Transfer-ESC, the clamping forces can be varied, so that modified forces for concavely and convexly bowed wafers (12) can be created. An example for application of this variation is photolithography. The flatness of a clamped process wafer (12) has a very important influence on the resolution of critical dimensions. A very high number of electrodes is needed to compensate for local imperfections in the flatness of a process wafer (12). In combination with a flatness measurement tool and a feedback of the measurement results to a control unit of the Transfer-ESC, a closed loop can be created to measure, change and control the flatness of a chucked process wafer (12).

Transfer-ESCs produced using a thick-film technology are not able to achieve such a flatness. Printing and sintering processes generate microscopic peaks and valleys on the

top dielectric layer (8), which are each in the range of about 3 to 30 µm in height. This causes an additional gap between the flat wafer (12) and the surface of the Transfer-ESC (8a). Thus, the effective thickness of the top dielectric layer (8) will be increased, but with an increased thickness of the dielectric layer the clamping force reduces drastically. The Transfer-ESC with wafer as base material (11) is as flat as a production wafer (12) and for this reason they are the best suited for this application. This flatness is especially needed to generate the extra force component of a non-uniform electric field, which needs a proximity of a few micrometres of the process wafer (12) and the surface (8a).

The advantage of the described embodiment of the invention is that a Transfer-ESC with a high number of electrode cells, as well as further integrated semiconductor components, can be produced on a base wafer made from silicon by common processes and technologies of the IC industry. The use of electrode tips makes it possible to generate a non-uniform electric field, which effectively clamps wafers in close proximity. The use of very pure materials and sophisticated processes enables construction of nearly defect-free dielectric layers with a very flat surface. Microscopic imperfections such as a rough surface or particles can be reduced or avoided by using IC manufacturing technologies and environments. The integration of fuses, which enables retention of the functionality of electrodes if a defect destroys some electrode cells, is also an important advantage. In this way a very robust, highly effective, transportable electrostatic chuck, suitable for temperatures above 300 degrees Celsius, for thin wafer clamping can be manufactured, the chuck itself being made from a semiconductor wafer. Using a silicon wafer as a base material (or other suitable materials to integrate semiconductor components) to produce a Transfer-ESC, provides the opportunity

to integrate other semiconductor components such as measurement or control units, processors or data storage units within a Transfer-ESC. Single electrodes can be switched "on" or "off" by using solid state switches. The use of the same material for the wafer and the Transfer-ESC reduces or even eliminates mechanical stress, because the thermal expansion coefficient is the same.

Claims

1. A Mobile, transportable electrostatic chuck with a surface (8a) for electrostatic clamping thereon of a thin process wafer (12) by application of a clamping voltage without permanent connection to an external power supply unit, the chuck serving for transportation or other process steps and the size and thickness of the chuck and a thin process wafer clamped thereon being similar to the size, thickness and shape to a standard wafer, wherein the chuck comprises a semiconductor base material (11) with electrodes thereon for generating a non-uniform electric field, the electrodes comprising a modular formation of individual bipolar electrode cells (10) which each comprises an inner electrode tip (1), a lateral insulator layer (2), an outer electrode (3) surround surrounding the inner electrode tip and a top dielectric layer (8) and which are combined into clusters (4).

2. A chuck as claimed in claim 1, wherein each cell (10) has a length and a width each of at most 5 microns.

3. A chuck as claimed in claim 1, wherein each cluster (4) comprises 4 to 100,000 of the cells (10).

4. A chuck as claimed in claim 1, wherein each electrode comprises a plurality of clusters (4).

5. A chuck as claimed in claim 4, wherein each cluster (4) is linked to at least one integrated fuse (5).

6. A chuck according to claim 1, comprising integrated semiconductor components incorporated in the semiconductor base material (11).

7. A chuck as claimed in claim 6, wherein the components comprise measurement units, control units, processor or data storage units.

8. A chuck as claimed in claim 6 or claim 7, wherein the components comprise active and passive components self-sufficiently supplied with energy by capacitors (9), batteries or accumulators.

9. A chuck as claimed in claim 1, comprising solid state switches incorporated in the semiconductor base material (11) and operable to switch the electrodes on and off.

10. A chuck as claimed in claim 9, wherein the switches are high-voltage DMOS transistors.