ABSTRACT

DUAL Si-Ge POLYSILICON GATE WITH DIFFERENT Ge CONCENTRATIONS FOR CMOS DEVICE OPTIMIZATION

A method for forming a dual Si-Ge poly-gates having different Ge concentrations is described. An NMOS active area and a PMOS active area are provided on a semiconductor substrate separated by an isolation region. A gate oxide layer is grown overlying the semiconductor substrate in each of the active areas. A polycrystalline silicon-germanium (Si-Ge) layer is deposited overlying the gate oxide layer wherein the polycrystalline Si-Ge layer has a first Ge concentration. The NMOS active area is blocked while the PMOS active area is exposed. Successive cycles of Ge plasma doping and laser annealing into the PMOS active area are performed to achieve a second Ge concentration higher than the first Ge concentration. The polycrystalline Si-Ge layer is patterned to form a gate in each of the active areas wherein the gate in the PMOS active area has a higher Ge concentration than the gate in the NMOS active area to complete formation of dual Si-Ge polysilicon gates with different Ge concentrations in the fabrication of an integrated circuit device.

FIGURE 7