CLAIMS

~~What is claimed is:~~

1. A voltage regulation circuit, comprising:

an oscillator, connected to a power supply circuit, and configured to generate a first clock signal based on an output voltage of the power supply circuit, wherein the output voltage of the power supply circuit is used to supply power to a logic circuit, and wherein a process corner type of the oscillator is the same as a process corner type of the logic circuit; and

a regulation circuit, connected to the power supply circuit and the oscillator, and ~~wherein the oscillator is configured to connect to a power supply circuit, and generate a first clock signal based on an output voltage of the power supply circuit, wherein the output voltage of the power supply circuit is used to supply power to a logic circuit, and a process corner type of the oscillator is the same as a process corner type of the logic circuit; and~~

~~the regulation circuit is~~ configured to control~~,~~ ~~based on the first clock signal,~~ the output voltage of the power supply circuit based on the first clock signal ~~to regulate the output voltage~~.

2. The voltage regulation circuit ~~according to~~of claim 1, wherein the oscillator comprises:

a first path, ~~and~~ wherein a delay of the first path is positively correlated with a delay of a second path of the logic circuit; and

the oscillator is configured to:

generate the first clock signal through the first path based on the output voltage of the power supply circuit.

3. The voltage regulation circuit ~~according to~~of claim 2, wherein ~~the delay of the first path is linearly positively correlated with the delay of the second path, and~~ the second path is a logical path with a critical timing margin in the logic circuit.

4. The voltage regulation circuit ~~according to~~of claim 2 or 3, wherein the first path comprises a plurality of serially-connected first gate circuits~~, wherein the plurality of serially-connected first gate circuits are configured to make the delay of the first path linearly positively correlated with the delay of the second path~~.

5. The voltage regulation circuit of claim 4, wherein each of the first gate circuits comprises an inverter.

6. The voltage regulation circuit of any one of claims 2 to 5, wherein the delay of the first

path is linearly positively correlated with the delay of the second path.

7. The voltage regulation circuit of claim 6, wherein the plurality of serially-connected first gate circuits are configured to:

make the delay of the first path linearly positively correlated with the delay of the second path.

~~5~~8. The voltage regulation circuit ~~according to~~of any one of claims ~~4~~4 to 7, wherein each first gate circuit in the first path corresponds to at least one second gate circuit in the second path, wherein a function type of the first gate circuit is the same as a function type of the corresponding at least one second gate circuit, and wherein a threshold voltage type of the first gate circuit is the same as a threshold voltage type of the corresponding at least one second gate circuit.

~~6~~9. The voltage regulation circuit ~~according to~~of claim ~~5~~8, wherein the threshold voltage type of the first gate circuit is any one of the following threshold voltage types:

an ultra-high threshold voltage (uhvt), a high threshold voltage (hvt), a standard threshold voltage (svt), a low threshold voltage (lvt), or an ultra-low threshold voltage (ulvt).

~~7~~10. The voltage regulation circuit ~~according to~~of any one of claims 4 to ~~6~~9, wherein the oscillator is further configured to configure ~~some or all of~~ a plurality of gate circuits in the oscillator as the plurality of first gate circuits in the first path based on received configuration information.

~~8~~11. The voltage regulation circuit ~~according to~~of claim ~~7~~10, wherein the plurality of gate circuits form a first series structure, the first series structure comprises a plurality of delay circuits, wherein each delay circuit comprises one or more gate circuits, an input signal and an output signal of each delay circuit have a same phase, and the oscillator further comprises:

a first selector, wherein an output end of each delay circuit is connected to a data input end of the first selector, the first selector is configured to:

output a first intermediate signal based on received first configuration information, wherein the first configuration information indicates a target delay circuit in the plurality of delay circuits, and the first intermediate signal is an output signal of the target delay circuit; and

a supplementary inverter~~;~~, wherein

~~the first series structure comprises a plurality of delay circuits, each delay circuit comprises one or more gate circuits, an input signal and an output signal of each delay circuit have a same phase, an output end of each delay circuit is connected to a data input end of the first selector,~~ an

input end of the first series structure is connected to an output end of the supplementary inverter, ~~and~~ an output end of the first selector is connected to an input end of the supplementary inverter, gate circuits between the input end of the first series structure and an output end of the target delay circuit are the plurality of first gate circuits, and wherein the supplementary inverter is configured to:

receive the first intermediate signal; and

output the first clock signal based on the first intermediate signal~~;~~

~~the first selector is configured to output a first intermediate signal based on received first configuration information, wherein the first configuration information indicates a target delay circuit in the plurality of delay circuits, the first intermediate signal is an output signal of the target delay circuit, and gate circuits between the input end of the first series structure and an output end of the target delay circuit are the plurality of first gate circuits; and~~

~~the supplementary inverter is configured to receive the first intermediate signal, and output the first clock signal based on the first intermediate signal~~.

~~9~~12. The voltage regulation circuit ~~according to~~of claim ~~7~~10, wherein ~~one~~ a first part of the plurality of gate circuits forms a second series structure, wherein the second series structure comprises a plurality of low-load delay circuits, each low-load delay circuit comprises one or more gate circuits, an input signal and an output signal of each low-load delay circuit have a same phase;

wherein ~~the other~~a second part of the plurality of gate circuits forms a third series structure, wherein the third series structure comprises a plurality of high-load delay circuits, each high-load delay circuit comprises one or more gate circuits, an input signal and an output signal of each high-load delay circuit have a same phase;

and wherein the oscillator further comprises:

a second selector, wherein an output end of each low-load delay circuit is connected to a data input end of the second selector, and an input end of the third series structure is connected to the second selector, and wherein the second selector is configured to:

output a second intermediate signal based on received second configuration information, wherein the second configuration information indicates a target low-load delay circuit in the plurality of low-load delay circuits, the second intermediate signal is an output signal of the target low-load delay circuit, and gate circuits between the input end of the second series structure and an output end of the target low-load delay circuit are the first part of the plurality of first delay

circuits,;

a third selector, wherein an output end of each high-load delay circuit is connected to a data input end of the third selector, and wherein the third selector is configured to output a third intermediate signal based on received third configuration information, wherein the third configuration information indicates a target high-load delay circuit in the plurality of high-load delay circuits, the third intermediate signal is an output signal of the target high-load delay circuit, and gate circuits between the input end of the third series structure and an output end of the target high-load delay circuit are the second part of the plurality of first delay circuits,; and

a supplementary inverter, wherein an input end of the second series structure is connected to an output end of the supplementary inverter;

~~the second series structure comprises a plurality of low-load delay circuits, each low-load delay circuit comprises one or more gate circuits, an input signal and an output signal of each low-load delay circuit have a same phase, an output end of each low-load delay circuit is connected to a data input end of the second selector, and an input end of the second series structure is connected to an output end of the supplementary inverter;~~

~~the third series structure comprises a plurality of high-load delay circuits, each high-load delay circuit comprises one or more gate circuits, an input signal and an output signal of each high-load delay circuit have a same phase, an output end of each high-load delay circuit is connected to a data input end of the third selector, and an input end of the third series structure is connected to the second selector;~~

~~the second selector is configured to output a second intermediate signal based on received second configuration information, wherein the second configuration information indicates a target low-load delay circuit in the plurality of low-load delay circuits, the second intermediate signal is an output signal of the target low-load delay circuit, and gate circuits between the input end of the second series structure and an output end of the target low-load delay circuit are the one part of the plurality of first delay circuits;~~

~~the third selector is configured to output a third intermediate signal based on received third configuration information, wherein the third configuration information indicates a target high-load delay circuit in the plurality of high-load delay circuits, the third intermediate signal is an output signal of the target high-load delay circuit, and gate circuits between the input end of the third series structure and an output end of the target high-load delay circuit are the other part of the~~

~~plurality of first delay circuits; and,~~

the wherein supplementary inverter is configured to receive the third intermediate signal, and output the first clock signal based on the third intermediate signal.

~~10. The voltage regulation circuit according to claim 9, wherein the high-load delay circuit further comprises at least one load routing.~~

~~11~~13. The voltage regulation circuit ~~according to~~of any one of claims 1 to ~~10~~12, wherein the regulation circuit comprises:

a frequency divider, separately connected to the oscillator and a frequency comparator, wherein the frequency divider is configured to perform frequency division on the first clock signal based on a frequency division multiple to obtain a second clock signal~~,~~;

~~a~~ the frequency comparator, connected to a controller, wherein the frequency comparator is configured to receive a reference clock signal, and output a frequency difference signal based on the second clock signal and the reference clock signal, wherein the frequency difference signal indicates a relative frequency value relationship between the second clock signal and the reference clock signal~~,~~; and

~~a~~ the controller~~, the frequency divider is separately connected to the oscillator and the frequency comparator, the frequency comparator is connected to the controller, and the controller is configured to~~ connected to the power supply circuit~~;~~

~~the frequency divider is configured to perform frequency division on the first clock signal based on a frequency division multiple to obtain a second clock signal;~~

~~the frequency comparator is configured to receive a reference clock signal, and output a frequency difference signal based on the second clock signal and the reference clock signal, wherein the frequency difference signal indicates a relative frequency value relationship between the second clock signal and the reference clock signal; and,~~ wherein

the controller is configured to control~~, based on the frequency difference signal,~~ the output voltage of the power supply circuit based on the frequency difference signal ~~to regulate the output voltage~~.

~~12~~14. The voltage regulation circuit ~~according to~~of claim ~~11~~13, wherein a quotient value obtained through division of a frequency of a first clock signal output by an oscillator of a typical typical process corner TT corner type by a frequency of the reference clock signal is the frequency division multiple.

~~13~~15. The voltage regulation circuit according to claim ~~11~~ 13 or ~~12~~14, wherein the controller is configured to:

~~when the frequency difference signal indicates that a frequency of the second clock signal is greater than the frequency of the reference clock signal,~~ control the power supply circuit to decrease the output voltage of the power supply circuit, wherein the frequency difference signal indicates that a frequency of the second clock signal is greater than the frequency of the reference clock signal; ~~and/~~or

~~when the frequency difference signal indicates that the frequency of the second clock signal is less than the frequency of the reference clock signal,~~ control the power supply circuit to increase the output voltage of the power supply circuit, wherein the frequency difference signal indicates that the frequency of the second clock signal is less than the frequency of the reference clock signa,.

~~14. The voltage regulation circuit according to any one of claims 11 to 13, wherein the regulation circuit further comprises a low-pass filter, an input end of the low-pass filter is connected to the frequency comparator, and an output end of the low-pass filter is connected to the controller; and~~

~~the low-pass filter is configured to filter the frequency difference signal, and output a filtered frequency difference signal to the controller.~~

~~15~~16. An operation system, comprising:

a power supply circuit~~,~~;

a logic circuit~~,~~; and

~~the~~ a voltage regulation circuit according to any one of claims 1 to ~~14~~15.

~~16~~17. The operation system according to claim ~~15~~16, wherein the operation system further comprises a phase-locked loop PLL, and the PLL is connected to the logic circuit; and

the PLL is configured to receive a reference clock signal, and provide a third clock signal for the logic circuit based on the reference clock signal.

~~17~~18. The operation system according to claim ~~15~~ 16 or ~~16~~17, wherein the power supply circuit comprises a first power supply and a second power supply;

the first power supply is configured to provide a first output voltage for the voltage regulation circuit;

the second power supply is configured to provide a second output voltage for the logic circuit; and

the regulation circuit is separately connected to the first power supply and the second power supply, and the regulation circuit is specifically configured to:

separately control, based on the first clock signal, the first power supply to regulate the first output voltage, and control the second power supply to regulate the second output voltage, wherein the first output voltage keeps consistent with the second output voltage.

~~18~~19. An integrated module, comprising a logic circuit and the voltage regulation circuit according to any one of claims 1 to ~~14~~15.

~~19~~20. An integrated circuit, comprising at least one operation system according to any one of claims ~~15~~ 16 to ~~17~~ 18 and a system bus, wherein the system bus is connected to the at least one operation system; and

the system bus is configured to separately provide at least one corresponding reference clock signal for the at least one operation system.

~~20~~21. A voltage regulation method, comprising:

generating a first clock signal ~~by using~~using an oscillator based on an output voltage of a power supply circuit, wherein a process corner type of the oscillator is the same as a process corner type of a logic circuit, and the output voltage of the power supply circuit is used to supply power to the logic circuit; and

controlling, based on the first clock signal, the output voltage of the power supply circuit ~~to regulate the output voltage~~.

~~21~~22. The method according to claim ~~20~~21, wherein the controlling, based on the first clock signal, the power supply circuit to regulate the output voltage comprises:

performing frequency division on the first clock signal based on a frequency division multiple to obtain a second clock signal; and

controlling, based on a relative frequency value relationship between the second clock signal and a reference clock signal, the power supply circuit to regulate the output voltage.

~~22~~23. The voltage regulation method according to claim ~~21~~22, wherein a quotient value obtained through division of a frequency of a first clock signal output by an oscillator of a typical typical process corner TT corner type by a frequency of the reference clock signal is the frequency division multiple.

~~23~~24. The method according to claim ~~21~~ 22 or ~~22~~22, wherein the controlling, based on a relative frequency value relationship between the second clock signal and a reference clock signal,

the power supply circuit to regulate the output voltage comprises:

when a frequency of the second clock signal is greater than the frequency of the reference clock signal, control the power supply circuit to decrease the output voltage; and/or

when the frequency of the second clock signal is less than the frequency of the reference clock signal, control the power supply circuit to increase the output voltage.