

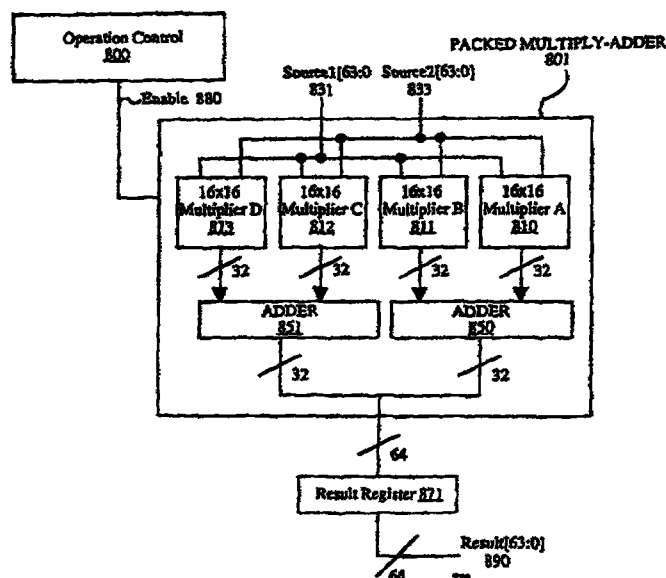


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(54) Title: **AN APPARATUS FOR PERFORMING MULTIPLY-ADD OPERATIONS ON PACKED DATA**

(57) Abstract

A processor having a first and second storage having a first and second packed data, respectively. Each packed data includes a first, second, third, and fourth data element. A multiply-add circuit is coupled to the first and second storage areas. The multiply-add circuit includes a first (810), second (811), third (812), and fourth multiplier (813), wherein each of the multipliers receives a corresponding set of said data elements. The multiply-add circuit further includes a first adder (850) coupled to the first and second multipliers (810, 811), and second adder (851) coupled to the third and fourth multipliers (812, 813). A third storage area (871) is coupled to the adders (850, 851). The third storage area (871) includes a first and second field for saving output of the first and second adders (850, 851), respectively, as first and second data elements of a third packed data.