

PATENT SPECIFICATION

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(54) LOGIC CIRCUIT

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED of Abacus House, 33 Gutter Lane, London, E.C.2., a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to logic gate circuits.

An Integrated Injection Logic (I²L) circuit comprises a logic gate circuit, comprising a first transistor, a second transistor whose base-emitter path is connected in parallel with the collector-emitter path of the first transistor, and a current source arrangement for biasing said transistors, which arrangement is coupled to the emitters of said transistors and is connected to the base of each said transistor.

Large-scale integration is possible with such gate circuits, which can be integrated very simply and compactly and which have a low dissipation per gate circuit without excessively impairing its speed. The known I²L circuits consist of transistors which are powered through injection of minority charge carriers. Injection is effected from an injection rail which forms a PN-injection with the emitter regions. The switching speed of the circuit can be varied within wide limits by selection of the current level.

A logic gate circuit of this type is, for example, known from "Philips Technisch Tijdschrift" 33, No. 3, 1973, page 84, Figure 6. This circuit consists of a first group of two transistors whose collector-emitter paths are connected in parallel, the logic input signals being applied to the base electrodes of these transistors, a second group of two transistors whose base-emitter paths are connected in parallel with the collector-emitter paths of the transistors of the first group, and a third group of two transistors whose base-emitter paths are connected in parallel. The collector of one of the transistors of the third group is connected to the collector of one transistor of the second

group. The current source arrangement is connected to the bases of all six transistors. Each transistor in the circuit provides the logic inversion of its base signal, while the interconnections of the collectors where present provide a "wired-and" function of the collector signals. As a result, the transistors with interconnected collectors may be regarded as NOR-gates. As is evident from Figure 6 of the cited article, the transistors of the second group may take the form of a multi-collector single transistor, as may the transistors of the third group; this is shown in Figure 7 on page 85 of said article.

When considering the switching speeds of I²L circuits a distinction must be made between situations of low and high current level. In the former situations only stray wiring capacitances and depletion capacitances have to be charged and discharged; in the latter situations charge storage in the transistors plays a more important part. As is known, each transistor collector in an I²L circuit has to be capable of taking up one base current. As a result of this, the effective current gain factor β of each transistor must be greater than 1. (In this respect it should be noted that the effective current gain factor in I²L technology is the β of the transistor (normally NPN) during the operating condition thereof in the presence of the current source arrangement (normally comprising a transistor of complementary type). This factor β can for example be measured as the ratio between the collector current and the base current of the NPN-transistor when the emitter-base junction of the complementary (PNP) transistor is short-circuited, so that the emitter of the last-mentioned transistor is coupled to the emitter of the NPN-transistor.) However, a high β means that the NPN transistor will be strongly bottomed (saturated) in the "ON" state, so that minority charge carriers become stored therein. This means that the charge storage in the transistor will determine the switching speed of this transistor. A low β would therefore be desirable, but

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too low a β is objectionable in its turn for reasons of susceptibility to interference or noise. Moreover, from the point of view of yield it is difficult to control a manufacturing process in such a way that transistors with, for example, $\beta=2$ can be realized. In addition, the factor β is geometry-dependent, so that a desired value of $\beta=2$ is tied to a specific geometry. A multi-collector transistor with for example two collectors almost automatically has a different current gain factor per collector than a multi-collector transistor with for example four collectors. It is far easier to realise a manufacturing process in which the current gain factors of the integrated transistors lie in a range of say $20 < \beta < 100$. However, as previously stated, this adversely affects the switching speeds of the integrated transistors.

The invention provides a logic gate circuit, comprising a first transistor, a second transistor whose base-emitter path is connected in parallel with the collector-emitter path of the first transistor, a current source arrangement for biasing said transistors, which arrangement is coupled to the emitters of said transistors and is connected to the base of each said transistor, and a current path in parallel with the base-emitter path of each said transistor for taking up a part of the current which is supplied by the current source arrangement for the relevant transistor when the relevant transistor is in the conductive state.

An embodiment of the invention will be described, by way of example, with reference to the accompanying diagrammatic drawings in which

Figure 1 shows the embodiment,

Figure 2 is a current diagram to explain how the embodiment of Figure 1 would operate if one component were omitted, and

Figure 3 is a current diagram to explain how the embodiment of Figure 1 actually operates.

In Figure 1a logic gate circuit of the I²L type comprises a first group E of transistors 10, 11 and 12, whose base-emitter paths are connected in parallel. The base-emitter paths of transistors 20 and 21 of a second group F are connected in parallel with the collector-emitter path of transistor 12. The bases of the transistors 10, 11 and 12 of the first group E are connected to a supply point of positive polarity via the collector-emitter path of a biasing transistor 14 of complementary type. A corresponding biasing transistor 23 is provided for the transistors of the second group F. A diode 13 is connected in parallel with the base-emitter paths of the transistors 10, 11 and 12 of the first group E. A corresponding diode 22 is provided for the transistors of the second group F. The forward direction

of the diode 13 is the same as the forward direction of the base-emitter junctions of the transistors 10, 11 and 12. The bases of the transistors 14 and 23 are connected to the emitters of the transistors 10, 11, 12, 20 and 21 via an impedance 30. This impedance serves to increase the switching speed, as is described in copending Patent Application 40778/75 (Serial No. 1532427), and is preferably formed by a resistance the value of which is such that, in operation, a potential difference of at least 30 mV and preferably more than 60 mV appears across said resistance. Of course an impedance element other than a resistance may be employed provided that the required potential difference can be obtained thereacross. For example, a Schottky diode may be employed for said purpose. As another alternative a voltage may be applied to the bases of the complementary transistors from the exterior.

To simplify the explanation of the operation of the logic circuit of Figure 1 it will be assumed that the collectors of the transistors 10 and 11 are connected to the collector of the transistor 12, this being indicated by a dashed line in Figure 1. The transistors 10, 11 and 12 will then effectively constitute a single transistor, which will be referred to as transistor 10 (11, 12) hereinafter. The collector currents of the transistors 14 and 23 will be assumed to be equal to I amperes each. When a logic signal a is applied to the base of the transistor 10

(11, 12), a logic signal $\bar{a}$ (negation of a) will appear at the collector of the transistor 10 (11, 12), and a logic signal a will appear at the collectors of the transistors 20 and 21. Assuming that $a=1$ and that positive logic is employed (which means that the condition $a=1$ corresponds to a high voltage) the transistor 10 (11, 12) will conduct. As a result, the diode 22 and the transistors 20 and 21 will not conduct. In the absence of the diode 13 the base current of the transistor 10 (11, 12) would be equal to I amperes but in fact a part of the current I supplied by the transistor 14 will flow through said diode. The base current of the transistor 10 (11, 12) will therefore be only a part pI ($p < 1$) of the current I.

Figure 2 shows a portion of the arrangement of Figure 1 in simplified form and with the diode 13 omitted. In Figure 2 the current source 14 corresponds to the PNP transistor 14 of Figure 1, the current source 23 corresponds to the PNP transistor 23 of Figure 1 and the transistor 10 (11, 12) corresponds to the composite transistor 10 (11, 12) of Figure 1.

The collector current of the transistor 10 (11, 12) will, in the absence of the diode 13, be equal to its base current, so that

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transistor 10 (11, 12) will be bottomed. The total base current $I(b)$ of the transistor 10 (11, 12) can be considered as being composed of two currents $i(1)$ and $i(2)$ respectively, as is shown in Figure 2. These two base currents result in two internal currents $\beta i(1)$ and $(1+\beta) i(1)$, owing to the forward biased emitter-base junction of the transistor 10 (11, 12) and two internal currents $\beta' i(2)$ and $(1+\beta') i(2)$, owing to the forward-biased collector-base junction of the transistor 10 (11, 12). In these formulae β is the forward current gain factor of the transistor 10 (11, 12), which is equal to the effective β , and β' is the current gain factor of the transistor 10 (11, 12) when said transistor is operated in the inverse direction. The emitter-base voltage and the collector-base voltage of the transistor 10 (11, 12) are such that the external currents are given by:

$$I(b) = I = i(1) + i(2) \quad (1)$$

$$I(e) = 2I = (1+\beta)i(1) - \beta' i(2) \quad (2)$$

$$I(c) = I = \beta i(1) - (1+\beta') i(2) \quad (3)$$

where $I(b)$ is the external base current, $I(e)$ is the external emitter current and $I(c)$ is the external collector current of the transistor 10 (11, 12). If, for example, $\beta = \beta' = 100$, then $i(1) = 0.507I$ and $i(2) = 0.493I$. The internally existing collector currents are a measure of the charge storage in the transistor. These currents are 50.7I and 49.3I in this case, which implies that the charge which is stored in the base is large. This means that the switching speed of the transistor will be correspondingly low.

Figure 3 shows the corresponding situation in which the diode 13 is included in parallel with the base-emitter path of the transistor 10 (11, 12). Most of the current I will now flow through the diode 13. The following relations are now valid:

$$I(b) = I' = i(1)' + i(2)' \quad (4)$$

$$I(e) = I + I' = (1+\beta)i(1)' - \beta' i(2)' \quad (5)$$

$$I(c) = I = \beta i(1)' - (1+\beta') i(2)' \quad (6)$$

$$I(d) = p(1+\beta)i(1)' \quad (7)$$

$$I(d) + I(b) = I \quad (8)$$

(The factor β occurs in equation (7) because it has been assumed that diode 13 is in fact a diode-connected transistor.) The factor p depends on the ratio between the diode junction area and the effective emitter area of the NPN transistor 10 (11, 12). (In this respect it should be noted that in the case of inverse operation of a transistor, as is usual with I_L , the effective emitter area equals the area of the collector zone of the transistor.) If, for example, the factor p is chosen to be $1/3$, and if $\beta = \beta' = 100$, a simple calculation reveals that $i(1)' = 0.02I$

and $i(2)' = 0.01I$. As the current $i(1)'$ is very much less than $i(1)$ and the current $i(2)'$ is very much less than $i(2)$, the internal currents which flow through the transistor 10 (11, 12) are substantially smaller than with diode 13 absent. In the present instance the oppositely directed collector currents are equal to $2I$ and I respectively, which means that the charge which is stored in the transistor will also be substantially smaller than in the situation without the diode. Thus the switching speed will increase accordingly.

In addition to increasing the switching speed of the logic circuit of Figure 1 by including the diode 13, the switching speed can be increased still further by including the resistance 30 between the base of the transistor 14 and the emitter of the transistor 10 (11, 12). When the transistor 10 (11, 12) is conductive, the collector-base junction of the transistor 14 will be less forward-biased when the resistance 30 is included than when said resistance is absent. If the voltage across the resistance is 200 to 300 mV, the storage of minority charge carriers in the base of the transistor 14 will be negligible in comparison with the storage in the base of the transistor 10 (11, 12). In the "off"-state of the transistor 10 (11, 12) the collector-base junction of the transistor 14 will have a reverse bias of 200 to 300 mV. Consequently, the switching time of the logic circuit will be determined only by the charge storage in the base of the transistor 10 (11, 12).

The circuit of Figure 1 may, for example, be integrated in a manner as described in the aforesaid copending Patent Application 40778/75 (Serial No. 1532427). Thus each group E and F of NPN transistors can be formed by a single transistor of the multi-collector type. If such a single transistor is provided with an additional collector short-circuited to its base, an emitter-base diode will effectively be formed connected in parallel with the emitter-base junction of the multi-collector transistor, i.e. the corresponding diode 13 or 22 will effectively be formed. The desired ratio p can be obtained by making the additional collector smaller than the other collectors. The complementary biasing transistor may be a lateral transistor if the circuit is constructed in integrated circuit form.

If desired, a resistance can be included in series with the diode 13 in Figure 1 in order to improve the noise margin, the input of the logic gate circuit then being constituted by the common point of said resistance and the diode.

As an alternative to the arrangement of Figure 1 in which the base-emitter paths of the transistors 10, 11 and 12 are connected in parallel, their collector-emitter paths may be connected in parallel. If this is done a

5 bias current source will have to be connected to the base of each of these transistors, and a diode similar to 13 will have to be provided across the base-emitter path of each of these transistors.

WHAT WE CLAIM IS:—

- 10 1. A logic gate circuit, comprising a first transistor, a second transistor whose base-emitter path is connected in parallel with the collector-emitter path of the first transistor, a current source arrangement for biasing said transistors, which arrangement is coupled to the emitters of said transistors and is connected to the base of each said transistor, and a current path in parallel with the base-emitter path of each said transistor for taking up a part of the current which is supplied by the current source arrangement for the relevant transistor when the relevant transistor is in the conductive state.
- 25 2. A logic gate circuit as claimed in claim 1, wherein each current path comprises a diode whose forward direction is the same as the forward direction of the base-emitter junction of the relevant transistor.
3. A logic gate circuit as claimed in claim 2, wherein the diode is constituted by a transistor whose base and collector are interconnected, the effective emitter area of said

transistor being smaller than the effective emitter area of the relevant transistor. 30

4. A logic gate circuit as claimed in claim 3, wherein the base and emitter regions of the diode-connected transistor are common to the base and emitter regions respectively of the relevant transistor. 35

5. A logic gate circuit as claimed in claim 1 or claim 2, wherein the current path includes a resistance.

6. A logic gate circuit as claimed in any preceding claim, wherein the first and second transistors are of the NPN-type and the current source arrangement comprises a lateral PNP-transistor, the base of the lateral PNP-transistor being connected to the emitters of the first and second transistors via a resistance. 40 45

7. A logic gate circuit as claimed in claim 2, wherein a resistance is included in series with the diode. 50

8. A logic gate circuit substantially as described herein with reference to Figure 1 of the drawings.

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WHAT WE CLAIM IS:—

1. A logic gate circuit, comprising a first
transistor, a second transistor whose base-
emitter path is connected in parallel with
the collector-emitter path of the first
transistor, a current source arrangement for
biasing said transistors, which arrangement
is coupled to the emitters of said transistors
and is connected to the base of each said
transistor, and a current path in parallel with
the base-emitter path of each said transistor
for taking up a part of the current which
is supplied by the current source arrangement
for the relevant transistor when the relevant
transistor is in the conductive state.

2. A logic gate circuit as claimed in claim
1, wherein each current path comprises a
diode whose forward direction is the same
as the forward direction of the base-emitter
junction of the relevant transistor.

3. A logic gate circuit as claimed in claim
2, wherein the diode is constituted by a
transistor whose base and collector are inter-
connected, the effective emitter area of said

transistor being smaller than the effective
emitter area of the relevant transistor.

4. A logic gate circuit as claimed in claim
3, wherein the base and emitter regions of
the diode-connected transistor are common
to the base and emitter regions respectively
of the relevant transistor.

5. A logic gate circuit as claimed in claim
1 or claim 2, wherein the current path
includes a resistance.

6. A logic gate circuit as claimed in any
preceding claim, wherein the first and second
transistors are of the NPN-type and the
current source arrangement comprises a
lateral PNP-transistor, the base of the lateral
PNP-transistor being connected to the
emitters of the first and second transistors via
a resistance.

7. A logic gate circuit as claimed in claim
2, wherein a resistance is included in series
with the diode.

8. A logic gate circuit substantially as
described herein with reference to Figure 1
of the drawings.

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