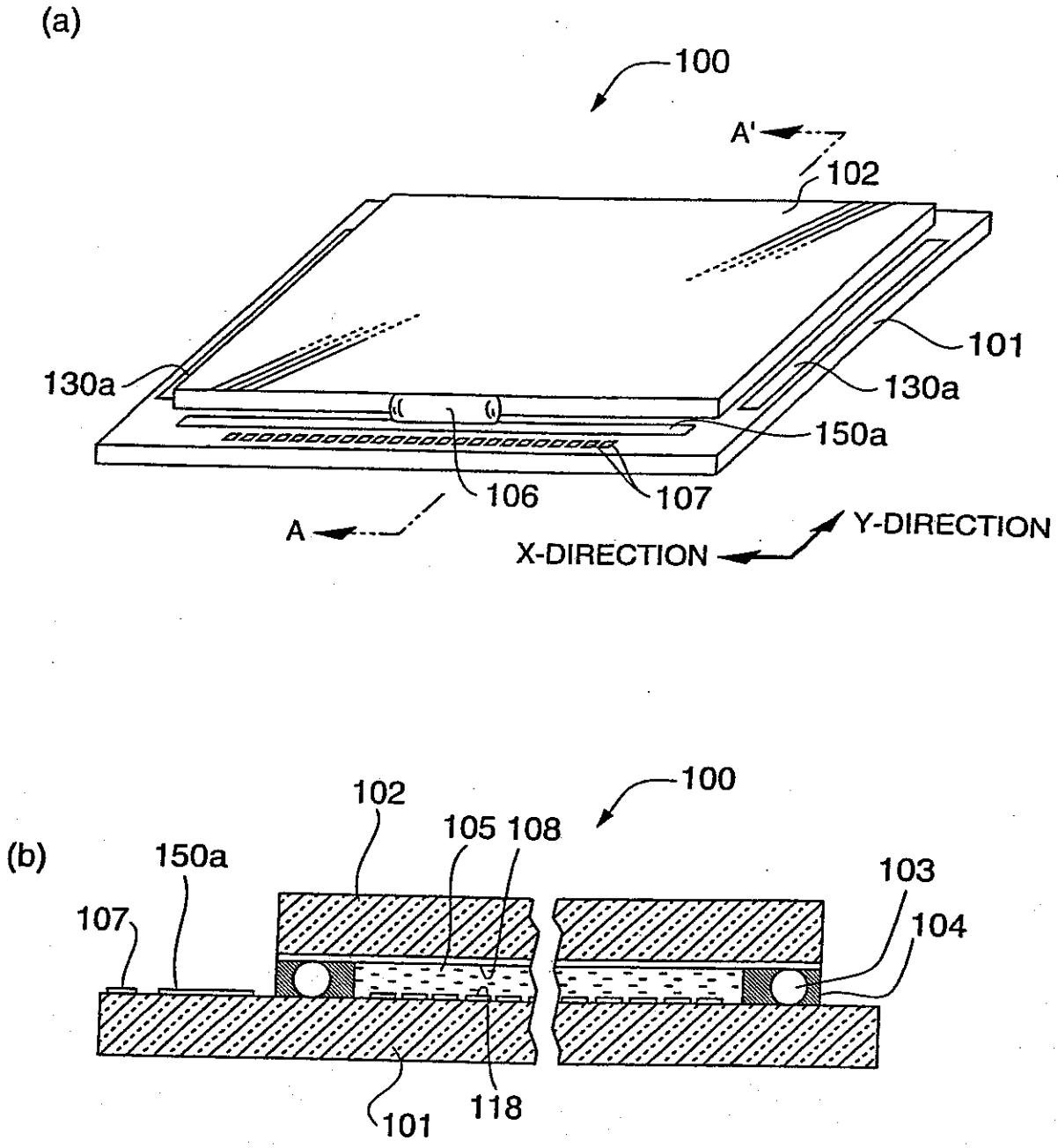

(a)
100
A'
102
101
130a
130a
150a
106
107
A
X-DIRECTION
Y-DIRECTION
(b)
102
100
105 108
150a
103
107
104
101
118

FIG. 1

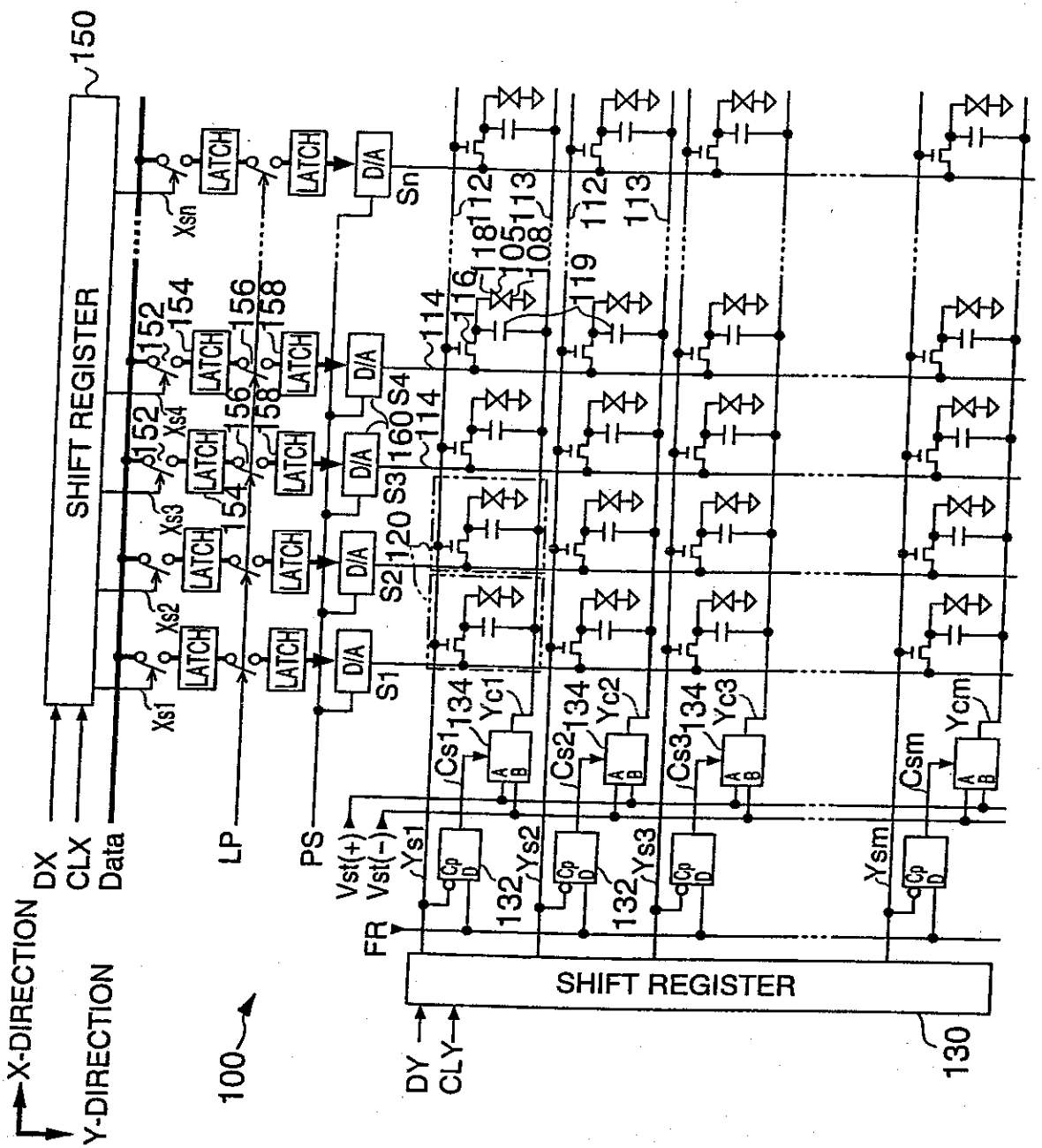

SHIFT REGISTER
150
LATCH
D/A
Xsn
Xs4
Xs3
Xs2
Xs1
Sn
S4
S3
S2
S1
152
154
156
158
160
112
113
114
116
118
119
120
105
108
134
Yc1
Yc2
Yc3
Ycm
Cs1
Cs2
Cs3
Csm
A
B
Cp
D
Ys1
Ys2
Ys3
Ysm
132
DX
CLX
Data
LP
PS
Vst(+)
Vst(−)
FR
DY
CLY
SHIFT REGISTER
130
100
X-DIRECTION
Y-DIRECTION

FIG. 2

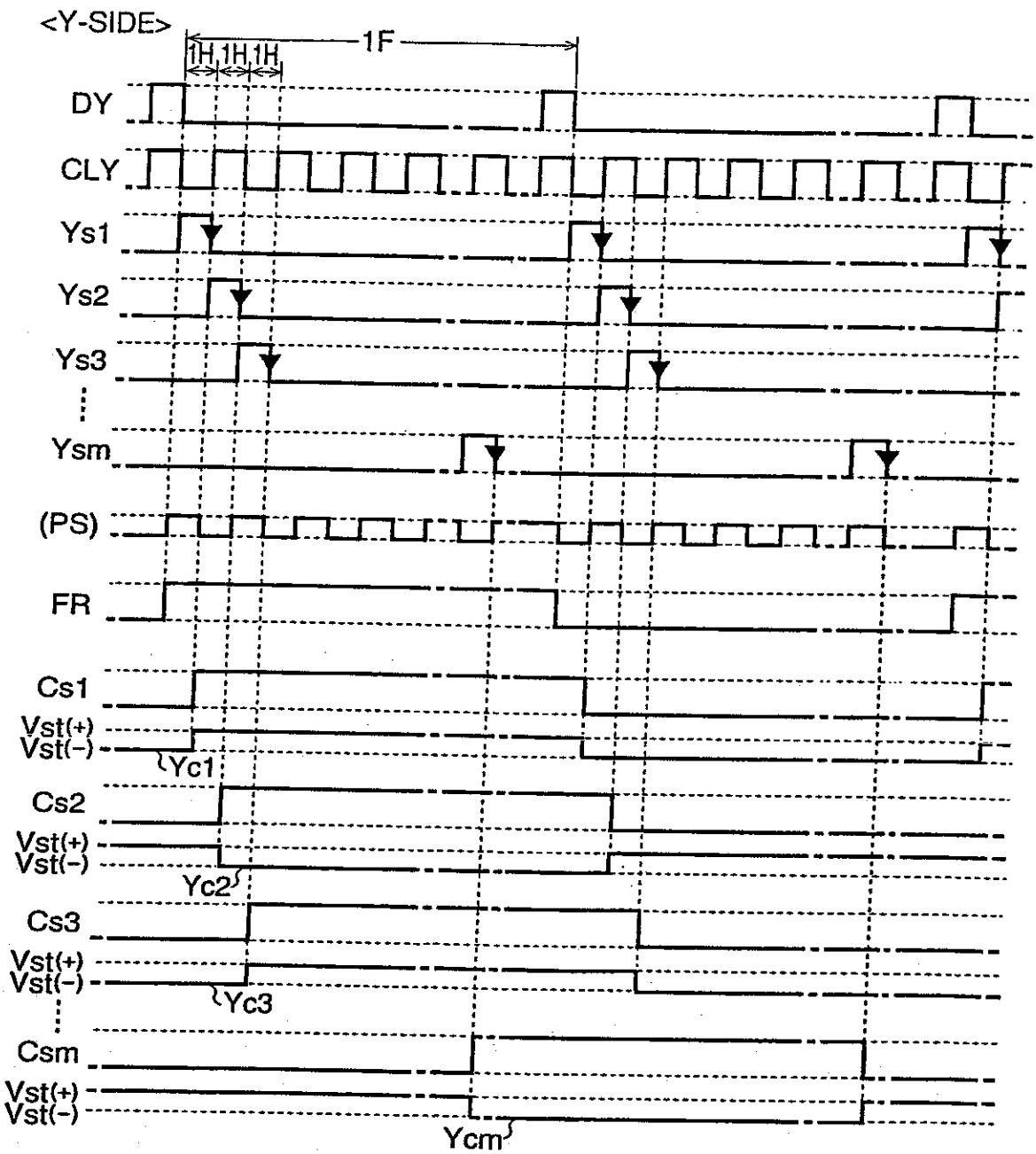
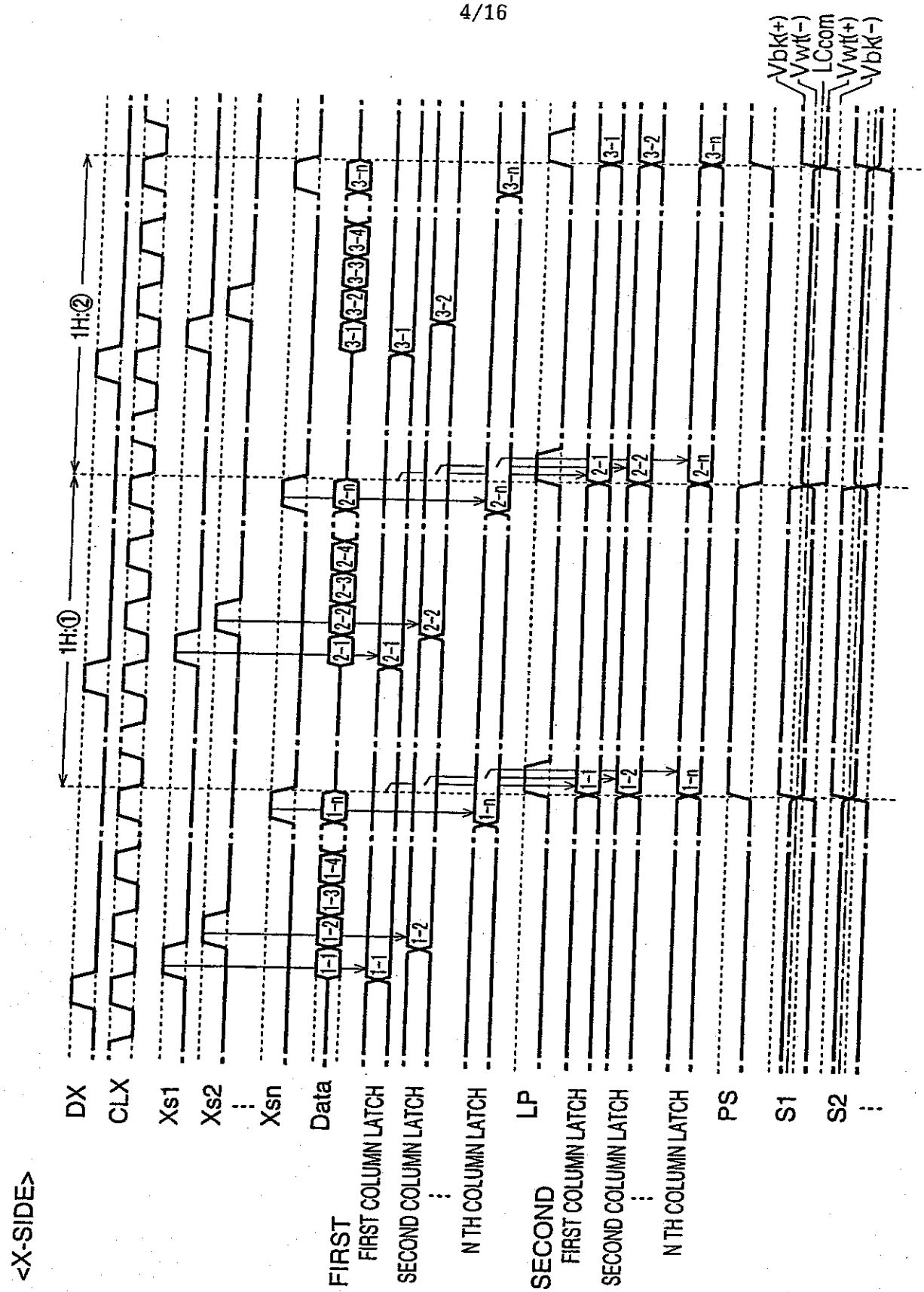

<Y-SIDE>
1H
1H
1H
1F
DY
CLY
Ys1
Ys2
Ys3
Ysm
(PS)
FR
Cs1
Vst(+)
Vst(−)
Yc1
Cs2
Vst(+)
Vst(−)
Yc2
Cs3
Vst(+)
Vst(−)
Yc3
Csm
Vst(+)
Vst(−)
Ycm

FIG. 3


<X-SIDE>
DX
CLX
Xs1
Xs2

Xsn
Data
1H:①
1H:②
FIRST
FIRST COLUMN LATCH
SECOND COLUMN LATCH

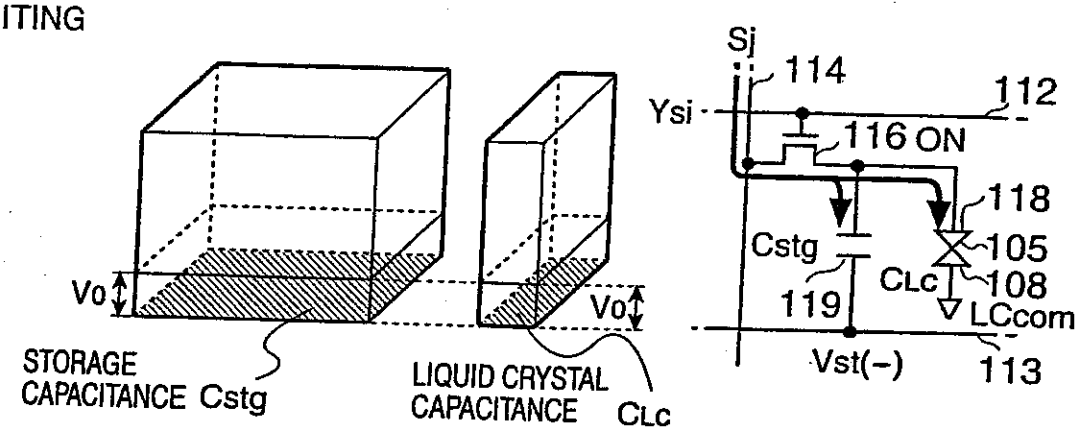
N TH COLUMN LATCH
LP
SECOND
FIRST COLUMN LATCH
SECOND COLUMN LATCH

N TH COLUMN LATCH
PS
S1
S2

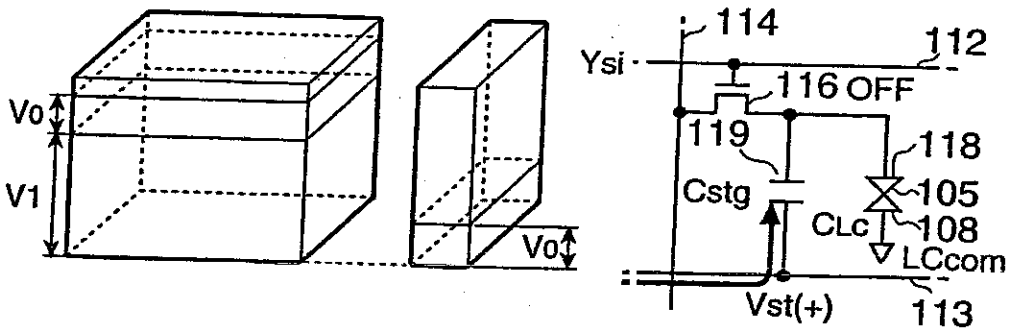
Vbk(+)
Vwt(-)
LCcom
Vwt(+)
Vbk(-)

FIG. 4

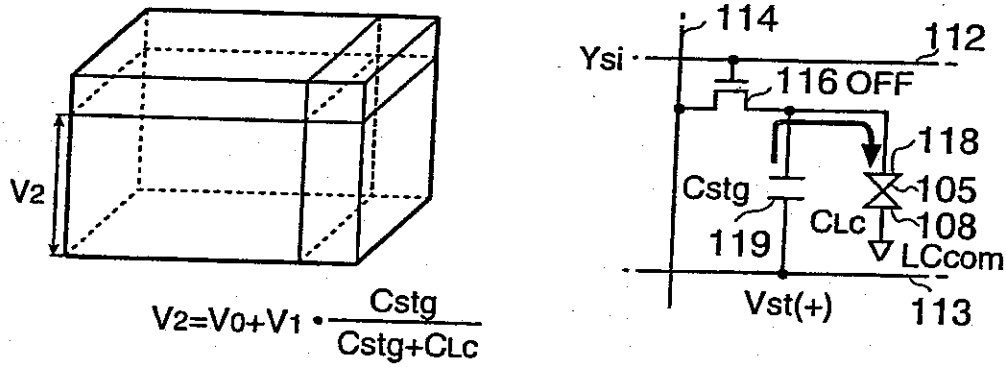
(a)WRITING



(b)VOLTAGE SHIFT OF STORAGE CAPACITANCE



(c)CHARGE REDISTRIBUTION



$$V_2 = V_0 + V_1 \cdot \frac{Cstg}{Cstg + CLc}$$

FIG. 5

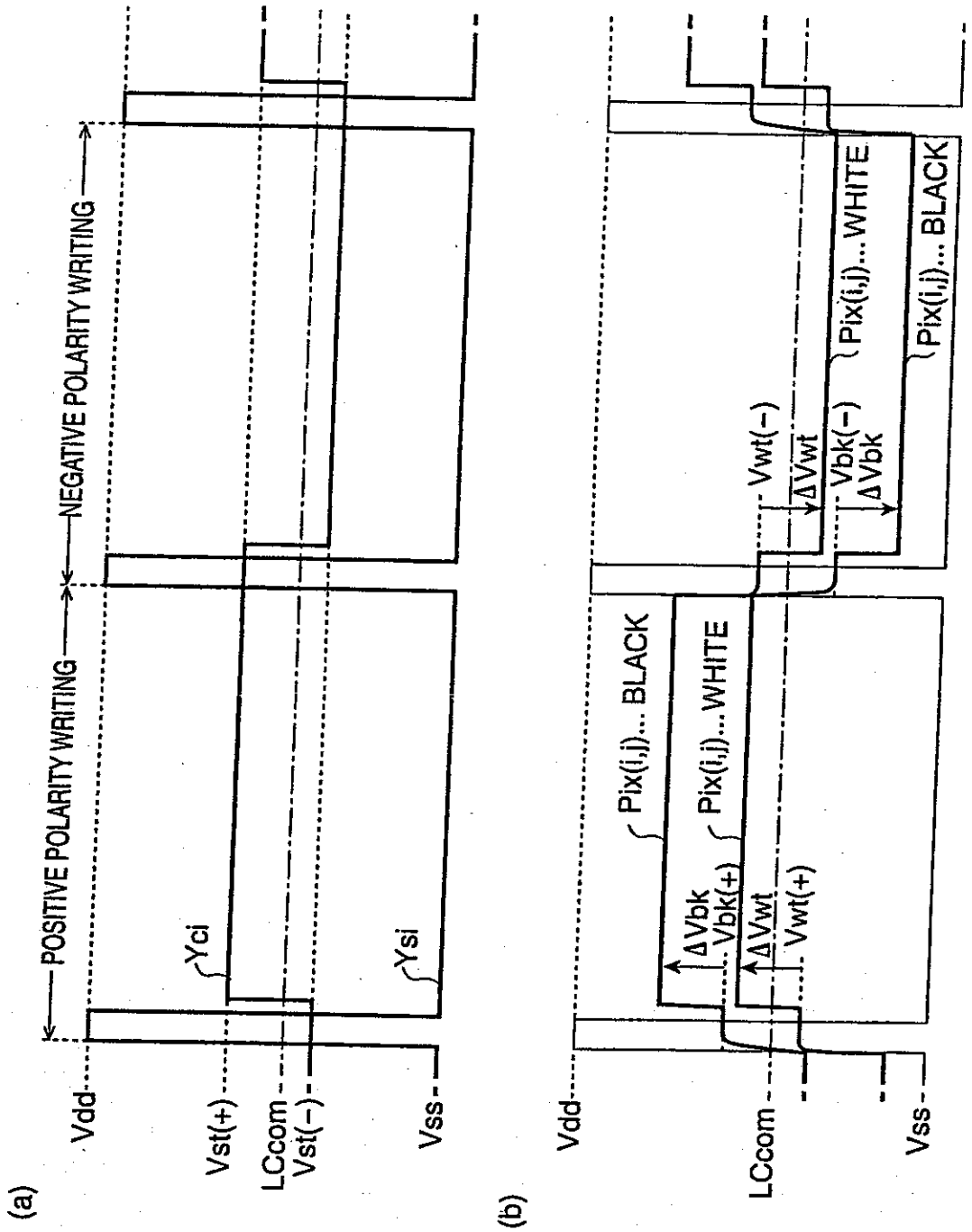

(a)
POSITIVE POLARITY WRITING
NEGATIVE POLARITY WRITING
Yci
Ysi
Vdd
Vst(+)
LCcom
Vst(−)
Vss
(b)
Pix(i,j)... BLACK
Pix(i,j)...WHITE
Pix(i,j)... WHITE
Pix(i,j)... BLACK
ΔVbk
Vbk(+)
ΔVwt
Vwt(+)
Vwt(−)
ΔVwt
Vbk(−)
ΔVbk
Vdd
LCcom
Vss

FIG. 6

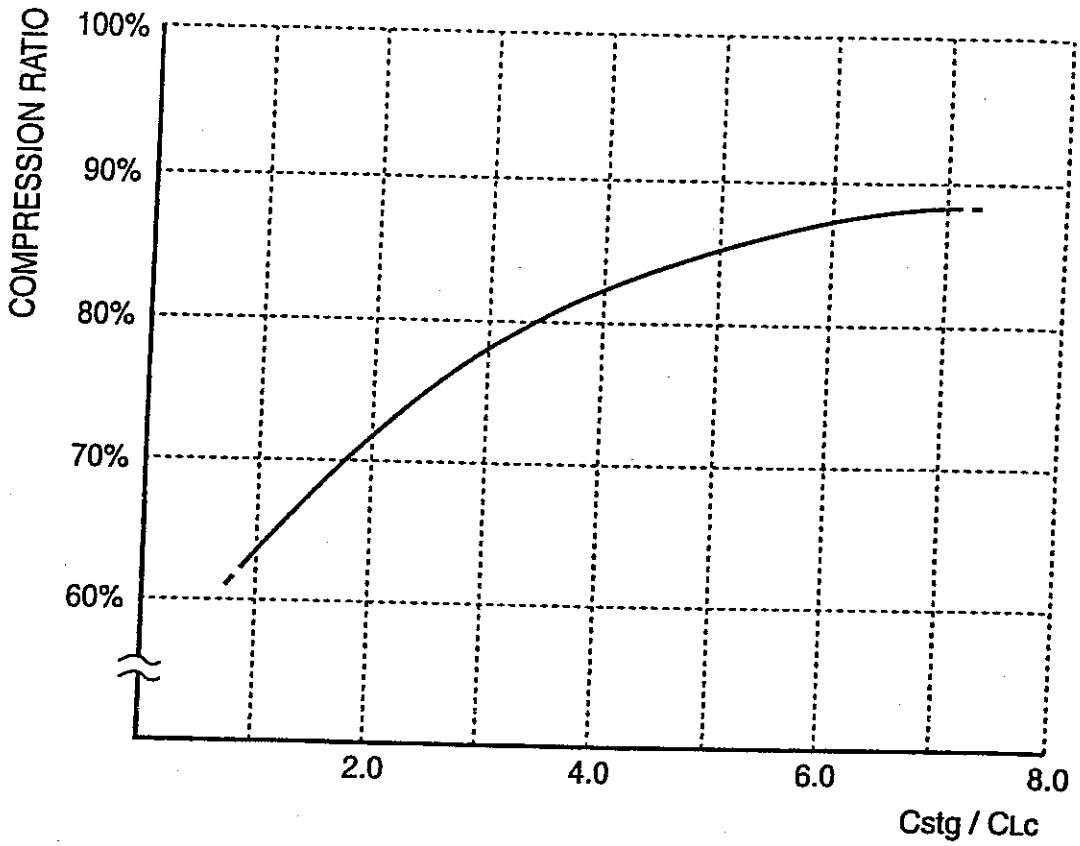


FIG. 7

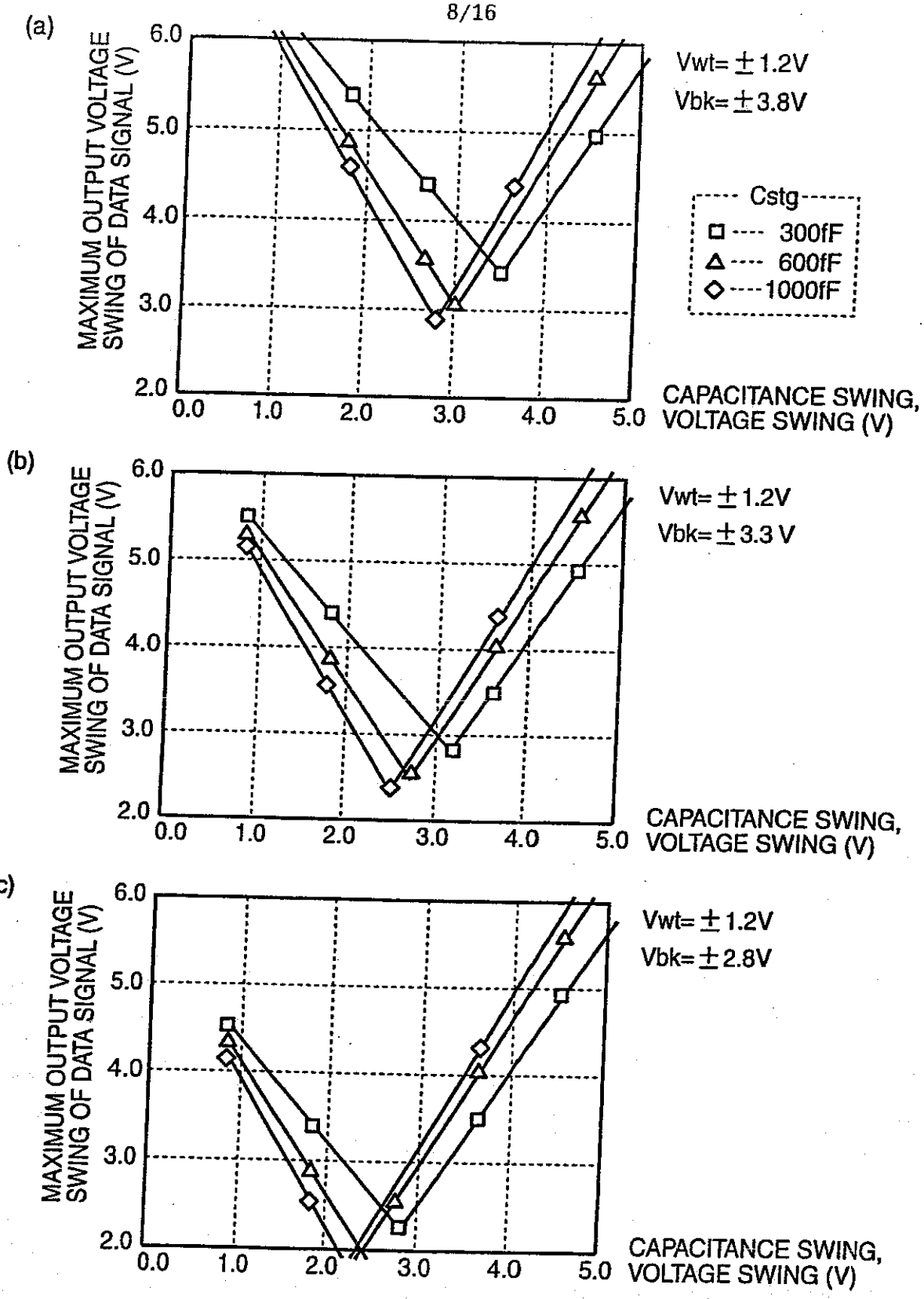

(a)
MAXIMUM OUTPUT VOLTAGE SWING OF DATA SIGNAL (V)
6.0
5.0
4.0
3.0
2.0
0.0
1.0
2.0
3.0
4.0
5.0
CAPACITANCE SWING, VOLTAGE SWING (V)
Vwt=±1.2V
Vbk=±3.8V
Cstg
300fF
600fF
1000fF
(b)
MAXIMUM OUTPUT VOLTAGE SWING OF DATA SIGNAL (V)
CAPACITANCE SWING, VOLTAGE SWING (V)
Vwt=±1.2V
Vbk=±3.3 V
(c)
MAXIMUM OUTPUT VOLTAGE SWING OF DATA SIGNAL (V)
CAPACITANCE SWING, VOLTAGE SWING (V)
Vwt=±1.2V
Vbk=±2.8V

FIG. 8

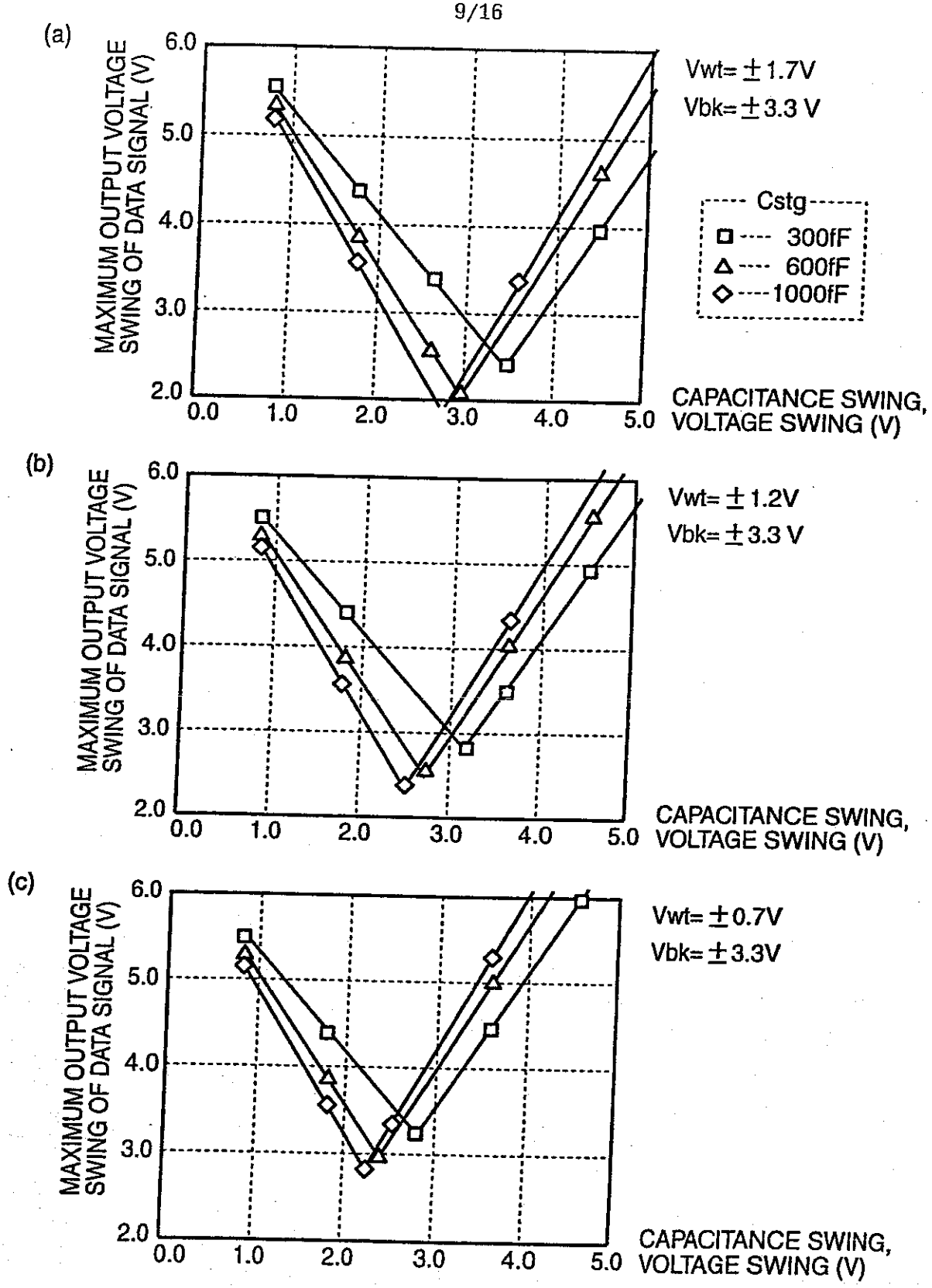

(a)
MAXIMUM OUTPUT VOLTAGE SWING OF DATA SIGNAL (V)
6.0
5.0
4.0
3.0
2.0
0.0
1.0
2.0
3.0
4.0
5.0
CAPACITANCE SWING, VOLTAGE SWING (V)
Vwt=±1.7V
Vbk=±3.3 V
Cstg
300fF
600fF
1000fF
(b)
MAXIMUM OUTPUT VOLTAGE SWING OF DATA SIGNAL (V)
CAPACITANCE SWING, VOLTAGE SWING (V)
Vwt=±1.2V
Vbk=±3.3 V
(c)
MAXIMUM OUTPUT VOLTAGE SWING OF DATA SIGNAL (V)
CAPACITANCE SWING, VOLTAGE SWING (V)
Vwt=±0.7V
Vbk=±3.3V

FIG. 9

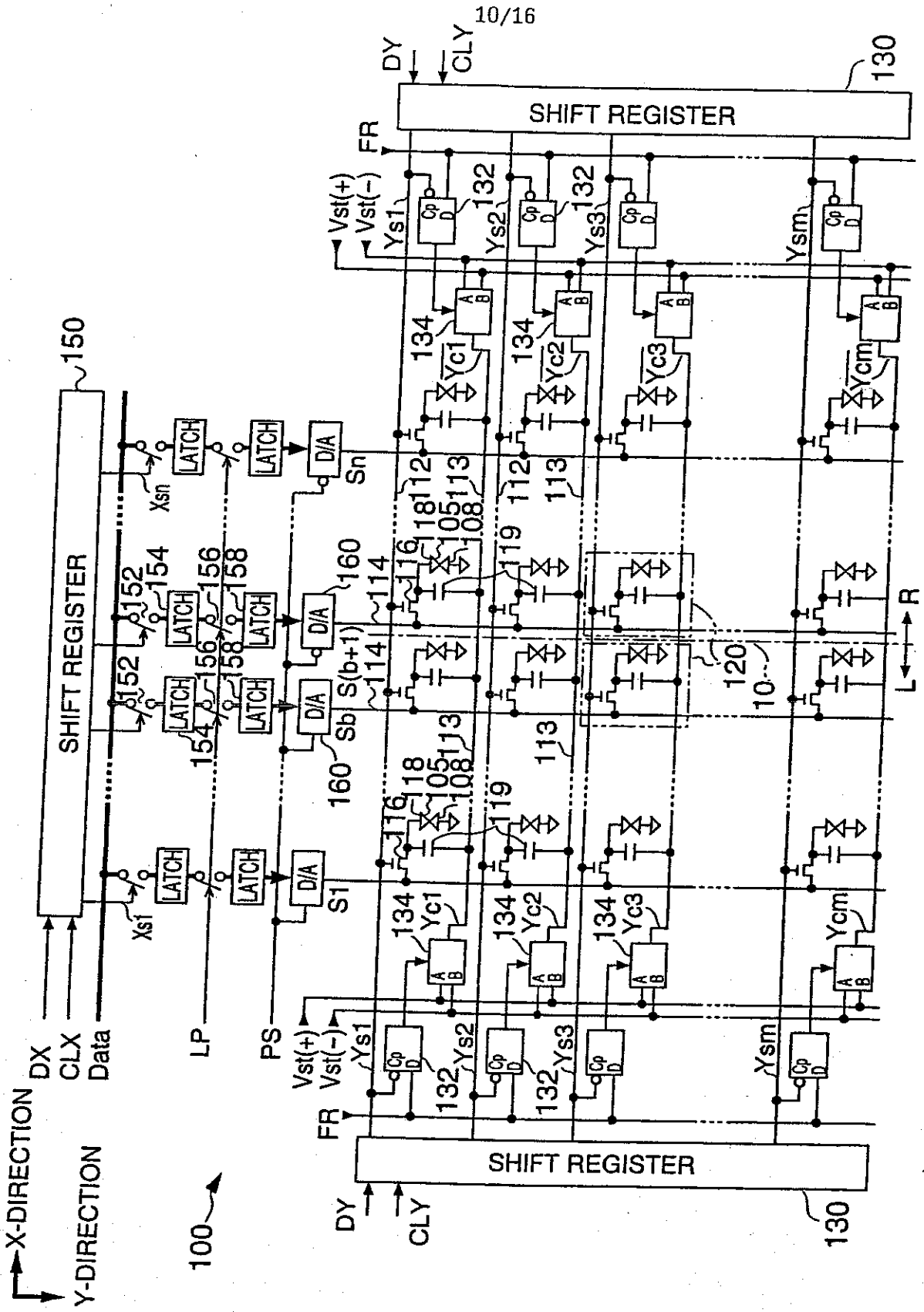

SHIFT REGISTER
SHIFT REGISTER
SHIFT REGISTER
LATCH
D/A
DY
CLY
FR
Vst(+)
Vst(-)
DX
CLX
Data
LP
PS
X-DIRECTION
Y-DIRECTION
100
150
130
132
134
160
R
L
120
10

FIG. 10

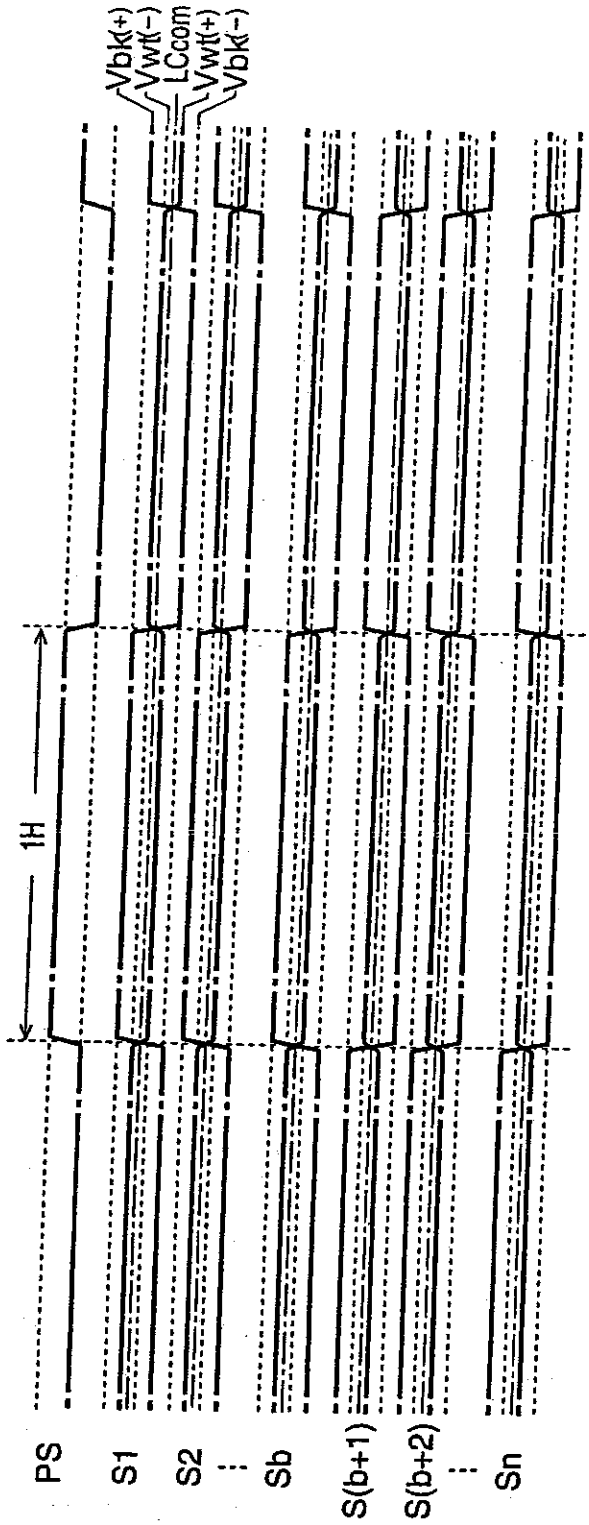


FIG. 11

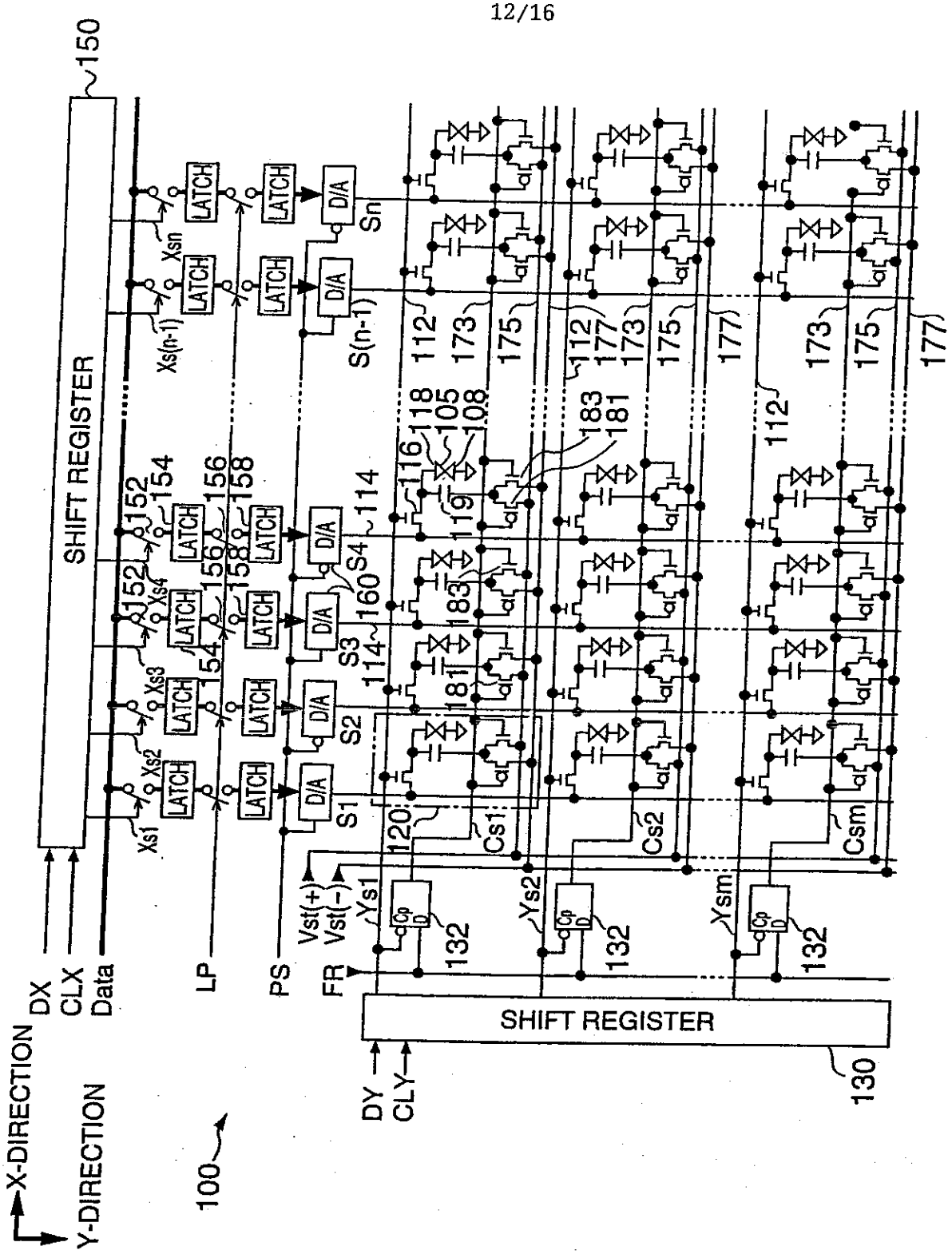

SHIFT REGISTER
150
LATCH
D/A
Sn
S(n-1)
S4
S3
S2
S1
Xsn
Xs(n-1)
Xs4
Xs3
Xs2
Xs1
152
154
156
158
114
160
116
118
105
108
119
183
181
112
173
175
177
120
Cs1
Cs2
Csm
Vst(+)
Vst(-)
Ys1
Ys2
Ysm
132
DX
CLX
Data
LP
PS
FR
DY
CLY
SHIFT REGISTER
130
X-DIRECTION
Y-DIRECTION
100

FIG. 12

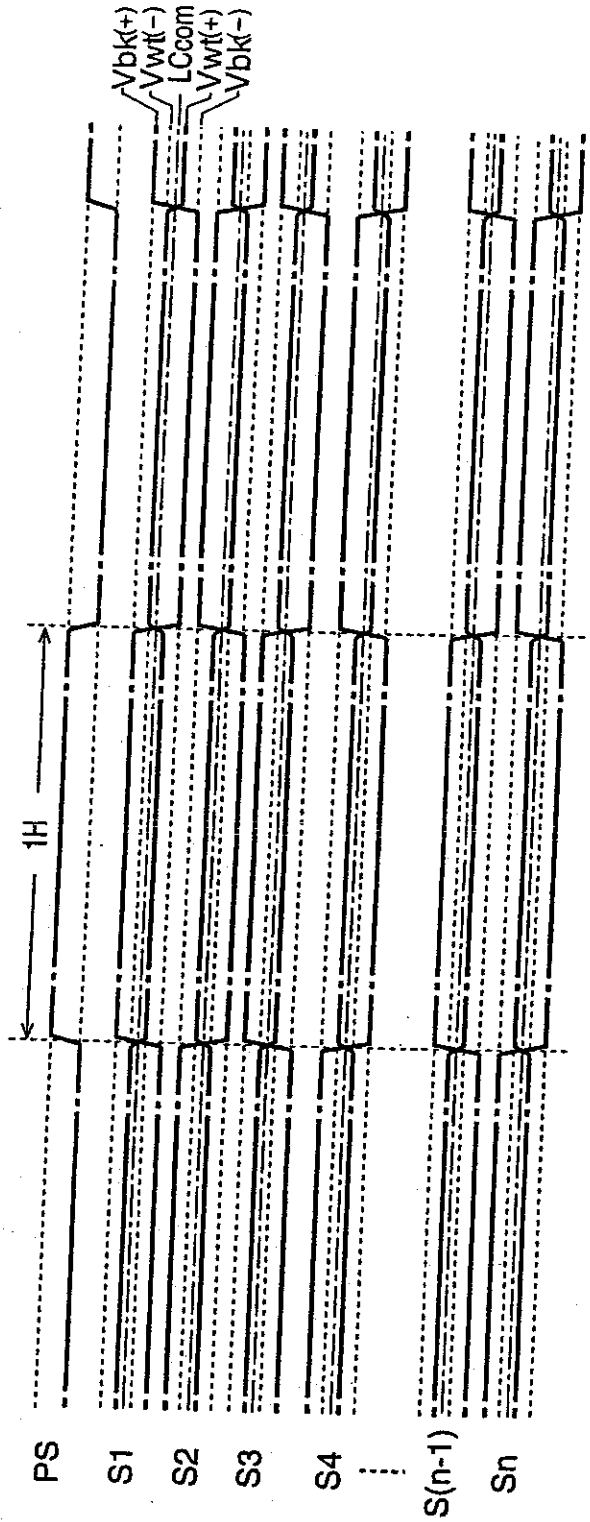


FIG. 13

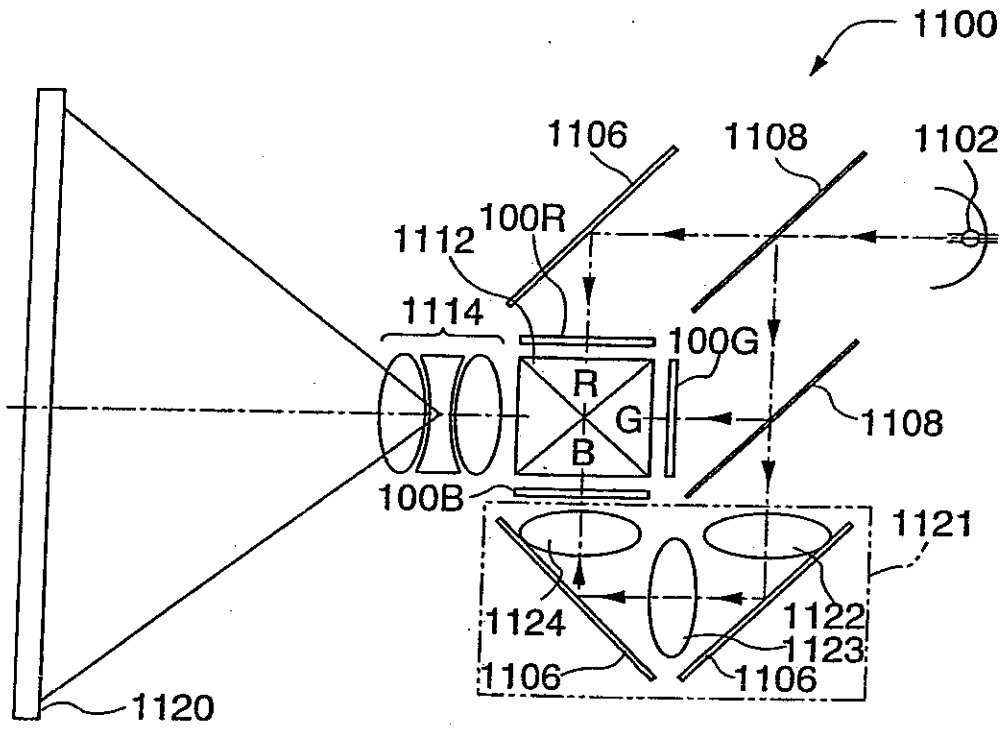

1100
1106
1108
1102
1112
100R
1114
100G
R
G
B
1108
100B
1121
1124
1122
1123
1106
1106
1120

FIG. 14

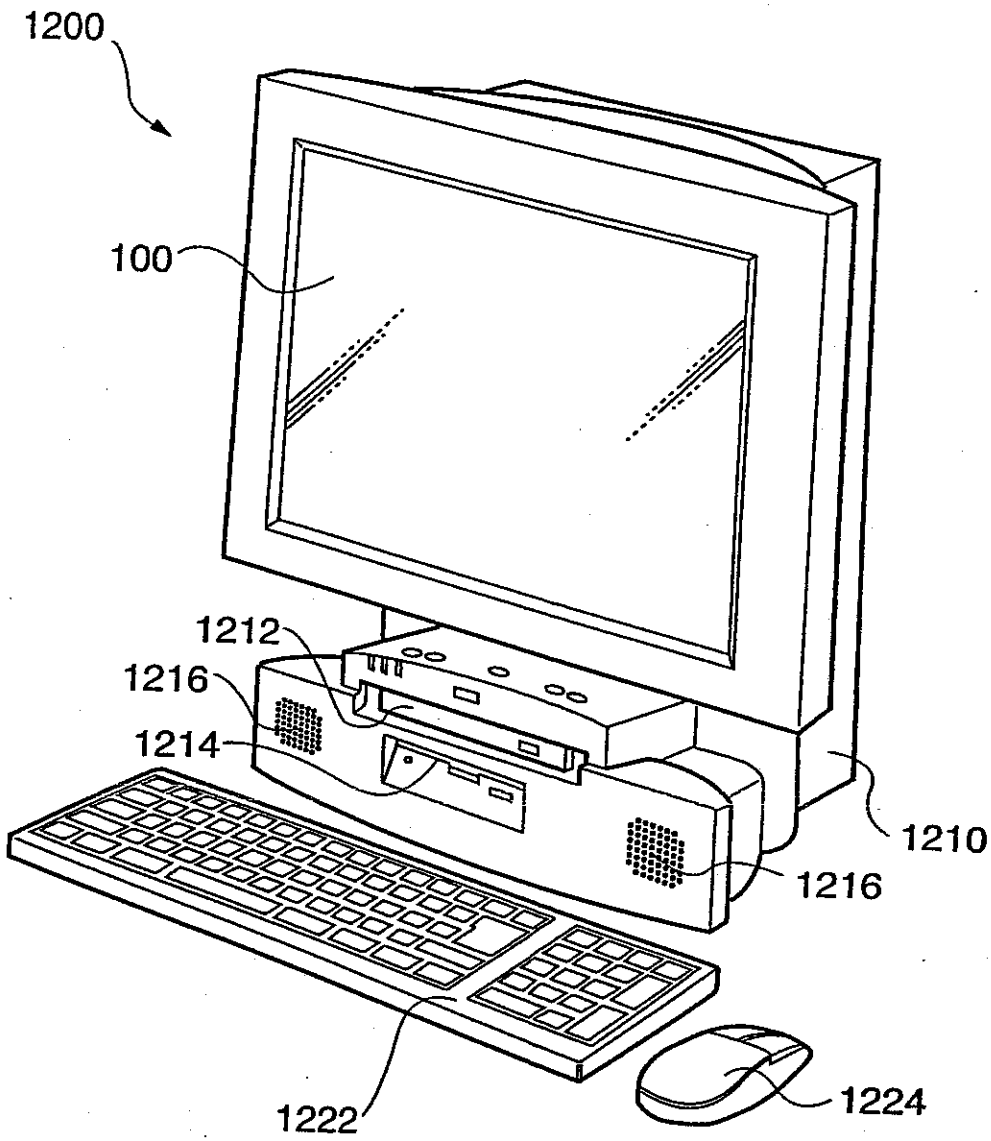


FIG. 15

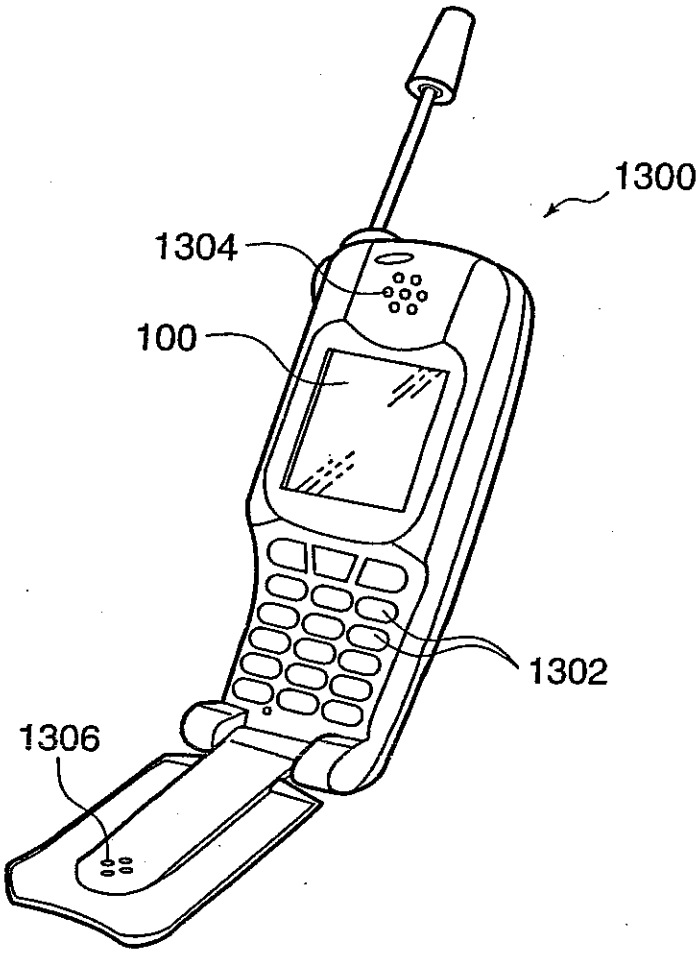


FIG. 16