WAFER LEVEL PACKAGING

ABSTRACT OF THE DISCLOSURE

An integrated circuit package (50) may include an integrated circuit chip (22) having an integrated circuit (14). A lead frame (28) may be opposite the integrated circuit chip (22). The lead frame (28) may include at least one lead (30) electrically coupled to the integrated circuit (14) by a connector (42). The lead (30) may be within a periphery (32) of the integrated circuit chip (22). An encapsulant (44) may cover the integrated circuit (14), the connector (42) and a portion of the lead frame (28). A remaining portion of the lead frame (28) may be exposed from the encapsulant (44).

Figure 1c