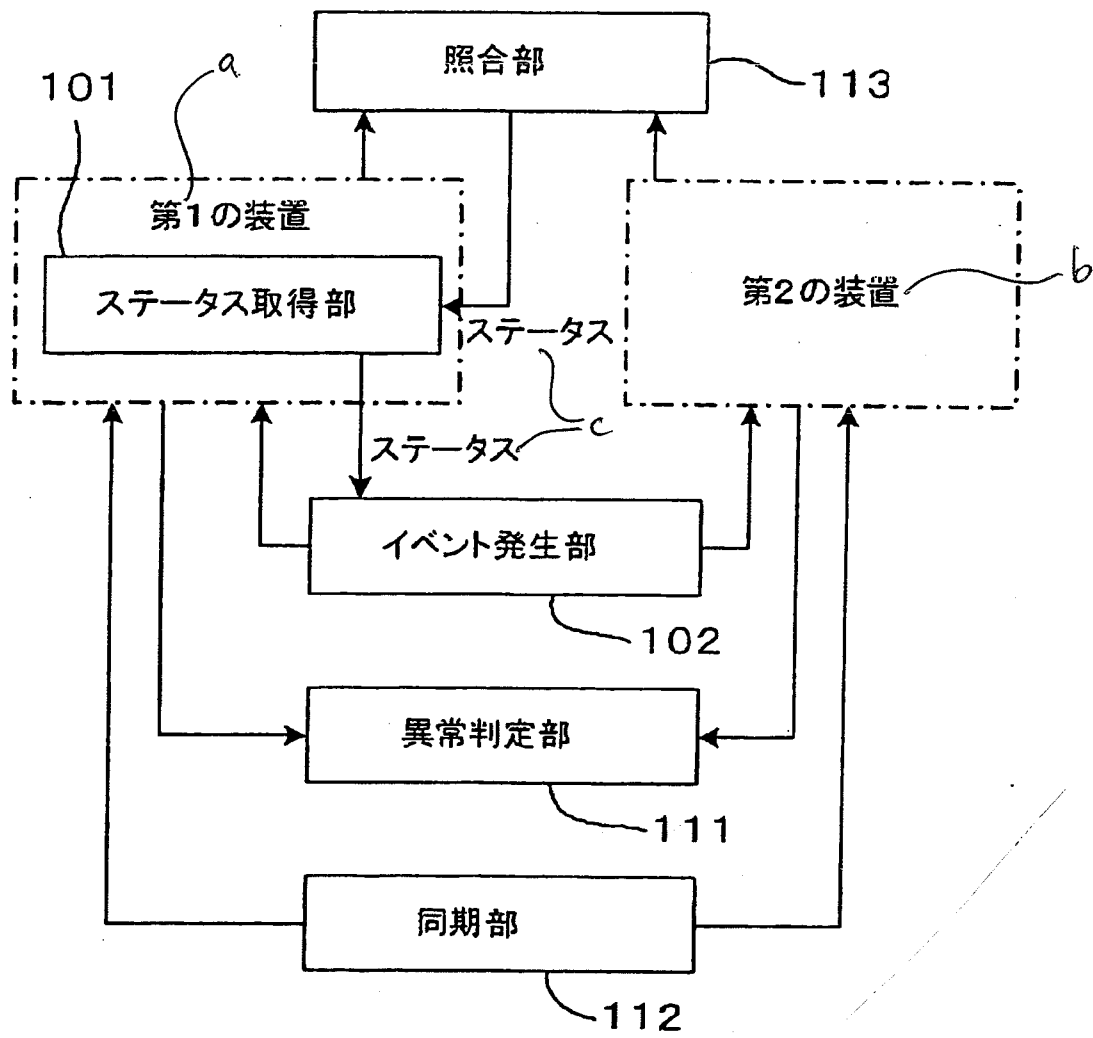
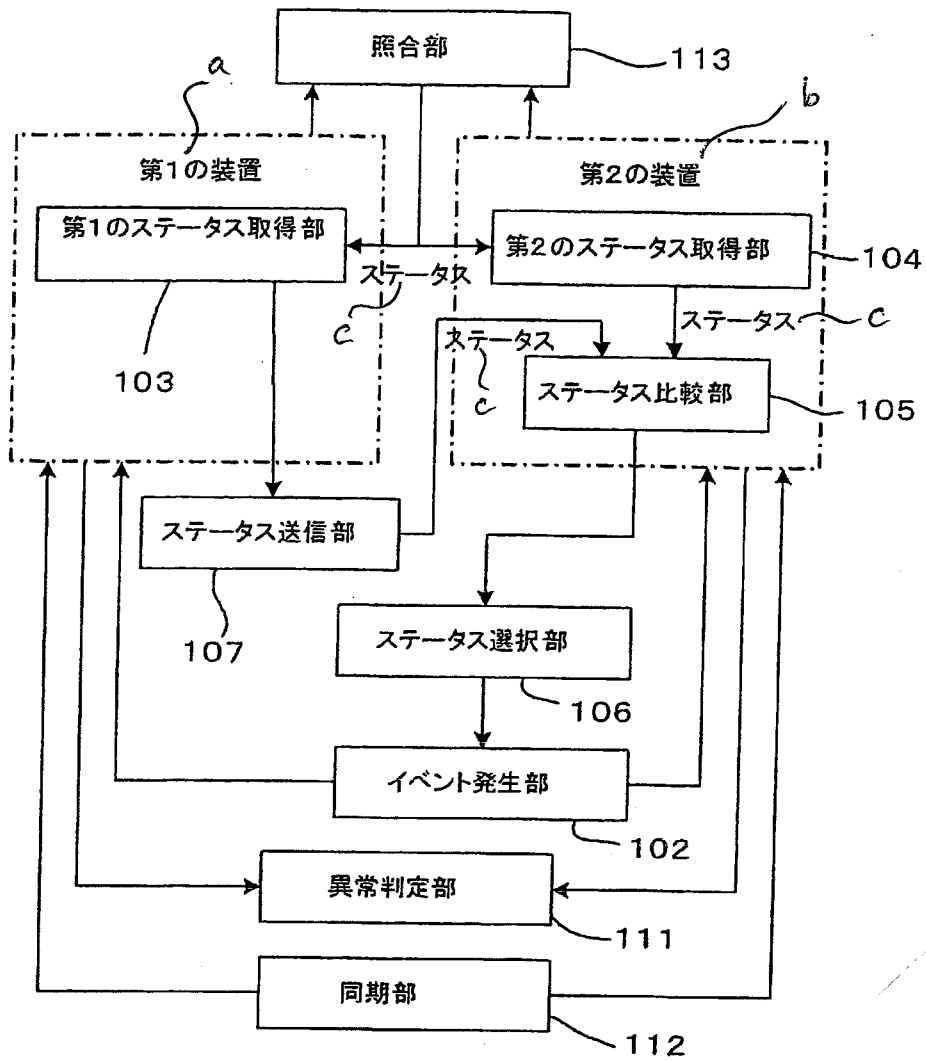


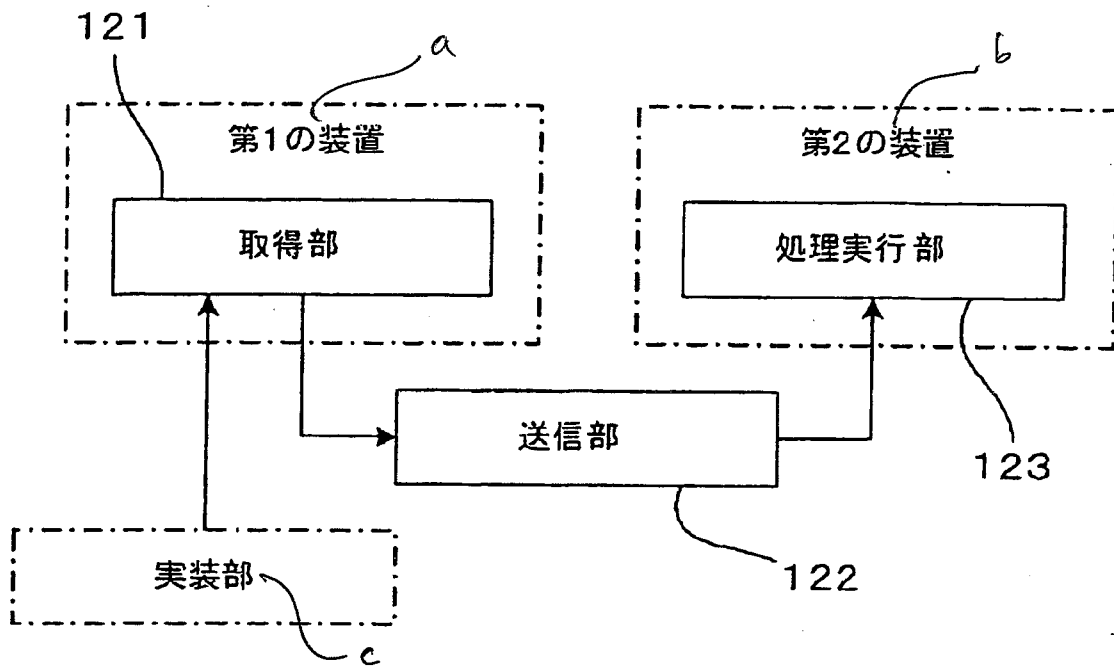
[図1] Fig. 1



~~[圖2]~~ Fig. 2



[図3] Fig. 3



[図4] Fig. 4

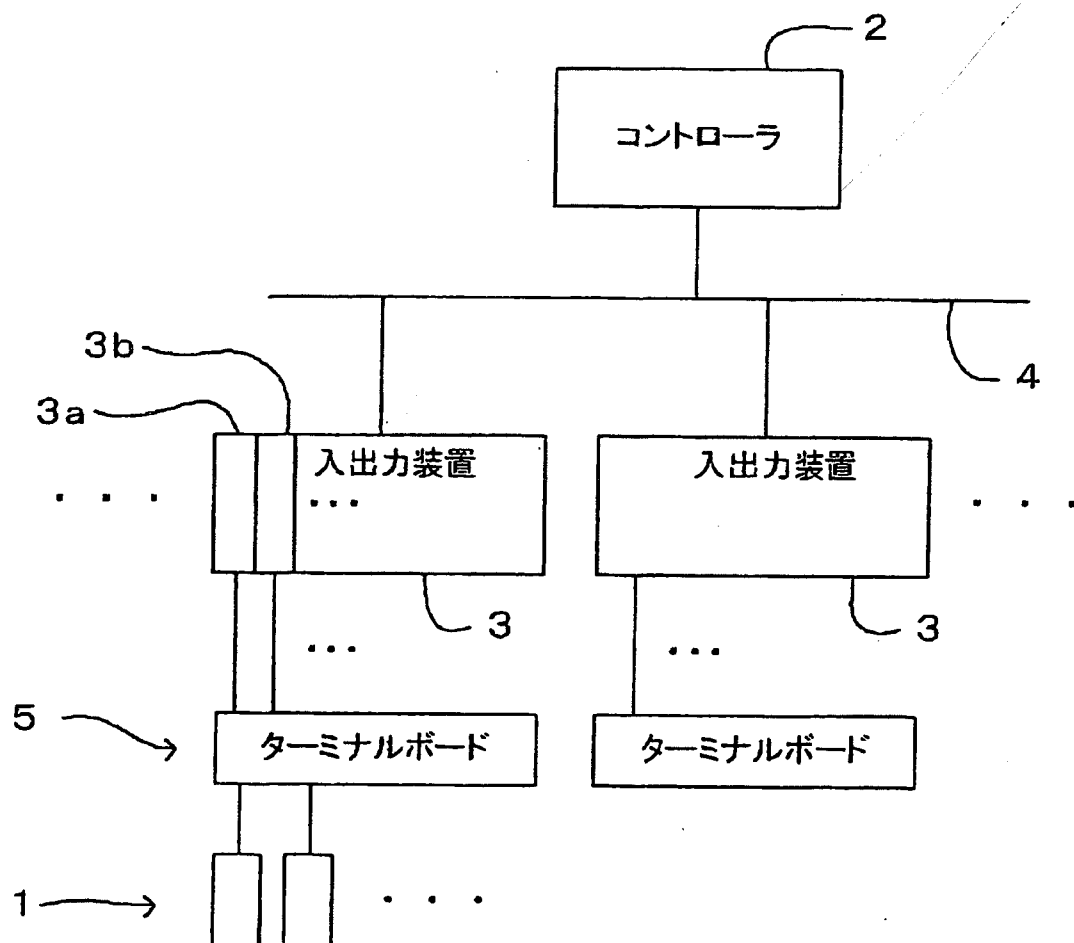


Fig. 5
[図5]

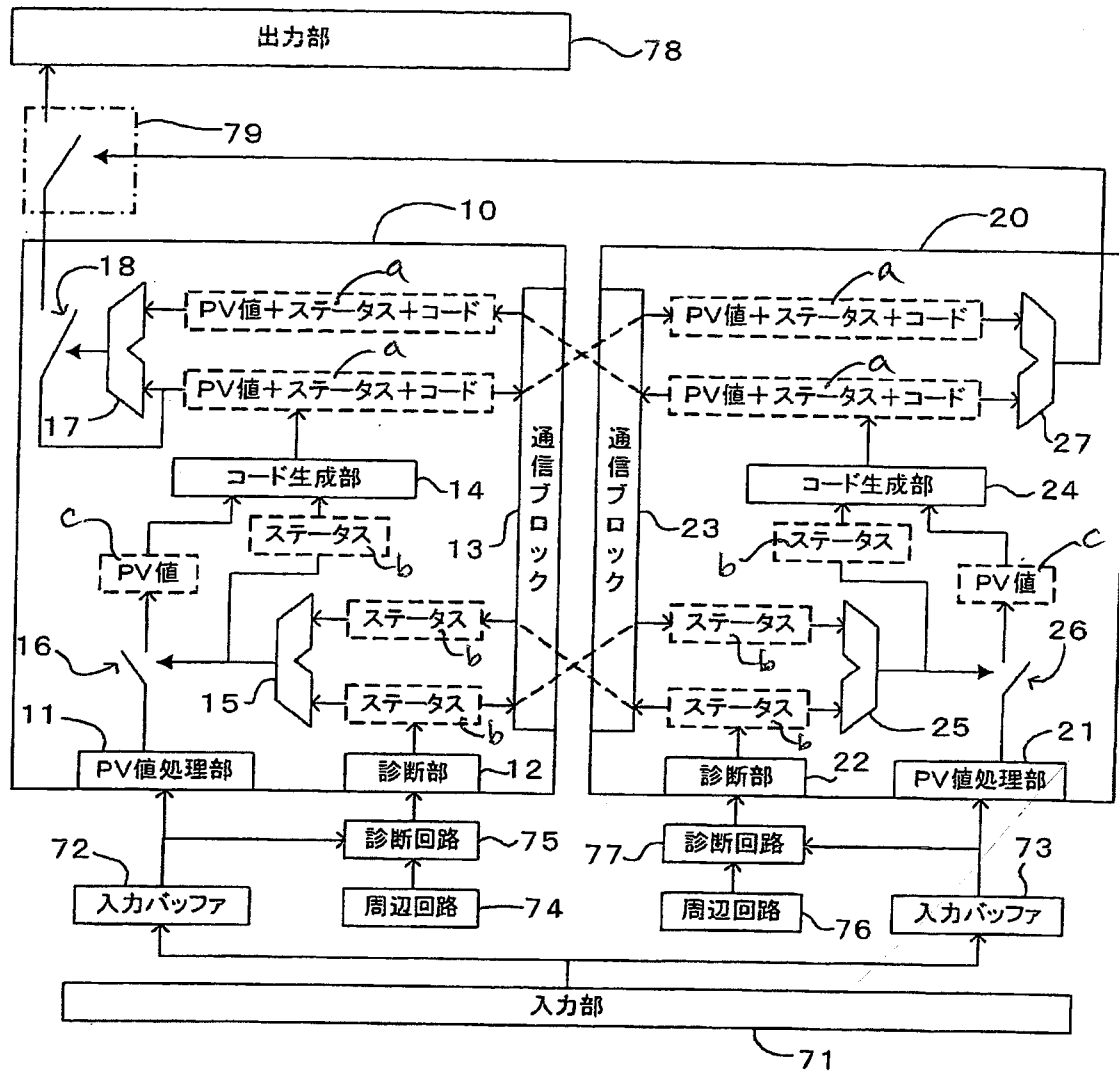


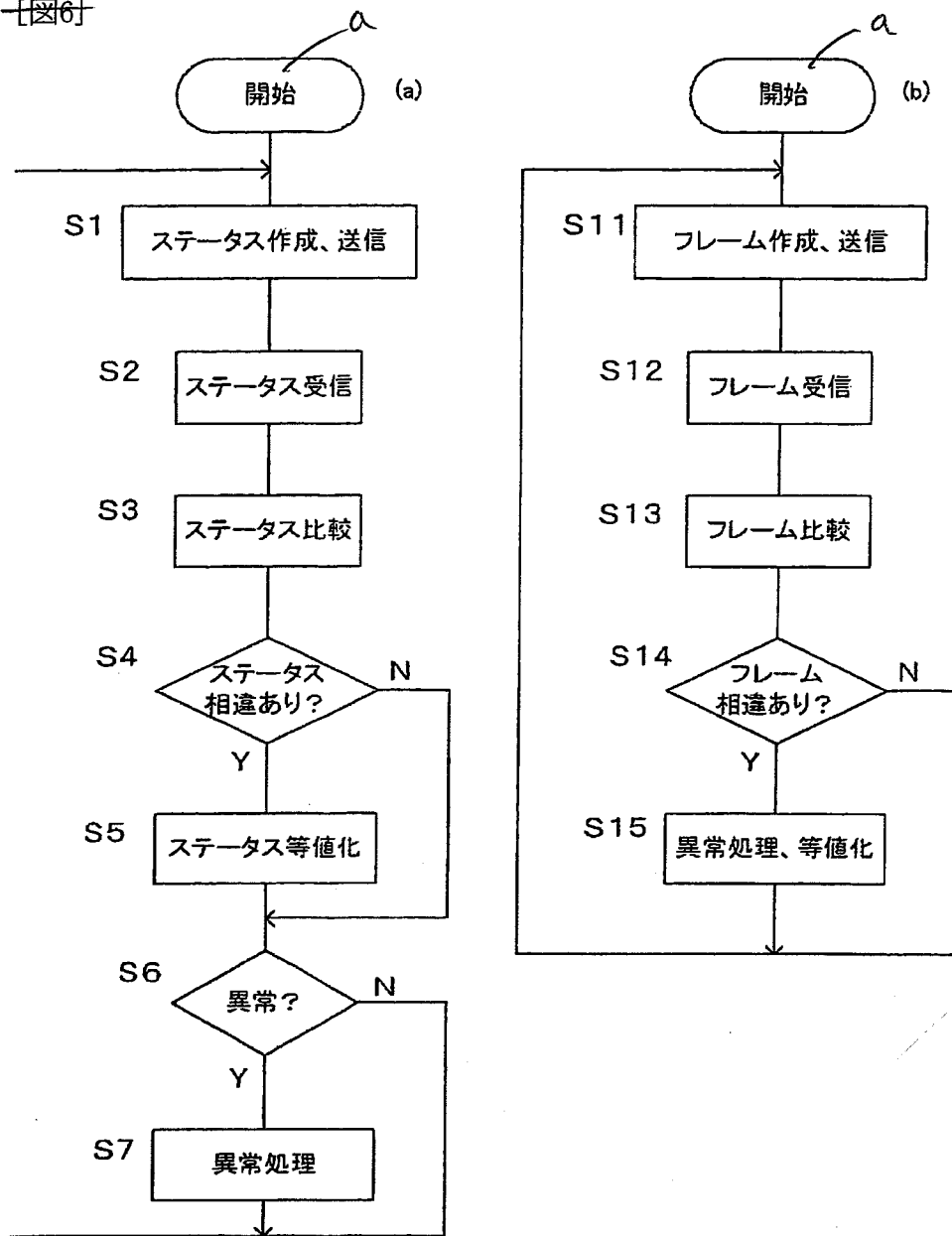
Fig. 6
[図6]

Fig. 7

[図7]

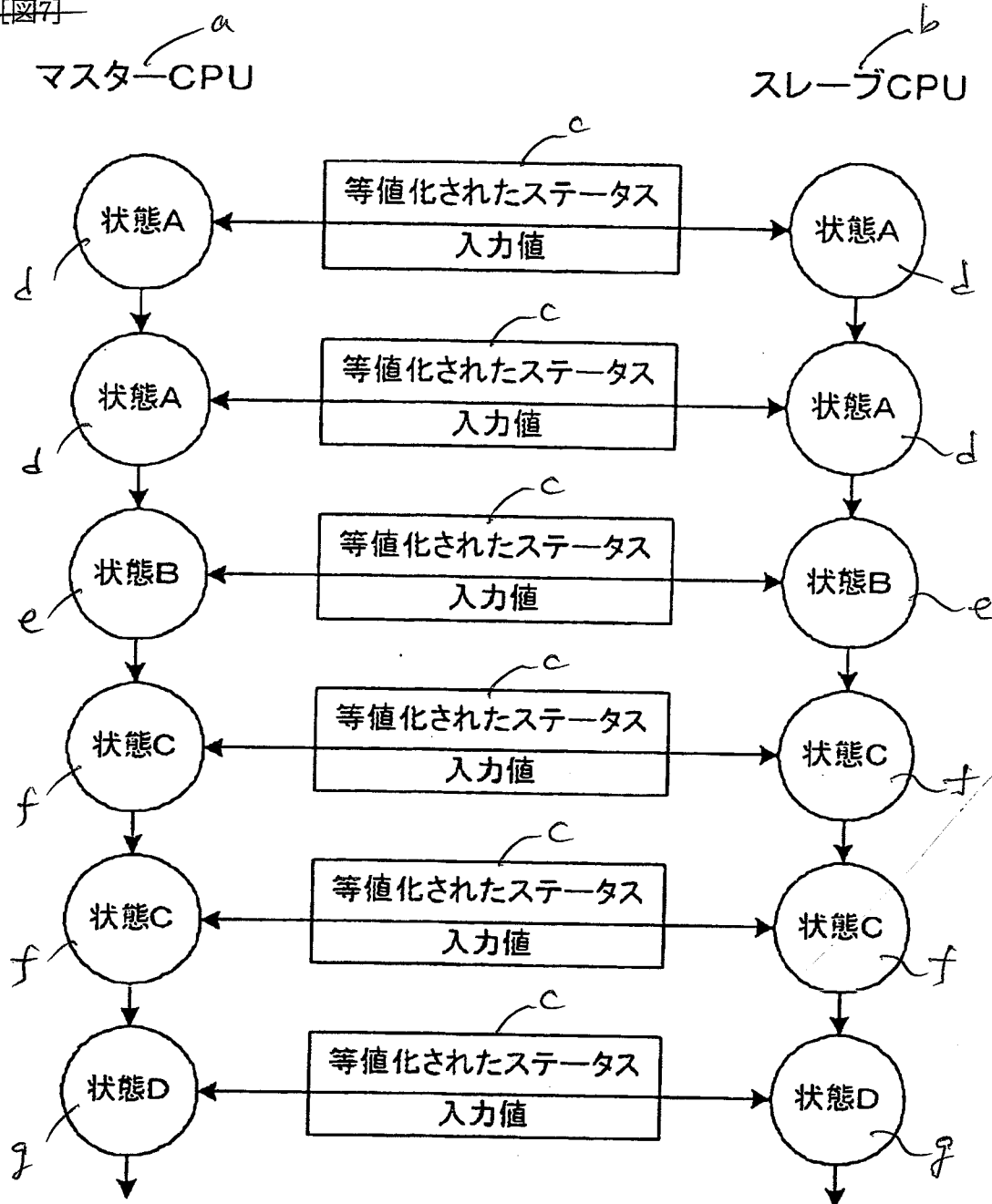


Fig. 8

[図8]

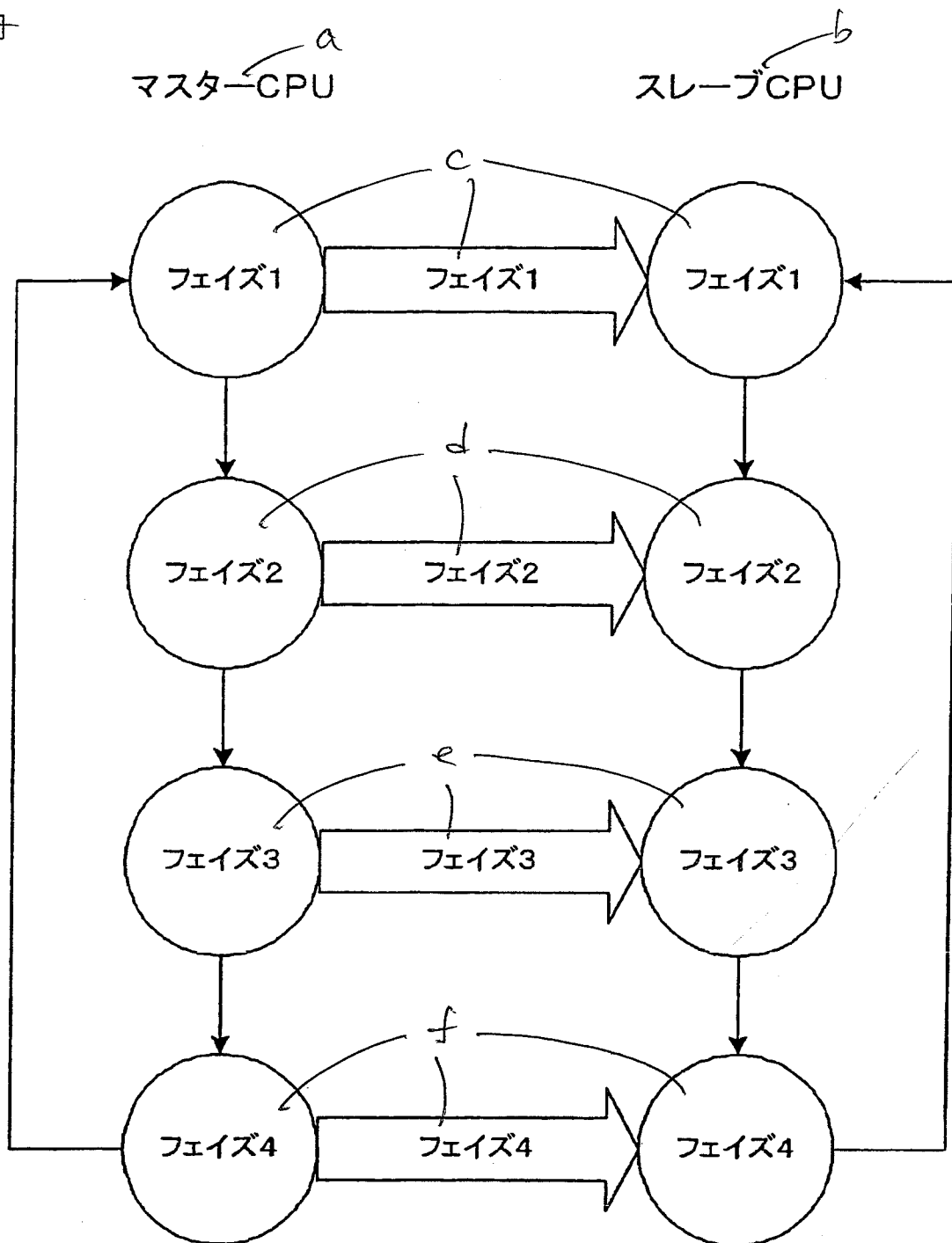
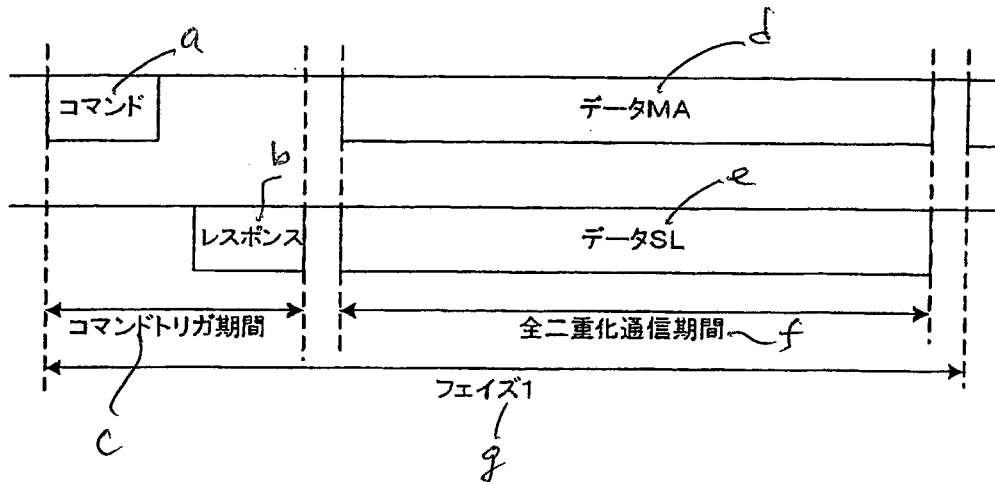


Fig. 9

[図9]

(a)



(b)

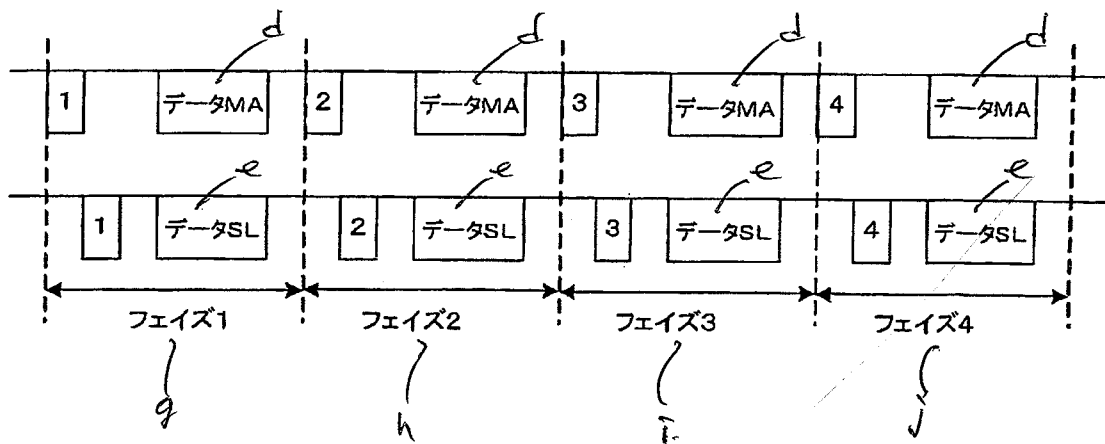


Fig. 10

[図10]

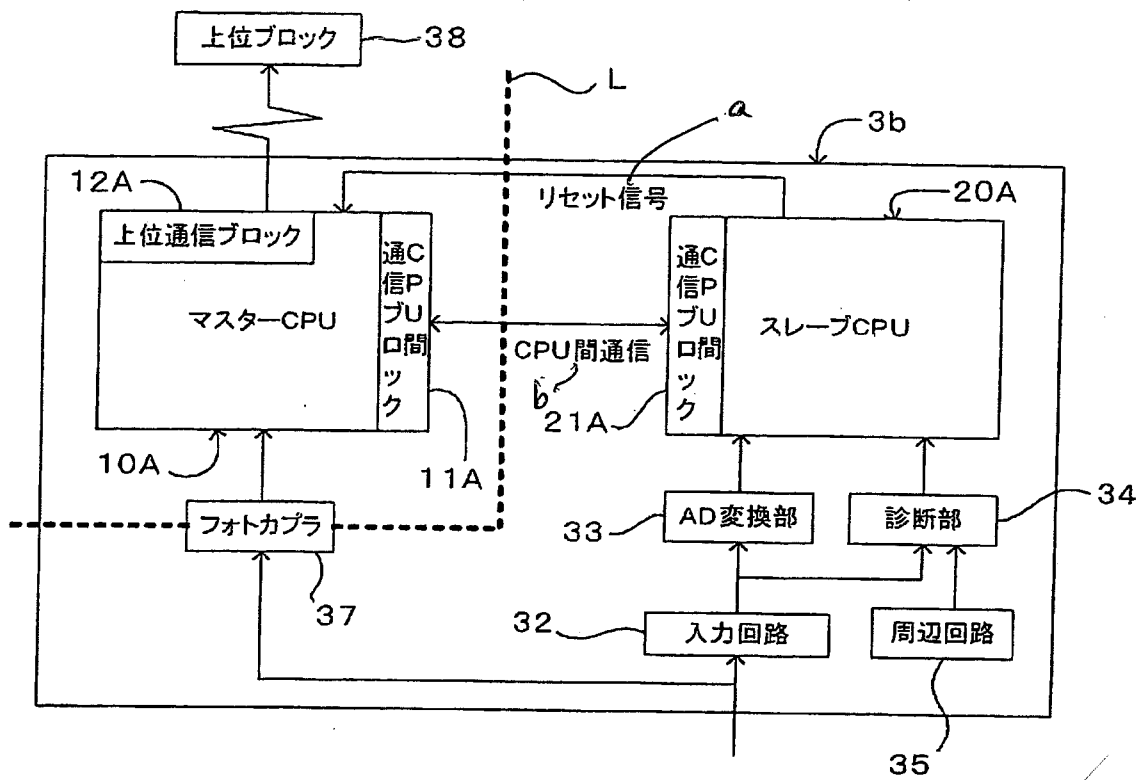


Fig. 11
[図11]

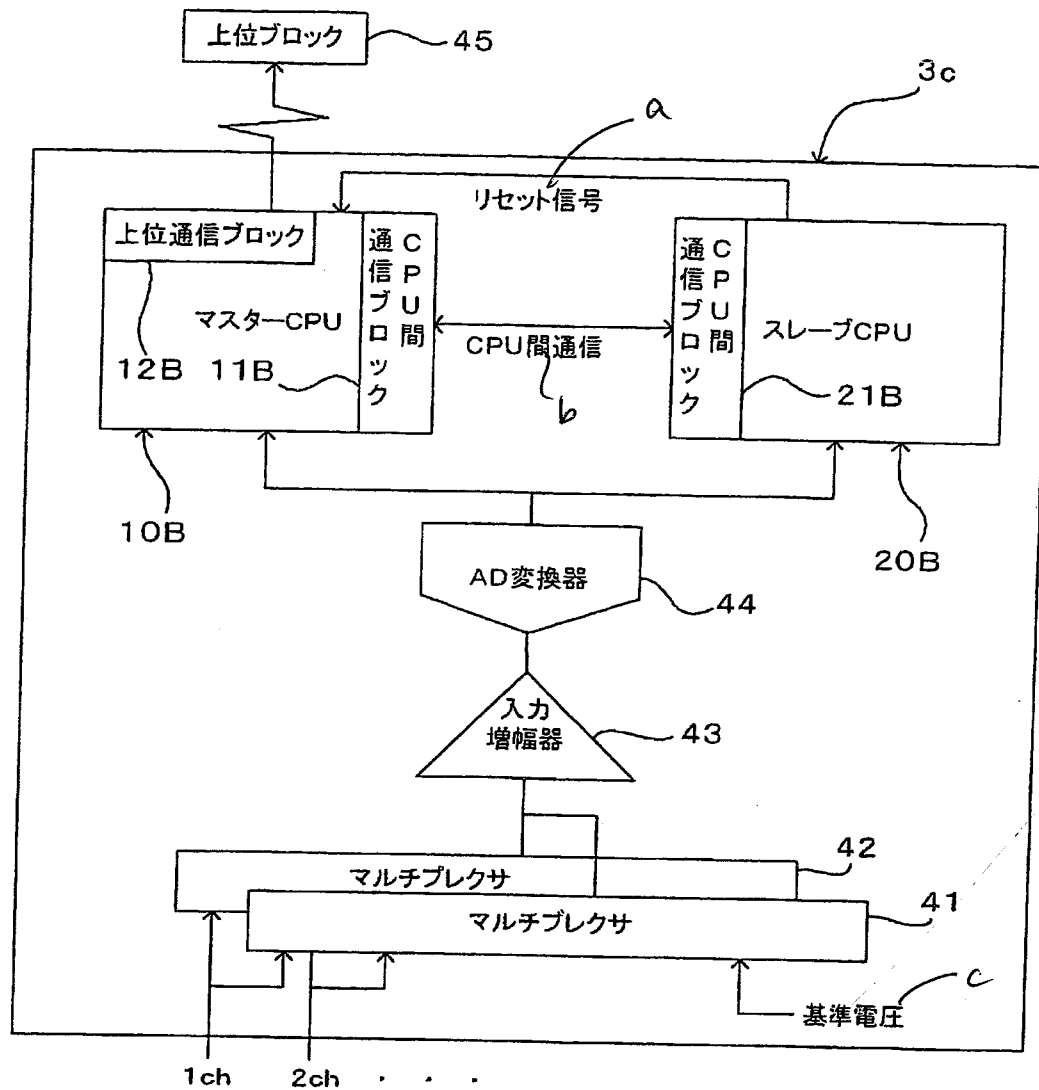


Fig. 12

[図12]

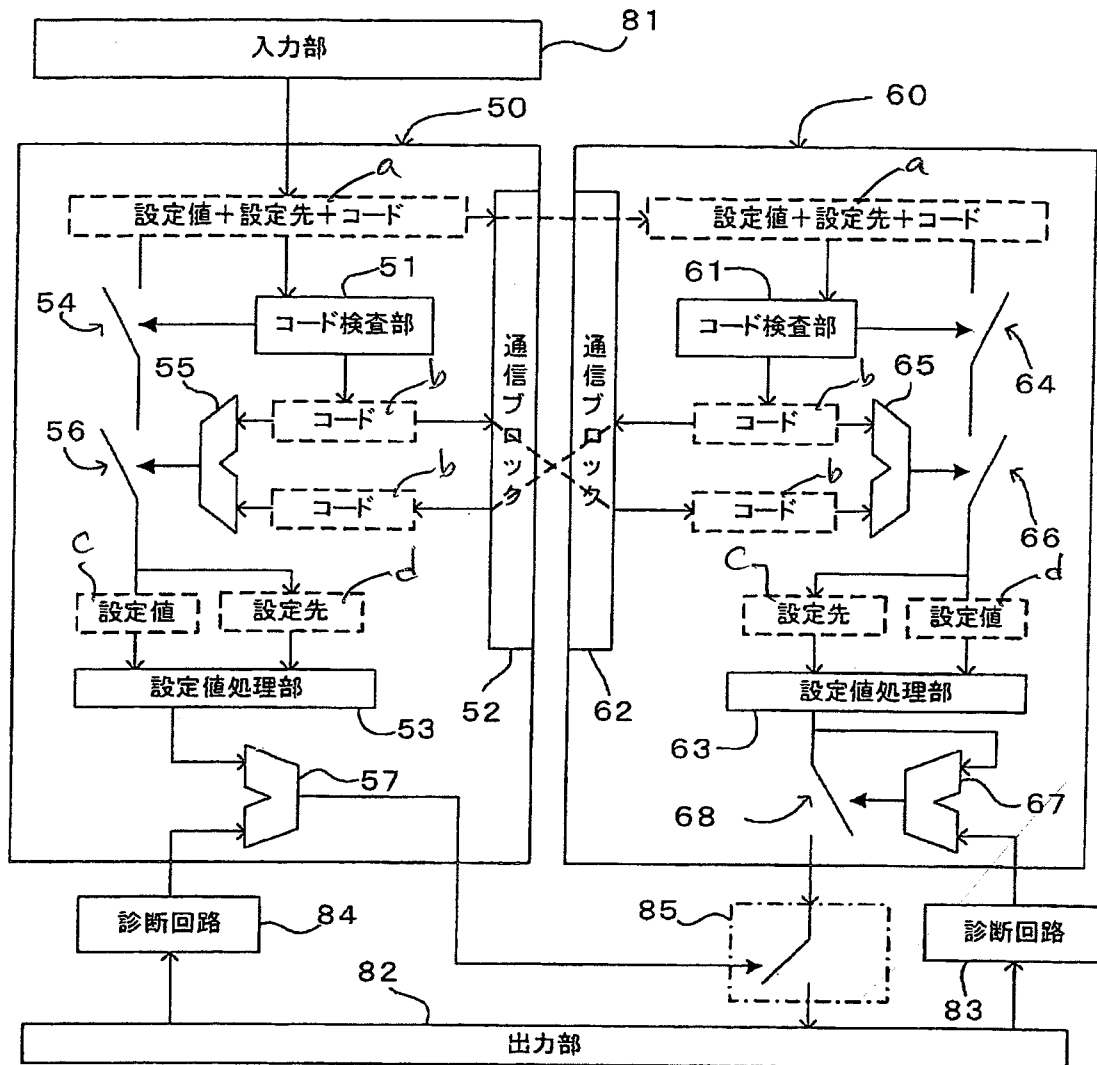


Fig. 1:

- a first device
- b second device
- c status
- 101 status acquiring part
- 102 event generating part
- 111 abnormality determining part
- 112 synchronizing part
- 113 collating part

Fig. 2:

- a first device
- b second device
- c status
- 102 event generating part
- 103 first status acquiring part
- 104 second status acquiring part
- 105 status comparing part
- 106 status selecting part
- 107 status sending part
- 111 abnormality determining part
- 112 synchronizing part
- 113 collating part

Fig. 3:

- a first device
- b second device
- c mounted part
- 121 acquiring part
- 122 sending part
- 123 process executing part

Fig. 4:

- 2 controller
- 3 input-output device
- 5 terminal board

Fig. 5:

- a PV value + status + code
- b status
- c PV value
- 11 PV value processing part
- 12 diagnostic part
- 13 communication block
- 14 code generating part
- 21 PV value processing part
- 22 diagnostic part
- 23 communication block
- 24 code generating part
- 71 input part

72	input buffer
73	input buffer
74	peripheral circuit
75	diagnostic circuit
76	peripheral circuit
77	diagnostic circuit
78	output part

Fig. 6:

a	start
S1	create and send status
S2	receive status
S3	compare status
S4	Are statuses different?
S5	status equalization
S6	Abnormal?
S7	abnormal processing
S11	create and send frame
S12	receive frame
S13	compare frame
S14	Are frames different?
S15	abnormal processing, equalization

Fig. 7:

a	master CPU
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- b slave CPU
- c equalized status, input value
- d state a
- e state b
- f state c
- g state d

Fig. 8:

- a master CPU
- b slave CPU
- c phase 1
- d phase 2
- e phase 3
- f phase 4

Fig. 9:

- a command
- b response
- c command trigger period
- d data MA
- e data SL
- f full-duplexing communication period
- g phase 1
- h phase 2
- i phase 3

j phase 4

Fig. 10:

a reset signal
b communication between CPUs
10A master CPU
11A communication block between CPUs
12A host communication block
20A slave CPU
21A communication block
32 input circuit
33 AD conversion part
34 diagnostic part
35 peripheral circuit
37 photo coupler
38 host block

Fig. 11:

a reset signal
b communication between CPUs
c reference voltage
10B master CPU
11B communication block between CPUs
12B host communication block
20B slave CPU

21B	communication block between CPUs
41	multiplexer
42	multiplexer
43	input amplifier
44	AD converter
45	host block

Fig. 12:

a	set value + set destination + code
b	code
c	set destination
d	set value
51	code inspection part
52	communication block
53	set value processing part
61	code inspection block
62	communication block
63	set value processing part
81	input part
82	output part
83	diagnostic circuit
84	diagnostic circuit