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(54) IMPROVEMENTS IN OR RELATING TO CHARGE TRANSFER DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195, Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to charge transfer devices.

One form of charge transfer device, the so-called "charge coupled device," is described in U.K. copending patent applications nos. 21832/71 and 21833/71 (Serial Nos. 1340619 and 1340620). In these devices information is represented by electronic signals in the form of "packets" of charge carriers localized by induced potential energy minima in suitable storage media such as semiconductors, semi-insulating semiconductors, and insulators. These copending applications describe a basic shift-register type of operation in which information is moved within the storage medium by transferring the "packets" of charge sequentially from each potential well to the one next adjacent.

In another form of charge transfer device, described in Great Britain copending patent application no. 21831/71 (Serial No. 1340618) "packets" of charge carriers are gated sequentially from zone to zone along the surface of a semiconductive body which includes a bulk portion of one type semiconductivity and a plurality of spaced localized zones of the other type semiconductivity. In these devices each zone is operated as a potential well, the boundary of which is defined by the PN junction which defines the zone. This type of charge transfer device is currently known as the "bucket-brigade" type by those in the art; this designation will be used below.

A problem in charge transfer devices is that a small fraction of the charge from each "packet" is left behind each time a "packet" is transferred from one potential well to another. As this charge loss results in signal degradation, some form of controlled charge regeneration and/or amplification must be provided if very long strings of information are to be so stored and processed.

It is also desirable to provide a device capable of performing a logic function. Perhaps the most basic of digital logic functions is "state inversion" (signal complementing) and "bit regeneration." Given these two basic functions, it is known that all other combinational logic functions, e.g., AND, OR, NAND, NOR, fan-in and fan-out, can be derived therefrom.

According to one aspect of this invention there is provided a charge transfer device wherein, in use, a localized region of stored charge carriers is transferable along a portion of a suitable storage medium by the application of suitable potentials to a plurality of electrodes associated with a surface of said medium, said device including regeneration means comprising means for detecting the amount of charge stored at a predetermined location in said medium, means for disposing of detected charge carriers, means for injecting charge carriers at another location in said medium, and gating means coupled to said detection means for controlling the transfer of newly-injected carriers away from said injection means in dependence upon charge detected at said predetermined location.

The storage medium may include a semiconductor body of a first type semiconductivity.

The detection means may comprise a floating conductive electrode insulated from said surface, or may include a zone of a second type semiconductivity disposed in said body and adjacent to one of said electrodes for sensing the number of charge carriers under said one electrode.

The injection means may include a zone of a second type semiconductivity disposed in said body.

The said plurality of electrodes may be serially disposed and there may be provided a further plurality of serially disposed electrodes associated with said surface for transferring a localized region of charge carriers, and a pair of conduction paths, alternate electrodes in said plurality and said further plurality being connected to one of said pair and the other electrodes in said pluralities being connected to the other one of said pair, said regeneration means being interposed between the end of said plurality of serially disposed electrodes and the start of said further plurality of serially disposed electrodes.

In one form the device may have a plurality of channels along which localized regions of charge carriers are transferrable each of said channels being defined by a respective plurality of serially-disposed electrodes, and said detection means may include a plurality of separate detection means each being disposed for detecting charge carriers at a predetermined location in a respective channel, and said gating means may include a plurality of means disposed in series with respect to said injection means whereby, in use, carriers are transferrable from said injection means only if less than a predetermined number of carriers exist at each of said predetermined locations, whereby said device is operable to provide a logical NOR-function.

In another form the device may have a plurality of channels along which localized regions of charge carriers are transferable each of said channels being defined by a respective plurality of serially-disposed electrodes, and said detection means may include a plurality of separate detection means each being disposed for detecting charge carriers at a predetermined location in a respective channel, and said gating means may include a plurality of means disposed in parallel in relation to said injection means whereby, in use, carriers are not transferable away from said injection means only if greater than a predetermined number of carriers exist at each of said predetermined locations, whereby said device is operable to provide a logical NAND-function.

According to another aspect of this invention there is provided a charge transfer device wherein, in use, a localized region of stored charge carriers is transferable along a portion of a suitable storage medium by the application of suitable potentials to a plurality of electrodes associated with a surface of said medium, said device including regeneration means comprising means for detecting the amount of charge stored at a predetermined location in said medium, means for pre-biasing the detection means to a fixed reference level prior to said detecting, means for injecting charge carriers at another location in said medium, and gating means coupled to said detection means for controlling the transfer of newly-injected carriers away from said injection means in dependence upon charge detected at said predetermined location.

The said storage medium may include a semiconductor body of a first type semiconductivity.

The said detection means may include a first zone of a second type semiconductivity in said body and adjacent to one of said plurality of electrodes for sensing the number of charge carriers under said one electrode, said pre-biasing means may include a second zone of the second type semiconductivity in said body and spaced from said first zone, and a first control electrode disposed over and insulated from at least part of the surface of said medium between said first and second zones, said injection means may include a third zone of the second type semiconductivity in said body and spaced from another of said plurality of electrodes, and said gating means may include a second control electrode disposed over and insulated from at least part of the surface of said medium between said injection means and said other electrode and conductively connected to said first zone.

The said third zone may be conductively connected to said first control electrode.

The device may be provided with a pair of conduction paths, each alternate electrode in said plurality of electrodes being connected to one of said pair, and the other electrodes in said plurality of electrodes being connected to the other one of said pair, said first control electrode being connected to the one of said pair to which the electrode adjacent the first zone is not connected.

The said other electrode may be conductively connected to said one electrode.

Preferably said other electrode is larger than the other ones of said plurality of electrodes.

In either aspect of the invention the said storage medium may include a semiconductor body of a first type semiconductivity, and a plurality of spaced localized zones of a second type semiconductivity disposed adjacent said surface of said body and asymmetrically with respect to said plurality of electrodes such that each of said plurality of electrodes

extends over the space between a pair of said localized zones and over one zone of said pair of zones more than over the other zone of said pair of zones.

The invention will now be described and explained by way of example with reference to the accompanying drawing in which:

FIG. 1 is an isometric cross-sectional view of a basic charge coupled device adapted primarily for three-phase operation;

FIGS. 2A—2C are schematic cross-sections of a linear arrangement of devices of the type shown in FIG. 1;

FIG. 3 is a cross-sectional view of a basic charge coupled device adapted for two-phase operation;

FIG. 4 is a cross-sectional view of a device including means for introducing a controlled amount of charge into the device channel.

FIGS 5 and 6 are isometric cross-sectional views of devices embodying the invention;

FIGS. 7—10 are schematic plan views of other devices embodying the invention;

FIGS. 11—14 are schematic plan views of logic devices embodying the invention;

FIG. 15 is a schematic cross-sectional view of a "bucket-brigade" device embodying the invention;

FIG. 16 is a schematic plan view of another device embodying the invention;

FIG. 17 is a cross-sectional view taken along line 17—17 in FIG. 16;

FIG. 18 is a schematic plan view of a device similar to that shown in FIG. 16 but modified to increase the output signal from the inversion-regeneration element;

FIG. 19 is a schematic plan view of yet another device embodying the invention; and

FIG. 20 is a cross-sectional view taken along line 20—20 in FIG. 19.

It will be appreciated that for simplicity and clarity the figures have not necessarily been drawn to scale. Reference numerals have been repeated from figure to figure to indicate corresponding elements where appropriate.

The present invention will be described by first briefly reviewing the structure and operation of the "charge coupled" type of devices described in the first two of the above-referenced copending patent applications. For a detailed description of their structure and operation reference is to be made to these copending applications.

In charge coupled devices (CCD's), digital information is represented by the presence or absence of a "packet" of charge carriers localized in and electro statically "coupled" to artificially induced potential energy minima, e.g., potential wells, often adjacent a surface of a suitable storage medium. Advantageously the potential wells are formed and controlled by application of voltages to field plate electrodes of the type conventionally used in the metal-insulator-semiconductor (MIS) devices.

FIG. 1 shows a basic charge coupled device *20* adapted primarily for three-phase operation and including a semiconductive N-type bulk portion 21 overlying which there is a relatively thin insulating layer 22. Overlying layer 22 are a plurality of close-spaced serially-disposed electrodes 24—26 connected by overlay contacts to sources of potential $(-V_1)$, $(-V_2)$, and $(-V_3)$, respectively. The V_i's will be taken as positive numbers, and V_3 is greater than V_2 which, in turn, is greater than V_1. V_1 is greater than V_T where V_T is the threshold voltage for producing an inversion of the semiconductor surface under steady state conditions.

Broken line 27 represents schematically the surface potential (depth of the potential wells) adjacent the surface. Where, as here, the operating medium is semiconductive, broken line 27 may also be considered as representing schematically the boundaries of depletion regions formed by voltages applied to the electrodes.

Charge carriers, holes in this case, are represented schematically by plus signs in the potential wells. As holes tend toward points of most negative potential, it is readily seen that holes stored under electrode 25 in FIG. 1 will transfer into the potential well under electrode 26 until all the holes have been transferred or until sufficient holes have transferred that the surface potentials under electrodes 25 and 26 have become equal, whichever occurs first. In operation, of course, ideally all the holes would be transferred to avoid loss of signal information but this, in fact, does not usually happen.

Turning now to FIGS. 2A—2C, a linear array of devices of the type shown in FIG. 1 has every third electrode connected to a common one of three clock line conduction paths 41—43. Because the electrodes function in triplets they are all given reference numerals 24—26 with successive alphabetic suffixes A, B, C, etc.

FIG. 2A represents an initial condition with $(-V_2)$ applied to the electrodes numbered 24 and $(-V_1)$ applied to the other electrodes, 25 and 26. In this figure and in the other other figures to be described below, the semiconductive portion is assumed to be held at zero potential. For the purpose of discussion, it is presumed that approximately equal amounts of positive charge (holes) exist under electrodes 24A and 24C and none under electrode 24B. This, of course, may be thought of as a logical "one" stored under electrodes 24A and 24C and as a logical "zero" stored under electrode 24B.

FIG. 2B shows the state of the structure of FIG. 2A after the voltage on clock line 42 has been changed to $(-V_3)$. Because $V_3 > V_2 > V_1$ the charge (or absence of charge)

previously under electrodes 24A, 24B, and 24C has transferred to the right into deeper potential wells now under electrodes 25A, 25B, and 25C. FIG. 2C shows the same structure again in a resting or holding state, i.e., with $(-V_1)$ applied to clock lines 41 and 43 and $(-V_2)$ applied to clock line 42, a condition adapted to retain the logical states under electrodes 25A, 25B, and 25C. The cycle is then in the condition shown in FIG. 2A and is ready to be repeated so as to move the logic states under electrodes 26A, 26B, 26C, etc.

In CCD's of the type shown in FIGS. 1 and 2A—2C in which the electrodes are at all points equidistant from a relatively uniformly doped semiconductor surface, symmetrical potential wells tend to form under each electrode. Because of this, three-phase operation of the electrodes in triplets is advantageous to provide asymmetry to the potential wells and thus to ensure unidirectionality of charge transfer. This is described in greater detail in the first two of the above-referenced copending patent applications.

Such is not the case in CCD structures of the type shown in FIG. 3 where each electrode 53 and 54 is formed over an insulator 52 of nonuniform thickness over a semiconductive portion 51. In FIG. 3 every second electrode is connected to a common one of two clock lines 55 and 56 which, in turn, are driven by a two-phase clock which alternately applies $(-V_1)$ and $(-V_2)$ to them. Note that the potential wells in FIG. 3 are inherently asymmetrical and that each time the clock line voltages are changed the stored logical state is transferred one step (one electrode) to the right in FIG. 3. All this is described in more detail in the second of the above-referenced copending patent applications.

Regardless of whether the CCD is adapted for two-phase, three-phase, or four-phase operation the problem still remains that normally a small fraction of the charge to be transferred is left behind each time a "packet" is transferred from one potential well to the next. To compensate for this and to provide combinational logic functions in CCD's, some form of controlled charge regeneration is required. As part of the solution, FIG. 4 represents a convenient means for introducing a controlled amount of charge into a CCD information channel.

In FIG. 4, electrodes 24A—26B represent a linear array of CCD electrodes spaced from the surface of an N-type semiconductive portion 61 by an insulating layer 62. Semiconductor 61 includes a P-type localized zone 63 to which a reverse-bias $(-V_S)$ is applied through an electrode 64. Broken line 65 represents schematically the depth of the potential wells under the electrodes 24A—26B, the surface potential under electrodes 24A and 24B being more negative than under the others. If $(-V_S)$ is more negative than the surface potential under electrode 24A, no holes will flow from zone 63 into the CCD channel. If $(-V_S)$ is less negative than the surface potential under electrode 25A, holes will flood into the channel filling up the potential wells until the surface potential along the entire channel has risen to about $(-V_S)$.

However, if $(-V_S)$ is more negative than the surface potential under electrode 25A but less negative than the surface potential under electrodes 24A, then holes will flow from zone 63 into the CCD channel and only partially fill the potential well under electrode 24A. Once sufficient holes have accumulated in the potential well under electrode 24A that the surface potential there is about equal to $(-V_S)$, then holes stop flowing into the CCD channel.

Thus, by adjusting V_S in relation to the voltages applied to the CCD electrodes, a controlled amount of charge can be selectively injected or not injected to generate a digital bit stream flowing in a new CCD channel to the right in FIG. 4. It will be appreciated that zone 63 is adapted to operate in similar fashion as the source in an insulated gate field effect transistor (IGFET).

If now a bit generator such as shown in FIG. 4 is combined with and coupled to a detector which senses the bits being transferred in a CCD channel, the bit generator can be made to regenerate into a new channel the information being transferred in the degraded channel in response to signals from the detector. FIGS. 5 and 6 illustrate two embodiments of such bit regenerators.

The device of FIG. 5 includes an N-type semiconductive bulk portion 71 and an overlying insulating layer 72. Serially disposed field plate electrodes 26Y, 24Z, 25Z, and 26Z represent the end of a CCD channel whose bit stream is to be regenerated. Serially disposed field plate electrodes 34A, 35A, and 36A represent the beginning of a fresh CCD channel to accept the regenerated bit stream. As in FIGS. 1 and 2A—2C, every third CCD electrode is connected to a common one of three clock lines 73—75.

A pair of P-type localized zones 76 and 77 are disposed adjacent the surface of semiconductor 71 and are conductively connected through electrodes 78 and 79 to sources of negative potential $(-V_D)$ and $(-V_S)$, respectively. P-type zone 76 is disposed adjacent the last electrode 26Z in the degraded channel, and, advantageously, $(-V_D)$ is selected to maintain P-type zone 76 more negative than the most negative surface potential induced under CCD electrode 26Z so that as each bit is transferred under electrode 26Z it is collected and destroyed, i.e., conducted to ground. It will be appreciated

that zone 76 is thus adapted to operate in similar fashion as the drain in an IGFET.

P-type zone 77 is adapted to operate as a bit generator, and, accordingly, $(-V_S)$ applied thereto advantageously is selected to maintain zone 77 sufficiently negative that only enough holes are drawn selectively therefrom to partially fill the potential wells under electrode 34A without flooding the new CCD channel.

Disposed under CCD electrode 25Z is an electrically floating sensor electrode 80 which is spaced from electrode 25Z and from the semiconductor 71 by portions of insulating layer 72. Sensor electrode 80 is connected by an overlay contact 81 to a gating electrode 82 disposed between the bit generator 77 and the first CCD electrode 34A.

The capacitance between electrodes 25Z and 80 is defined as C_1, and the capacitance between electrode 80 and semiconductor 71 is defined as C_2. The capacitance associated with the depletion region formed under electrodes 25Z and 80 is assumed small with respect to C_1 and C_2. With these definitions, then, the voltage induced on electrode 80 is approximately the applied clock pulse voltage (ϕ_1) if the potential well thereunder is empty (logical "zero" bit). Conversely, if the potential well is nearly full of charge (logical "one" bit) the voltage induced on electrode 80 is approximately ϕ_1 multiplied by the ratio $C_1/(C_1+C_2)$. Remembering that ϕ_1 is a negative voltage and C_1 and C_2 are positive numbers, it is seen that a more negative voltage is induced on electrode 80 if a "zero" is under electrode 25Z than if a "one" is there.

Note that these induced voltages on electrode 80 are coupled directly to and appear upon gating electrode 82, disposed between bit generator 77 and CCD electrode 34A. Note also that the first CCD electrode 34A is connected to the same clock line as is electrode 25Z under which the bits are being sensed. Because of this, a "packet" of holes (logical "one" bit) is transferred from bit generator 77 to the potential well under electrode 34A if a "zero" is at that time under electrode 25Z. Conversely, the capacitance ratio $C_1/(C_1+C2)$ and the spacing of electrode 82 from the semiconductor surface are adjusted such that no holes (logical "zero" bit) are transferred from bit generator 77 if a "one" is at that time under electrode 25Z. This is accomplished, of course, by adjusting the capacitance ratio and the spacing of electrode 82 such that if a "one" is under electrode 25Z, the surface potential under electrode 82 is less negative than $(-V_S)$.

In some uses, it may be desirable to establish a DC bias on gating electrode 82 for optimum operation. This is readily accomplished by additionally connecting gating electrode 82 through a high impedance (not shown) to a DC voltage source (not shown). In this case the time constant associated with the high impedance advantageously is significantly greater than the inverse of the bit transfer rate through the CCD channel so that the pulse voltages induced on sensor electrode 80 can cause gating electrode 82 to vary in response thereto without interference from the DC bias. It will be appreciated that electrodes 80 and 82 thus may still be thought of as "electrically floating" with respect to AC and pulsed signals.

FIG. 6 shows another device which is like that of FIG. 5 except that the sensing function is performed by an electrically floating P-type localized zone 90 disposed adjacent the semiconductor surface under CCD electrode 25Z. The only difference between FIGS. 5 and 6 is that electrically floating sensor electrode 80 has been removed and replaced by an electrical floating localized zone 90 in FIG. 6.

In similar fashion to that described with reference to FIG. 5, voltages are induced on sensor zone 90 in FIG. 6 and are coupled directly to gating electrode 82 which inhibits or allows the transfer of a quantity of charge from bit generator 77. The voltage on zone 90 at any instant is approximately equal to the surface potential induced thereon. This surface potential is approximately equal to ϕ_1 if a "zero" transfers under electrode 25Z as ϕ_1 is applied thereto, and is something less negative than ϕ_1 if a "one" ("packet" of holes) transfers in. If as ϕ_1 is applied a sufficient number of holes flow in to fill the potential well, the surface potential will rise to some maximum value less than zero. The voltage induced on zone 90 when a "one" is present can be readily made to be less than one-third as negative as the voltage induced when a "zero" is present, and this difference is sufficient to cause the desired gating action at electrode 82. Note that as with the structure of FIG. 5, a "one" is gated away from bit generator 77 in FIG. 6 if a "zero" is under electrode 25Z, and a "zero" is gated away if a "one" is under electrode 25Z.

A number of alternatives, modifications and uses will now be described with reference to FIGS. 7—14. Without sacrificing completeness, FIGS. 7—14 are somewhat schematic plan views of CCD structures.

In FIGS. 7—14, solid line patterns depict field plate electrodes disposed over an insulating layer; broken line patterns depict either electrodes disposed within the insulator (such as electrode 80 in FIG. 5) or localized zones in the semiconductor (such as zones 76, 77, and 90 in FIGS. 5 and 6). This mode of illustration is adopted primarily for simplicity and generality, and the devices illustrated thereby will become more clearly understood as the description proceeds.

With reference now to FIG. 7, there is

shown a schematic plan view of a device similar to those shown in FIGS. 5 and 6. In FIG. 7 124Y—126Z represent field plate electrodes at the end of a CCD channel whose information is to be inverted and regenerated, and 134—136A represent field plate electrodes at the beginning of a fresh CCD channel to accept the newly-regenerated bit stream. It will be appreciated that electrodes 124Y—126Z and 134A—136A are analogous to the electrodes 26Y—26Z and 34A—36A, respectively, of FIGS, 5 and 6. As in the previously described FIGS. 1, 2A—2C, 5, and 6, every third CCD electrode is connected to a common one of three clock lines 173—175, to which clock voltages ϕ_1—ϕ_3 (alternately $(-V_1)$, $(-V_3)$, and $(-V_2)$) are applied.

In FIG. 7, 100, disposed under CCD electrode 124Z, represents a sensor electrode similar to either electrode 80 in FIG. 5 or electrode 90 in FIG. 6. As in FIGS. 5 and 6, the sensor electrode 100 is not connected to the clock lines but is coupled by a conductor 181 to a gating electrode 182 which operates as does gating electrode 82 in FIGS. 5 and 6.

176 represents a P-type localized zone connected to a source of negative voltage $(-V_D)$ and adapted to operate as a drain, analogous to zone 76 in FIGS. 5 and 6. 177 represents a P-type localized zone connected to a source of negative voltage $(-V_S)$ and adapted to operate as a bit generator, analogous to zone 77 in FIGS. 5 and 6.

Unlike the apparatus depicted in FIGS. 5 and 6, sensor element 100 in FIG. 7 is disposed under field plate electrode 124Z and is separated from drain 176 by a pair of field plate electrodes 125Z and 126Z, instead of only one. This separation by two electrodes rather than one is not necessary for operability but is advantageous to more effectively decouple and isolate sensor element 100 from the effects of drain 176.

Referring back now to FIGS. 1 and 2A—2C, it will be observed that the "packets" of charge representing information are located only under the electrodes to which $(-V_3)$, the most negative clock voltage, is applied. The other two electrodes of each triplet serve to separate each charge packet from the adjacent packets. Thus, in FIG. 7, it is desired to transfer a packet of charge away from bit generator 177 only when $(-V_3)$ is applied to electrode 124Z (overlying sensor 100) because only then is there a packet of charge (or the absence thereof) representing information to be sensed under electrode 124Z. As a result of this reasoning, the general principle obtains that the field plate electrode (124Z in FIG. 7) overlying the sensor (100 in FIG. 7) will always be connected to the same clock line (173 in FIG. 7) as is the first field plate electrode (134A in FIG. 7) following the gating electrode (182 in FIG. 7) so that information is simultaneously sensed, inverted, regenerated, and transferred to the first field plate (134A in FIG. 7) of the new CCD channel. Also as a result of the above reasoning, it will be appreciated that V_S should be greater than V_1 and V_2 but less than V_3 so that gating electrode 182 will allow charge to be transferred away from bit generator 177 only when $(-V_3)$ is simultaneously applied to electrode 124Z and a "zero" is under electrode 124Z.

With reference now to FIG. 8, the device shown is similar to those of FIGS. 5 and 6 but is adapted for two-phase operation. To this end, field plate electrodes 153Y—154Z represent the end of a CCD channel whose information is to be inverted and regenerated, and field plate electrodes 253A—254A represent the beginning of a new CCD channel to accept the newly-regenerated bit stream. To ensure unidirectionality of charge transfer, these field plate electrodes advantageously are of the type adapted to produce asymmetrical potential wells, as described with reference to FIG. 3.

In FIG. 8 every second one of the field plate electrodes is coupled to a common one of two clock lines 155 and 156. 176 and 177 represent a drain and a bit generator, respectively and as such are coupled to appropriate sources of voltage $(-V_D)$ and $(-V_S)$. A sensing element 100, like either electrode 80 in FIG. 5 or electrode 90 in FIG. 6, is disposed under field plate 153Z and is coupled by a conductor 181 to a gating electrode 182. Where, as here, field plate electrodes of the type shown in FIG. 3 are used, sensor 100 advantageously is disposed only under that part of the appropriate field plate electrode (153Z in FIG. 8) which overlies the thinner dielectric because that is where the charge "packet" is localized, as shown in FIG. 3. In this manner a maximum of induced voltage and a minimum amount of parasitic capacitance are realized. Operation of the device of FIG. 8 will be apparent from the foregoing discussion.

FIG. 9 illustrates another device adapted for two-phase operation and which differs from that of FIG. 8 only in that bit generator 177 is coupled to and therefore driven by the clock line 156, and sensor element 100 is separated from drain 176 by a pair of field plate electrodes 154Z and 153ZZ, rather than just one.

As with the above-described three-phase embodiments, the field plate electrodes (153Z in FIG. 9) under which sensor 100 is disposed must be connected to the same clock line (155 in FIG. 9) as is the first field plate electrode (253A in FIG. 9) following the gating electrode (182). If, as in FIG. 9, the bit generator is to be

driven by a clock line to reduce the number of different conduction paths required, the bit generator (177) must be connected to a different clock line (156 in FIG. 9) than electrodes 153Z and 253A so as to achieve the appropriate voltage relationships. This will be better understood from the following detailed description of a complete cycle of operation of the devices.

First, assume one half-cycle in which

$$\phi_1=(-V_1)$$

is applied to clock line 155 and

$$\phi_2=(-V_2)$$

is applied to clock line 156, where $V_2>V_1$. During this half-cycle the bit to be inverted and regenerated is stored under electrode 154Y. Another bit which has been inverted and regenerated is stored in duplicate, the degraded bit under electrode 154Z and the inverted and regenerated bit under electrode 254A. In this condition no "packet" of positive charge can be transferred from bit generator 177 to field plate electrode 253A regardless of the voltage on gating electrode 182 because the bit generator is more negative ($-V_2$) than electrode 253A.

Now, assume that the clock switches polarity to the other half-cycle in which ϕ_1 becomes ($-V_2$) and ϕ_2 becomes ($-V_1$). As the voltages are changed, each charge "packet" moves one step (one electrode) down in FIG. 9 as indicated by arrows 157 and 257 in the manner described with reference to FIG. 3. The degraded bit under electrode 154Z is transferred to electrode 154ZZ and is swept into drain 176 by ($-V_D$) which is more negative than ($-V_2$), and the inverted replica of this bit is transferred from electrode 254A to the next electrode (not shown) in the regenerated channel. Note that electrode 253A is now more negative ($-V_2$) than bit generator 177 ($-V_1$) so that a packet of positive charge will be transferred to electrode 253A if allowed by gating electrode 182.

As the clock voltages are changed to this second condition, the incoming bit moves from electrode 154Y to electrode 153Z where it is detected by sensor 100. As described with reference to FIGS. 5 and 6, sensor 100 and gating electrode 182 are adapted such that a "packet" of charge ("one") is allowed to transfer from bit generator 177 to electrode 253A if the absence of a "packet" of charge ("zero") is detected by sensor 100, and no charge ("zero") is permitted to transfer if a "one" is detected by sensor 100.

Thus, no bit is allowed to transfer to electrode 253A during the first half-cycle because of the voltage relationship between bit generator 177 and electrode 253A, and during the other half-cycle the voltage relationship between generator 177 and electrode 253A is reversed such that a "one" is permitted to transfer therebetween only if a "zero" is at the sensor.

It will be appreciated that the device of FIG. 8 also could be operated with bit generator 177 driven by clock line 156. The three-phase device of FIG. 7 also could be operated with bit generator 177 driven by clock line 175 provided the clock pulse is suitably shaped, e.g., a sine wave, so that the appropriate voltage relationships are maintained between bit generator 177, gating electrode 182, and field plate electrode 134A.

FIG. 10 shows another device adapted for two phase-operation. The device is similar to that shown in FIG. 8 except for the means for generating bits, and, accordingly, the description of FIG. 10 will be abbreviated and directed primarily to the different features. As in FIG. 8, the device includes a P-type localized drain 176 connected to a suitably negative source of potential ($-V_D$) and a P-type localized zone 177 for providing a source of positive charge carriers. Unlike in FIG. 8, however, source 177 in FIG. 10 is connected to electrical ground and is spaced from gating electrode 182 by a field plate electrode 105 and an electrically floating P-type localized zone 178.

In operation, negative voltages applied to field plate electrode 253A and negative voltages induced on gating electrode 182 cause charge to be transferred away from zone 178 to field plate 253A which, in turn, causes a negative potential to be induced on zone 178. Then, with zone 178 negative and zone 177 at ground, and after gating electrode 182 has been turned off, a negative "priming pulse" applied to electrode 105 for a given time allows a relatively precisely determinable amount of charge to transfer from zone 177 to zone 178.

This is termed "priming" because it enables the preliminary storage in zone 178 of a relatively precise amount of charge which can then be gated as a "one" to electrode 253A. This availability of a precisely predictable amount of charge is desirable because the noise margin of any system is dependent on, among other things, the degree by which each "one" bit is like the other "one" bits and by which each "zero" is like the other "zeros".

Turning now to FIGS. 11—13, there are shown a variety of devices adapted for performing logic functions.

FIG. 11 is a schematic plan view of a device adapted for performing a logical NOR operation, the truth table for which is shown in the lower right-hand corner of FIG. 11. The upper portion of the figure represents two CCD channels A and B coupled to a common pair of clock lines 155 and 156 for

propagating information downward, as indicated by arrows 157A and 157B. Electrodes 154AY, 153AZ, 154AZ, 154BY, 154BZ, and 154BZ are field plate electrodes in the respective channels, analogous to electrodes 154Y, 153Z, and 154Z in FIGS. 8—10. The lower portion of the figure, i.e., field plate electrods 253CA and 253CB, represents the beginning of a new CCD channel, labelled C, to accept the regenerated bits resulting from the NOR operation. 276 represents a P-type localized zone connected to a source of negative voltage ($-V_D$) and adapted to operate as a drain, analogous to zones 76 and 176 in the preceding figures. 277 represents a P-type localized zone adapted to operate as a bit generator in the manner described with reference to zone 177 in FIG. 9 and as such is connected to one of the clock lines 156.

A pair of separate sensor elements 100A and 100B are disposed under electrodes 153AZ and 153BZ in channels A and B. Each of the sensors is connected in the manner described with reference to the preceding figures by conductors 181A and 181B to separate ones of a pair of gating electrodes 182A and 182B. As shown, for a NOR element the gating electrodes are disposed in series with respect to bit generator 277 and with respect to the first field electrode 253CA of channel C.

In operation separate bit streams of information are transferred simultaneously along channels A and B in response to clock signals applied to clock lines 155 and 156. The bit streams are synchronized such that bits move under electrodes 153AZ and 153BZ simultaneously. If either sensor 100A or 100B detects a "one", there will be induced on the gating electrode to which that sensor is coupled a voltage sufficient to prohibit the transfer of charge thereunder. Thus, it will be seen that, in accordance with the truth table in FIG. 11, a "one" will be allowed to transfer from bit generator 277 to field plate electrode 253CA only if a "zero" exists at both sensors 100A and 100B.

At this point it should be appreciated that within the NOR element shown in FIG. 11, gating electrodes 182A and 182B perform a logical AND function, i.e., only if a potential well is induced under both of them can a "packet" of charge be transferred from bit generator 277 to field plate 253CA. This leads to the more general teaching that wherever an AND function is desired in a CCD system it can be accomplished in part by disposing a plurality of gating electrodes in series.

FIG. 12 shows a device adapted for performing a logical NAND operation, the truth table for which is shown in the lower right-hand corner of the figure. The apparatus of FIG. 12 differs from that shown in FIG. 11 only in that gating electrodes 182A and 182B are disposed in parallel with respect to bit generator 277 and CDD electrode 253CA. With this disposition of the gating means charge is prevented from transferring away from bit generator 277 only if a "one" is present at both sensors 100A and 100B. This, of course, is consonant with the NAND truth table in FIG. 12.

At this point it should be appreciated that within the NAND element shown in FIG. 12, gating electrodes 182A and 182B perform a logical OR function, i.e., if a potential well is induced under either of them a packet of charge can be transferred from bit generator 277 to field plate 253A. This leads to the more general teaching that whenever an OR function is desired in a CCD system it can be accomplished in part by disposing a plurality of gating electrodes in parallel.

FIG. 13 shows a device adapted for performing a logical "FAN-OUT" operation, the truth table for which is shown in the lower right-hand corner of the figure. The upper portion of the figure represents a CCD channel, labelled A, coupled to a pair of clock lines 155 and 156 and having information propagating downward, as indicated by arrow 157A. Electrodes 154AY, 153AZ, and 154AZ are field plate electrodes of channel A, analogous to electrodes 154Y, 153Z, and 154Z in FIGS 8—10. The lower portion of the figure, i.e., field plate electrodes 253BA, 254BB, 253CA, and 254CB, represents the beginning of a pair of CCD channels, labelled B and C, to accept the regenerated bits resulting from the "FAN-OUT" operation. 276 and 277 represent a drain and a bit generator, respectively, adapted to operate as described with reference to FIGS. 11 and 12.

A sensor 100A is disposed under electrode 153AZ and is coupled by conductors 181B and 181C to a pair of gating electrodes 182B and 182C. From the description hereinabove, it will be appreciated that whenever a "zero" is present at sensor 100A a "one" will be gated by electrode 182B from bit generator 277 into channel B and another "one" will be gated into channel C. Conversely, when a "one" is present at sensor 100A, "zeroes" will be gated into channels B and C.

Of course, "FAN-OUT" can also be accomplished in a variety of other ways besides the one shown in FIG. 13. In many applications, for example, it may be advantageous to connect the sensor to a single gating electrode and to merge field plate electrodes 253BA and 253CA (FIG. 13) into one larger electrode so as to minimize parasitic capacitive loading on the sensor.

It will be appreciated by those skilled in art that modifications may be made to the devices described.

For example, throughout this description the semiconductivity types may be reversed

as desired, provided a corresponding reversal of voltage polarities also is made.

Also, of course, the devices shown in FIGS. 11 and 12 are not limited to sensing only a pair of incoming channels but may have a greater plurality of incoming channels, provided a sensor is disposed in each one and each sensor is coupled to a separate serially disposed or parallel disposed gating electrode, depending upon the logical operation desired. Also, a "FAN-OUT" such as shown in FIG. 13 is not limited to two output channels but may be extended to a greater number.

Further, it will be appreciated that a pair of inverter-regenerators as described herein may be connected in tandem such that the regenerated pulse is inverted twice and therefore restored to a regenerated replica. An example of where such an arrangement might find use is shown schematically in FIG. 14. In FIG. 14, channels 300 and 301 represent part of a serpentine CCD channel, the flow of information in which is represented by the arrows. In channel 300 a sensor 302 (of either type described in FIGS. 5 and 6) detects incoming degraded signals and induces a corresponding voltage on a gating electrode 303. After the incoming signals are sensed, they are collected in the manner described hereinabove by a drain, such as 76 in FIGS. 5—6, represented by the square broken line 304. Another square broken line 305 represents a source or bit generator, such as feature 77 in FIGS. 5—6. Thus, the combination of 302, 303, 304, and 305 represents an inversion-regeneration element.

Bits from source 305 are gated by electrode 303 to another field plate electrode 306. Another sensor 307 is connected to a field electrode 308 disposed at the beginning of channel 301. After the bits from source 305 have been detected by sensor 307, they are collected by a second drain 309. A second source represented by broken line 310 serves as a bit generator, the bits from which are gated by electrode 308 into channel 301. Although this double inversion is seldom, if ever, necessary, it may be desirable in relatively short serpentine datad pattern, if the system designer would rather perform double inversion than account for single state inversion.

It will be appreciated that because NAND and NOR each constitutes a logically independent set, all other logic functions can be readily derived from combinations of either one in accordance with principles well known in the logic arts.

Also, of course, it will be appreciated that bit generators, sensors, and inversion-regeneration elements described can readily be combined in numerous ways to provide other basic logic functions not expressly discussed herein.

The aforedescribed inversion-regeneration elements and the many and diverse forms thereof can be readily adapted for use in charge transfer devices of the above mentioned "bucket-brigade" type. A basic form of such an adaptation is shown in FIG. 15 and will now be described with reference thereto.

FIG. 15 shows a portion *400* of a charge transfer apparatus including a basic inversion-regeneration element. Element *400* includes a semiconductive bulk portion 401, shown here illustratively as N-type, and a plurality of P-type surface zones. A dielectric layer 402 is disposed over the surface of semiconductor 401. Overlying dielectric layer 402 are a plurality of serially disposed field plate electrodes 401X, 402X, 401Y, 402Y, 401Z, and 402Z which in combination with a corresponding plurality of asymmetrically disposed, underlying, P-type localized zones, represented at 403X, 404X, 403Y, 404Y, 403Z, and 76 represent the end of a "bucket-brigade" channel whose bit stream is to be inverted and regenerated. In like manner, serially disposed field plate electrodes 411A, 412A, and 411B which in combination with a plurality of asymmetrically disposed, underlying P-type localized zones, represented at 413A, 414A, and 413B, represent the beginning of a fresh "bucket-brigade" channel to accept the inverted and regenerated bit stream. As shown, every second one of the aforementioned field plate electrodes is connected to a common one of a pair of clock lines 455 and 456.

As is more fully described in the third of the aforementioned copending patent applications, the preferred direction for information advance is determined by the asymmetry with which each pair of underlying zones is overlapped by the field plate electrodes. More specifically, it should be noted in FIG. 15 that each of the aforementioned electrodes overlaps a portion of two separate underlying zones and that in the incoming channel whose bit stream is to be regenerated and in the outgoing channel which accepts the inverted and regenerated bit stream, the greater overlap is to the right. This asymmetry in overlap causes preferential direction of information advance because of the resulting asymmetry incapacitive coupling between the field plate electrodes and the underlying zones.

The reference numerals used in FIGS. 5 and 6 have been repeated in FIG. 15, where appropriate. Accordingly, in FIG. 15, P-type zone 76 represents a drain zone for disposing of degraded bits after detection, and P-type zone represents an independent source zone, i.e., a bit generator, from which injected mobile charge carriers are gated selectively to produce the regenerated bit stream. Note that, as in FIG. 6, drain and source zones 76 and 77 are conductively connected through

electrodes 78 and 79, respectively, to sources of negative potential ($-V_D$) and ($-V_S$), respectively. As in the apparatus of FIGS. 5 and 6, ($-V_D$) advantageously is selected to maintain P-type zone 76 more negative than the most negative surface potential induced on adjacent zone 403Z so that degraded bits can always transfer from zone 403Z into drain 76 and thus be collected and destroyed, i.e., conducted to ground. Also ($-V_S$) is selected to maintain bit generator zone 77 sufficiently negative that only enough holes are drawn selectively therefrom to partially fill the potential wells formed in zone 408 without flooding the new channel.

In operation, zone 404Y operates as a sensor zone, and voltages induced thereon are coupled directly through electrode 405 and conductor 406 to a gating electrode 407, disposed between bit generator 77 and zone 408. In similar fashion to that described with reference to FIG. 6, the voltage on zone 404Y at any instant is approximately equal to the surface potential induced thereon. This surface potential is approximately equal to the clock line voltage (ϕ_1) if a "zero" transfers into sensor zone 404Y as ϕ_1 is applied to electrode 402Y, and is something less negative than ϕ_1 if a "one" ("packet" of holes) transfers in.

If as ϕ_1 is applied a sufficient number of holes flow in to partially fill the potential well, the surface potential of zone 404Y will rise to some maximum value less than zero. As with the devices of FIGS. 5 and 6, the voltage induced on sensor zone 404Y when a "one" is present readily can be made to be less than one-third as negative as the voltage induced when a "zero" is present, and this difference is sufficient to cause the desired gating action at electrode 407. Thus, clearly, in a fashion analogous with that of FIGS. 5 and 6, the parasitic capacitance and spacing of electrode 407 from the surface of semiconductor 401 can be adjusted such that a "one" is gated by electrode 407 from source 77 to zone 408 if a "zero" is in sensor zone 404Y, and a "zero" is gated by electrode 407 from source 77 to zone 408 if a "one" is in sensor zone 404Y.

As discussed above with reference to FIGS. 5 and 6, it may be desirable in some situations to estabish a DC bias on the gating electrode (407 in FIG. 15) and/or on the sensor (404Y in FIG. 15) for optimum operation. This is readily accomplished by connecting conductor 406 through a high impedance to a DC voltage source. This is depicted schematically in FIG. 15 by a phantom resistor 409 connected between conductor 406 and a DC bias source ($-V_R$). Again the time constant associated with the high impedance (409) advantageously is significantly greater than the inverse of the bit transfer rate through the "bucket-brigade" channel so that the pulse voltages can cause gating electrode 407 to vary in response thereto without interference from the DC bias.

It will be appreciated that the "bucket-brigade" shift register and inversion-regeneration element shown in and described with reference to FIG. 15 may readily be be adapted for all the many and diverse uses depicted in and suggested with respect to FIGS. 7—14 and the devices discussed in greater detail above.

Other devices in accordance with the invention will now be described with reference to FIGS. 16 to 20. Referring now to FIG. 16, a plurality of serially disposed field plate electrodes 523A, 524A, 523B, 524B, and 523C represent the end of a CCD channel whose bit stream is to be inverted and regenerated, and serially disposed field plate electrodes 533A, 534A, 533B, 534B, and 533C represent the beginning of a fresh CCD channel to accept the inverted and regenerated bit stream. As shown, every second one of these electrodes is connected to a common one of a pair of clock lines 525 and 526. Further, it will be assumed that these electrodes are asymmetrical in such a direction to cause information to be transferred to the right in the input or degraded channel (as indicated schematically by arrow 522) and to cause information to be transferred to the left in the output or lower channel (as indicated schematically by arrow 535).

Broken line patterns 541, 542, and 543 depict localized P-type semiconductive zones disposed beneath the surface of the insulating layer. Solid line patterns 524 and 532 represent field plate electrodes overlying the insulating layer. Localized zones 541—543 in combination with field plate control electrodes 524 and 532 represent the inversion-regeneration element.

As will be described in more detail immediately below, zone 541 is adapted for sensing information in the degraded channel and, accordingly, is disposed adjacent the last electrode 523C at the end of the degraded channel. Zone 542 is spaced from zone 541 and the space therebetween is bridged by field plate control electrode 524 so that zones 542 and 541 can effectively be coupled together by applying a voltage to electrode 524 sufficient to invert the surface between zones 542 and 541.

In operation zone 542 is held at a fixed negative potential indicated by ($-V_R$) in the figure. Zone 541 operates to sense "packets" of charge which sequentially are transferred under electrode 523C and the voltage thereby induced on zone 541 by the incoming "packets" of charge is conductively coupled directly to field plate electrode 532 by a metallic overlay 544.

Zone 543 represents an independent source

of charge carriers which are gated under electrode 533A or inhibited from being transferred thereunder, depending on the voltage induced on field plate electrode 532.

Accordingly, as shown, field plate control electrode 532 is disposed between source 543 and electrode 533A (the first electrode in the regenerated channel) so that zone 543 can be effectively coupled to the potential well under electrode 533A by applying a voltage to control electrode 532 sufficient to invert the semiconductor surface thereunder. As shown, source 543 and field plate electrode 524 are connected together and to clock line 526, i.e., the one other than that to which electrodes 523C and 533A are connected.

Advantageously $(-V_R)$ is selected to be more negative than the most negative $(-V_2)$ of the pair of voltages alternately applied to the clock lines. In this case, when $(-V_2)$ is applied to clock line 526 and $(-V_1)$ is applied to clock line 525, charge "packets" in the channels are located under electrodes 524A, 524B, 534A, and 534B. Because field plate 524 is connected to clockline 526 and because $(-V_R)$ is at least as negative as $(-V_2)$, a potential of approximately $(-V_2+V_T$ is induced on floating sensor zone 541. Of course, this same voltage also is coupled to and appears upon gating electrode 532.

Physically this voltage is induced on zone 541 because positive charge carriers (holes) are drawn from zone 541 through the inverted region under electrode 524 into the more negative zone 542. It will be appreciated that zone 542 is thus adapted to operate in similar fashion as the drain in an insulated gate field effect transistor (IGFET). In this condition a heavily inverted region is formed under gating electrode 532 but no positive charge carriers are transferred from source 543 to electrode 533A because source 543 is more negative than electrode 533A.

At the next half of the clock cycle (when

$$\phi_1=(-V_2)$$

and

$$\phi_2=(-V_1))$$

sensor 541 is decoupled from drain 542 because of the less negative voltage applied to coupling electrode 524. Also of importance is the fact that source 543 is now less negative than electrode 533A so that positive charge carriers can be transferred to electrode 533A unless inhibited by the action of gating electrode 532.

As the clock voltages are switched into this last-described condition, the charge "packets" representing information are transferred from the electrodes numbered 524 and 534 under electrodes numbered 523 and 533, respectively. If a logical "1" (a "packet" of charge) is transferred from electrode 524B to electrode 523C, most of that charge is drawn into zone 541 and serves to discharge the negative potential stored there. The potentials and the spacing of gating electrode 532 from the semiconductor surface are adjusted such that after a "1" (a "packet" of charge) is drawn into sensor 541, the voltage remaining on gating electrode 532 is insufficiently negative to allow the transfer of charge from source 543 to electrode 533A. Thus, as a "1" is transferred under electrode 523C, a "0" appears under electrode 533A.

Conversely, if a "0" (absence of a "packet" of charge) is transferred under electrode 523C the voltage on sensor 541 will not be discharged and the voltage on gating electrode 532 will remain sufficiently negative to allow a "packet" of charge to transfer from source 543 to electrode 533A. Thus, as a "0" is transferred under electrode 523C, a "1" appears under electrode 533A.

At the next reversal of the clock voltages (when

$$\phi_1=(-V_1)$$

and

$$\phi=(-V_2))$$

any excess positive charge is drawn from sensor 541 into drain 542. In this manner the voltage on sensor 541 is reset to a predetermined voltage prior to accepting each incoming degraded bit. Because of this reset feature which causes the sensor to start at the same potential when accepting an incoming bit, the inversion-regeneration element offers improved sensitivity and operating noise margin.

For a more complete understanding of the device depicted schematically in FIG. 16, FIG. 17 shows a cross-sectional view taken along lines 17—17 in FIG. 16. Reference numerals have been repeated to indicate corresponding elements where appropriate. In FIG. 17, P-type localized sensor zone 541 is shown contacted electrically by a low resistance electrode 527 (not shown in FIG. 16), and drain zone 542 is shown contacted electrically by a similar low resistance electrode 528 (also not shown in FIG. 16). The other features will be understood from a comparison of the two figures. It should be noted that control electrode 524 is disposed only over the thinner portion of dielectric layer 512, i.e., control electrode 524 need not be asymmetrically disposed like electrodes 524B and 524C. Likewise gating electrode 532 also need not be asymmetrical, but advantageously is disposed over the thinner portion of dielectric laver 512 between zone 543 and electrode 533A.

Although it will be appreciated that a wide variety of operating voltages may be used with

the above-described apparatus, we have found the structure to be operative with

$(V_1)=6$ volts,

$(V_2)=10$ volts,

and

$(V_R)=12$ volts

with a structure in which the thinner portion of dielectric portion 512 was about 1000 Å. It will not usually be advantageous to decrease (V_1) below about 6 volts, but operation in some instances may be enhanced by increasing (V_2) up to as much as 30 volts or greater, in which cases, of course, the (V_R) would be increased correspondingly to be somewhat greater than (V_2).

The rate of charge transfer from zone 543 to electrode 533A to represent a "1" is limited by the voltage at that time existing on gating electrode 532. The voltage on gating electrode 532 may be less negative than ($-V_R$) because of parasitic effects and because each degraded "0" sensed by sensor 541 contains some positive charge which serves to partially discharge the voltage thereon. The net effect is to cause the transfer of a "1" containing less charge than might be desired into the potential well under electrode 533A.

The rate of charge transfer from zone 543 to electrode 533A to represent a "1" also is limited by the instantaneous difference between the potential on zone 543 (the source) and the surface potential under electrode 533A. Unfortunately, this potential difference monotically decreases as charge transfers into the potential well under electrode 533A. Because of this decrease in potential difference, the rate of charge transfer also decreases as charge is transferred. The net effect of this limitation also is to cause the transfer of a "1" containing less charge than might be desired into the potential well under electrode 533A.

Inasmuch as these are voltage limitations rather than limitations on the amount of charge available to be transferred, they can be alleviated by making the first electrode following the gating electrode larger than the other electrodes. Because operation is essentially capacitively coupled transfer of charge, the surface potential under the bigger electrode (bigger capacitance) decreases less rapidly than would the surface potential under a smaller electrode (smaller capacitance). In accordance with this principle, the size of this first electrode can be adjusted relative to the size of the other electrodes to compensate for the aforesaid predictable voltage limitations so that the desired amount of charge is transferred under the first and successive electrodes to represent a "1".

This is represented schematically in FIG. 18 which shows apparatus identical to that of FIG. 16, except that electrode 533A (now denoted 533A') is represented as being twice as large as the other electrodes. It will be appreciated that the principle applied to achieve the improvement shown in FIG. 18 is not limited to inversion-regeneration elements but may be applied in general in such devices in accordance with capacitive division techniques well known in the art.

Although the foregoing has been directed primarily to an inversion-regeneration element in two-phase charge coupled devices, it will be appreciated that the inverter-regenerator can be readily adapted for use in three-phase and four-phase devices in accordance with the principles described with reference to the latter two-phase embodiment.

Further, it will be appreciated that the afore-described inversion-regeneration element can be readily adapted for use in charge transfer devices of the "bucket-brigade" type described in the third of the above-identified copending applications. One form of such an adaptation is shown in FIGS. 19 and 20 and will now be described with reference thereto.

FIG. 19 shows a portion 50 of a "bucket-brigade" type of charge transfer device employing a basic inversion-regeneration element. In FIG. 19 a plurality of serially disposed field plate electrodes 551A, 552A, 551B, 552B, and 551C in combination with a plurality of asymmetrically disposed, underlying P-type localized zones, represented at 553A, 554A, 553B and 554B, represent the end of a "bucket-brigade" channel whose bit stream is to be inverted and regenerated. In like manner, serially disposed field plate electrodes 561A, 562A, 561B, 562B, and 561C in combination with a plurality of asymmetrically disposed, underlying P-type localized zones represented at 565A, 566A, 565B, 566B. and 565C, represent the beginning of a fresh "bucket-brigade" channel to accept the inverted and regenerated bit stream. As shown, every second one of the aforementioned field plate electrodes is connected to a common one of a pair of clock lines 567 and 568.

As indicated schematically by arrows 569 and 570, respectively, the device is adapted so that information is transferred to the right in the input or degraded channel and to the left in the output or regenerated channel. As is described in the third of the above-mentioned copending applications, the preferred direction for information advance is determined by the asymmetry with which the underlying zones are overlapped by the field plate electrodes. More specifically, it should be noted in FIG. 19 that each of the aforementioned electrodes overlaps a portion of two separate underlying zones and that in the upper channel the greater overlap is on the right while in the lower channel the

greater overlap is to the left. This asymmetry in overlap causes preferential information advance because of the resulting asymmetry in capacitive coupling between the field plate electrodes and the underlying zones.

The reference numerals used in FIG. 16 for the features included in the inversion-regeneration element have been repeated in FIG. 19. Accordingly, in FIG. 19, 541 represents the sensor zone and 542 represents the reference zone to which sensor zone 541 is coupled for resetting by applying a suitable voltage to a bridging field plate electrode 524. 543 represents the independent source of carriers which are gated into the lower channel by voltages induced on field plate electrode 532. Note, however, the inclusion of an additional P-type localized zone 563 for bridging the gap between gate 532 and electrode 561A.

In operation, analogous to the operation described above with reference to FIG. 16, zone 542 is held at a fixed negative potential indicated by $(-V_R)$ in FIG. 19. Zone 541 senses "packets" of charge which are sequentially transferred under the last "bucket-brigade" electrode 551C, and the voltage thereby induced on zone 541 by the incoming "packets" of charge is conductively coupled directly to gate electrode 532 by conductor 544. As shown, source 543 and field plate electrode 524 are connected together by conductors 544A, 544B, and 544C, e.g., metallic overlays, and to clock line 568, i.e., the clock line other than the one to which "bucket-brigade" electrodes 551C and 561A are connected.

Of course, source 543 need not be connected to a clock line but instead may be driven by an independent pulse generator which is synchronized with the clock line pulses to realize greater flexibility in driving the source 543 but at the expense of greater complexity. This option is represented schematically in FIG. 19. As shown, phantom line 544C indicates that electrode 524 and source 543 are connected together and to a common clock line, 568. If the option is exercised, the connection between 544A and 544B would not be made, and, instead, conductor 544B would be connected to the independent pulse generator, labelled "pulse means" in FIG. 19.

It will be appreciated that this option also may be used with the previous charge coupled device. Further, it will be appreciated that if other than two-phase, e.g., a three-phase or four-phase, charge coupled device is used, the source 543 need not be pulsed, but instead may be connected to a DC voltage. In this case, selective introduction of bits into the regenerated channel is accomplished by field plate electrodes without the need for a pulsed source.

Advantageously, $(-V_R)$ is selected to be more negative than the most negative $(-V_2)$ of the pair of voltages alternately applied to the clock lines. When $(-V_1)$ is applied to clock line 567 and $(-V_2)$ is applied to clock line 568, bits (charge "packets" or the absence thereof) in the "bucket-brigade" channels are located in zones 554A, 554B, 566A, and 566B under electrodes 552A, 552B, 562A, and 562B, respectively. Because field plate 524 is connected to clock line 568 and because $(-V_R)$ is at least as negative as $(-V_2)$, a potential of approximately $(-V_2)+V_T$ is induced on floating sensor zone 541. Physically this voltage is induced on zone 541 because positive charge carriers (holes) are drawn from zone 541 through the inverted region under electrode 524 into the more negative zone 542. It will be appreciated that zone 542 is thus adapted to operate in similar fashion as the drain in an insulated gate field effect transistor (IGFET).

Because of the conductive coupling 544 between zone 541 and gating electrode 532, the potential of zone 541 also appears on gating electrode 532. In this condition a heavily inverted region is formed under gating electrode 532 but no positive charge carriers are transferred from source 543 to zone 563 under electrode 532 because source 543 is more negative than zone 563.

That source 543 is more negative than zone 563 in this half of the clock cycle is readily seen from the following consideration. In this half of the clock cycle the more negative potential $(-V_2)$ is applied to source 543 and the less negative potential $(-V_1)$ is applied to electrode 561A. Because of the capacitive overlap between electrode 561A and zone 565A and because electrode 561A acts as a bridging field plate electrode causing zones 563 and 565A to be coupled together by a heavily inverted region at the previous half of the clock cycle, the potential of zones 563 and 565A both are driven to a potential nearly equal to $(-V_1)$ as the clock switches into this half cycle. Thus, source 543 is more negative $(-V_2)$ than zone 563 (nearly $(-V_1)$) during this half cycle.

From the foregoing analysis of the relation between zones 563 and 565A, it will be appreciated that they need not be separate zones (as shown in FIG. 19) but instead may be merged together into one common zone. This merger may be a problem for some applications, however, because of the resulting increase in parasitic capacitance from the single longer zone.

Continuing now with the description of operation, at the next half of the clock cycle (when

$$\phi_1=(-V_2)$$

and

$$\phi=(-V_2))$$

sensor 541 is decoupled from drain 542 because of the less negative voltage applied to coupling electrode 524. Also of importance is the fact that source 543 is now less negative than zone 563 and 565A so that positive charge carriers can be transferred to zone 565A unless inhibited by the action of gating electrode 532.

As the clock voltages are switched into this last-described condition, the charge representing information are transferred from the zones numbered 554 and 566 to the zones numbered 553 and 565, respectively. If a logical "1" (a packet of charge) is transferred from zone 554B into zone 541, that charge serves to discharge the negative potential stored there. The potentials and the spacing of gating electrode 532 from the semiconductor surface are adjusted such that after a "packet" of charge is drawn into sensor 541 the voltage remaining on gating electrode 532 is insufficiently negative to allow the transfer of charge from source 543 to zone 565A. Thus, as a "1" is transferred into sensor zone 541, a "0" appears in zone 565A.

Conversely, if a "0" (absence of a "packet" of charge) is transferred into sensor zone 541, the voltage on sensor 541 will not be discharged and the voltage on gating electrode 532 will remain sufficiently negative to allow a "packet" of charge to transfer from source 543 to zone 563 and further into zone 565A. Thus, as a "0" is transferred into zone 541, a "1" appears in zone 565A.

At the next reversal of the clock voltages (when

$$\phi_1=(-V_1)$$

and

$$\phi_2=(-V_2))$$

any excess positive charge is drawn from sensor 541 into drain 542. In this manner the voltage on sensor 541 is reset to a predetermined voltage prior to accepting each incoming degraded bit. Because of this reset feature which causes the sensor always to start at the same potential when accepting an incoming bit, the inversion-regeneration element offers improved sensitivity and operating noise margin.

For a more complete understanding of the device depicted schematically in FIG. 19, FIG. 20 shows a cross-sectional view taken along lines 20—20 in FIG. 19. Reference numerals have been repeated to indicate corresponding elements where appropriate. In FIG. 20, P-type localized sensor zone 541 is shown contacted electrically by a low resistance electrode 527 (not shown in FIG. 19), and drain zone 542 is shown contacted electrically by a similar low resistance electrode 528 (also not shown in FIG. 19). The other features will be understood from a comparison of the two figures.

It will be appreciated that a wide variety of operating voltages may be used with the above-described device. We have found the structure to be operative, for example, with

$$(V_1)=6 \text{ volts},$$

$$(V_2)=10 \text{ volts},$$

and

$$(V_R)=12 \text{ volts}$$

with a structure in which the dielectric portion 512 was about 1000 Å thick. It will not usually be advantageous to decrease (V_1) below about 6 volts, but operation in some instances may be enhanced by increasing (V_2) up to as much as 30 volts or greater, in which cases, of course, the (V_R) would be increased correspondingly to be somewhat greater than (V_2).

Again, it will be appreciated that a pair of inverter-regenerators described with reference to FIGS. 16 to 20 may be cascaded such that the regenerated pulse is inverted twice and therefore restored to a regenerated replica of the original.

Further, it will be appreciated that devices described with reference to FIGS. 16 to 20 may be readily adapted to perform logic operations in a manner similar to that already described with reference to FIGS 11 to 13.

It will be appreciated that suitably injecting Schottky-barrier diodes and/or other rectifying barrier means can be substituted for any or all of the zones in the above-described devices as an alternative means for providing the collecting and injecting functions.

It will be appreciated that the invention will find application in charge transfer devices wherein the storage medium is other than semiconductive. Such transfer devices are described, for example, in the first of the above identified patent applications. In such devices the storage medium may, for example, be an insulator which is not characterized by any one particular conductivity type. In certain of these insulators, zones suitable for injection and collection of carriers can be formed. In others, suitable zones cannot readily be formed and in such cases, the required injection and collection of carriers can be achieved by substituting injecting contacts, for example of the type described in the latter copending application, for the zones. These contacts, formed with the surface of the storage medium, may be substituted for the zones in the inversion-regeneration elements in accordance with principles well known in the art.

WHAT WE CLAIM IS:—

1. A charge transfer device wherein, in use, a localised region of stored charge carriers is transferable along a portion of a suitable storage medium by the application of suitable potentials to a plurality of electrodes associated with a surface of said medium, said device including regeneration means comprising means for detecting the amount of charge stored at a predetermined location in said medium, means for disposing of detected charge carriers, means for injecting charge carriers at another location in said medium, and gating means coupled to said detection means for controlling the transfer of newly-injected carriers away from said injection means in dependence upon charge detected at said predetermined location.

2. A device as claimed in claim 1 wherein said storage medium includes a semiconductor body of a first type semiconductivity.

3. A device as claimed in claim 2 wherein said detection means comprises a floating conductive electrode insulated from said surface.

4. A device as claimed in claim 2 wherein said detection means includes a zone of a second type semiconductivity disposed in said body and adjacent to one of said electrodes for sensing the number of charge carriers under said one electrode.

5. A device as claimed in claim 3 or 4 wherein said injection means includes a zone of a second type semiconductivity disposed in said body.

6. A device as claimed in claim 5 including means for applying a bias potential to said injection means zone.

7. A device as claimed in claim 6 wherein the bias potential is a DC bias potential.

8. A device as claimed in any one of claims 2 to 7 wherein said plurality of electrodes is serially disposed, and there is provided a further plurality of serially disposed electrodes associated with said surface for transferring a localised region of charge carriers, and a pair of conduction paths, alternate electrodes in said plurality and said further plurality being connected to one of said pair and the other electrodes in said pluralities being connected to the other one of said pair, said regeneration means being interposed between the end of said plurality of serially disposed electrodes and the start of said further plurality of serially disposed electrodes.

9. A device as claimed in claim 2 having a plurality of channels along which localised regions of charge carriers are transferable each of said channels being defined by a respective plurality of serially-disposed electrodes, and wherein said detection means includes a plurality of separate detection means each being disposed for detecting charge carriers at a predetermined location in a respective channel, and said gating means includes a plurality of means disposed in series with respect to said injection means whereby, in use, carriers are transferable from said injection means only if less than a predetermined number of carriers exist at each of said predetermined locations, whereby said device is operable to provide a logical NOR-function.

10. A device as claimed in claim 2 having a plurality of channels along which localised regions of charge carriers are transferable each of said channels being defined by a respective plurality of serially-disposed electrodes, and wherein said detection means includes a plurality of separate detection means each being disposed for detecting charge carriers at a predetermined location in a respective channel, and said gating means includes a plurality of means disposed in parallel in relation to said injection means whereby, in use, carriers are not transferable away from said injection means only if greater than a predetermined number of carriers exist at each of said predetermined locations, whereby said device is operable to provide a logical NAND-function.

11. A device as claimed in claim 2 wherein said storage medium includes a plurality of spaced localised zones of a second type semiconductivity disposed adjacent said surface of said body and asymmetrically with respect to said plurality of electrodes such that each electrode extends over the space between a pair of said zones and over one zone of said pair of zones more than over the other zone of said pair of zones.

12. A charge transfer device wherein, in use, a localised region of stored charge carriers is transferable along a portion of a suitable storage medium by the application of suitable potentials to a plurality of electrodes associated with a surface of said medium, said device including regeneration means comprising means for detecting the amount of charge stored at a predetermined location in said medium, means for prebiasing the detection means to a fixed reference level prior to said detecting, means for injecting charge carriers at another location in said medium, and gating means coupled to said detection means for controlling the transfer of newly-injected carriers away from said injection means in dependence upon charge detected at said predetermined location.

13. A device as claimed in claim 12 wherein said storage medium includes a semiconductor body of a first type semiconductivity.

14. A device as claimed in claim 13 wherein said detection means includes a first zone of a second type semiconductivity in said body and adjacent to one of said plurality of electrodes for sensing the number of charge carriers under said one electrode, said

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pre-biasing means includes a second zone of the second type semiconductivity in said body and spaced from said first zone, and a first control electrode disposed over and insulated from at least part of the surface of said medium between said first and second zones, said injection means includes a third zone of the second type semiconductivity in said body and spaced from another of said plurality of electrodes, and said gating means includes a second control electrode disposed over and insulated from at least part of the surface of said medium between said injection means and said other electrode and conductively connected to said first zone.

15. A device as claimed in claim 14 wherein said third zone is conductively connected to said first control electrode.

16. A device as claimed in claim 14 or 15 including means for applying a bias potential to said second zone.

17. A device as claimed in claim 16 wherein the bias potential is a DC bias potential.

18. A device as claimed in claim 16 or 17 including means for sequentially applying a plurality of differing potentials to said first control electrode.

19. A device as claimed in any one of claims 14 to 18 wherein there is provided a pair of conduction paths, each alternate electrode in said plurality of electrodes being connected to one of said pair, and the other electrodes in said plurality of electrodes being connected to the other one of said pair, said first control electrode being connected to the one of said pair to which the electrode adjacent the first zone is not connected.

20. A device as claimed in any one of claims 14 to 19 wherein said other electrode is conductively connected to said one electrode.

21. A device as claimed in any one of claims 14 to 20 wherein said other electrode is larger than the other ones of said plurality of electrodes.

22. A device as claimed in any one of claims 13 to 21 wherein said storage medium includes a plurality of spaced localized zones of second type semiconductivity disposed adjacent said surface of said body and asymmetrically with respect to said plurality of electrodes such that each of said plurality of electrodes extends over the space between a pair of said localized zones and over one zone of said pair of zones more than over the other zone of said pair of zones.

23. A charge transfer device substantially as herein described with reference to any one of figs. 5 to 14 of the accompanying drawing.

24. A charge transfer device substantially as herein described with reference to fig. 15 of the accompanying drawing.

25. A charge transfer device substantially as herein described with reference to figs. 16 and 17 or to fig. 18 of the accompanying drawing.

26. A charge transfer device substantially as herein described with reference to figs. 19 and 20 of the accompanying drawing.

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