cutting tool 148 to separate the individual semiconductor die 124 into FO-WLCSP 150. Saw blade or laser cutting tool 148 can use a single cut or step cut.

FIG. 5 shows FO-WLCSP 150 after singulation. Contact pads ~~132~~126, RDL 142, and bumps 146 provide electrical connection to the circuits on active surface ~~130~~128. The insulating layer 136 is formed prior to RDL 142 and covers saw street 134 and substrate edge 135, less channel 140, to reduce out-gassing from molding area 138. The insulating layer 136 improves contact resistance in PVD for fan-out edge pads and plasma stability during oxide etching. The insulating layer 136 also reduces particles and other contaminants from molding area 138 during singulation.

FIGs. 6a-6d illustrate, in relation to FIGs. 2 and 3a-3c, a process of forming an insulating layer in a net pattern over the saw street and around the substrate edge. FIG. 6a shows substrate 160 with embedded semiconductor die 164, similar to FIG. 4c. Semiconductor die 164 have active surface 170 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface 170 to implement analog circuits or digital circuits, such as DSP, ASIC, memory, or other signal processing circuit. Semiconductor die 164 may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing.

An insulating or dielectric layer 174 is formed over active surface 170 and contact pads 172 using PVD, CVD, printing, spin coating, spray coating, or thermal oxidation.

## Claims

What is claimed:

1. A semiconductor device, comprising:

a plurality of semiconductor die;

a first insulating layer formed over the semiconductor die;

an encapsulant deposited around the semiconductor die;

a second insulating layer formed over ~~the encapsulant and semiconductor die~~the first insulating layer, encapsulant, and semiconductor die and directly over a saw street between the semiconductor die, wherein the second insulating layer includes a pattern comprising at least three portions of a material of the second insulating layer;

a conductive layer formed over the second insulating layer; and

a third insulating layer formed over the second insulating layer and conductive layer.

2. The semiconductor device of claim 1, wherein the pattern includes ~~further including~~ a channel in the second insulating layer around the semiconductor die.

3. The semiconductor device of claim 1, wherein the pattern includes ~~further including~~ a net pattern in the second insulating layer around the semiconductor die.

4. The semiconductor device of claim 1, wherein the ~~second insulating layer covers the encapsulant around the semiconductor die~~pattern includes a double channel in the second insulating layer around the semiconductor die.

5. The semiconductor device of claim 1, further including an interconnect structure formed over the third insulating layer and electrically connected to the conductive layer.

6. The semiconductor device of claim 1, wherein the plurality of semiconductor die is singulated through the second insulating layer and encapsulant.

7. A semiconductor device, comprising:

a ~~plurality of~~ semiconductor die;

an encapsulant deposited around the semiconductor die;

a first insulating layer formed over the encapsulant and over a singulation area of the semiconductor device including a pattern formed in the first insulating layer between the singulation area and the semiconductor die;

a conductive layer formed over the first insulating layer; and

a second insulating layer formed over the first insulating layer and conductive layer.

8. The semiconductor device of claim 7, further including a third insulating layer formed over the semiconductor die.

9. The semiconductor device of claim 7, ~~further including a channel in the first insulating layer around the semiconductor die~~ wherein the pattern includes a channel.

~~10. The semiconductor device of claim 9, wherein the plurality of semiconductor die is singulated through the channel and encapsulant.~~

11~~1~~0. The semiconductor device of claim 7, ~~further including a net pattern in the first insulating layer around the semiconductor die~~ wherein the pattern includes a net pattern.

~~12. The semiconductor device of claim 7, wherein the first insulating layer covers the encapsulant around the semiconductor die.~~

~~13. The semiconductor device of claim 7, wherein the plurality of semiconductor die is singulated through the first insulating layer and encapsulant.~~

1~~4~~1. A semiconductor device, comprising:

a semiconductor die;

a first insulating layer formed over the semiconductor die;

an encapsulant deposited around the semiconductor die;

a second insulating layer formed over the ~~encapsulant~~ first insulating layer, the encapsulant, and over a singulation area of the semiconductor device;

a pattern formed in the second insulating layer directly over the singulation area, wherein the pattern includes at least three portions of the second insulating layer; and

an interconnect structure formed over the second insulating layer.

1~~5~~2. The semiconductor device of claim 1~~4~~1, wherein the interconnect structure includes:

a conductive layer formed over the second insulating layer; and

a third insulating layer formed over the second insulating layer and conductive layer.

1~~6~~3. The semiconductor device of claim 1~~4~~1, wherein the pattern includes a channel ~~further including a channel in the second insulating layer around the semiconductor die~~.

~~17. The semiconductor device of claim 16, wherein the plurality of semiconductor die is singulated through the channel and encapsulant.~~

1~~8~~4. The semiconductor device of claim 1~~4~~1, ~~further including~~ wherein the pattern includes a net pattern~~ in the second insulating layer around the semiconductor die~~.

~~19. The semiconductor device of claim 14, wherein the second insulating layer covers the encapsulant around the semiconductor die.~~

~~20~~15. A semiconductor device, comprising:

a semiconductor die;

an encapsulant deposited around the semiconductor die;

a first insulating layer formed over the encapsulant and semiconductor die extending beyond an active area of the semiconductor die including a pattern formed in the first insulating layer beyond the active area between a singulation area and the semiconductor die, wherein the pattern includes at least three portions of the first insulating layer; and

an interconnect structure formed over the first insulating layer.

~~21~~16. The semiconductor device of claim ~~20~~15, wherein the interconnect structure includes:

a conductive layer formed over the first insulating layer; and

a second insulating layer formed over the first insulating layer and conductive layer.

~~22~~17. The semiconductor device of claim ~~20~~15, further including a second insulating layer formed over the semiconductor die.

~~23~~18. The semiconductor device of claim ~~20~~15, ~~further including a channel in the first insulating layer around the semiconductor die~~ wherein the pattern includes a channel.

~~24~~19. The semiconductor device of claim ~~20~~15, ~~further including a net pattern in the first insulating layer around the semiconductor die~~ wherein the pattern includes a net pattern.

~~25. The semiconductor device of claim 20, wherein the first insulating layer covers the encapsulant around the semiconductor die.~~

20. A semiconductor device, comprising:

a semiconductor die;

an encapsulant deposited around the semiconductor die; and

an insulating layer formed over the encapsulant and over a singulation area of the semiconductor device including a pattern formed in the insulating layer directly over the singulation area, wherein the pattern includes at least three portions of the insulating layer.

21. The semiconductor device of claim 20, wherein the pattern includes a rectangular waveform pattern.

22. The semiconductor device of claim 20, wherein the insulating layer covers a substrate edge of the semiconductor device.

23. The semiconductor device of claim 20, further including:

a conductive layer formed over the insulating layer;

a second insulating layer formed over the conductive layer; and

an interconnect structure formed over the conductive layer.

24. The semiconductor device of claim 7, wherein the pattern includes a rectangular waveform pattern.

25. The semiconductor device of claim 15, wherein the pattern includes a rectangular waveform pattern.

26. The semiconductor device of claim 1, wherein the pattern includes a rectangular waveform pattern.

27. The semiconductor device of claim 7, wherein the pattern includes a double channel in the first insulating layer.

28. The semiconductor device of claim 11, wherein the pattern includes a double channel in the second insulating layer.

29. The semiconductor device of claim 15, wherein the pattern includes a double channel in the first insulating layer.

30. The semiconductor device of claim 20, wherein the pattern includes a double channel in the insulating layer.