

ABSTRACT OF THE DISCLOSURE

METHOD FOR FORMING A HIGH AREAL CAPACITANCE PLANAR CAPACITOR

A method for forming within an integrated circuit a high areal capacitance planar capacitor, and the high areal capacitance planar capacitor which results from the method. There is first formed upon a semiconductor substrate a first planar capacitor electrode. The first planar capacitor electrode has a first planar capacitor dielectric layer formed thereupon, and the first planar capacitor dielectric layer has a second planar capacitor electrode formed thereupon. Formed then upon the semiconductor substrate is a Pre-Metal Dielectric (PMD) layer which is planarized until the surface of the second planar capacitor electrode is fully exposed. There is formed upon the second planar capacitor electrode a second planar capacitor dielectric layer. Finally, there is formed upon the second planar capacitor dielectric layer a third planar capacitor electrode. The high areal capacitance areal capacitor may be formed within the integrated circuit without masking steps beyond those which are routinely employed in forming the integrated circuit.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)