## Asymmetrical Layout Structure for ESD Protection

ABSTRACT OF THE DISCLOSURE

A semiconductor structure for electrostatic discharge protection is presented. The semiconductor structure comprises a grounded gate nMOS (GGNMOS) having a substrate, a gate electrode, a source region and a drain region. A plurality of contact plugs is formed on the source and drain side. A plurality of first level vias is electrically coupled to the GGNMOS and has a substantially asymmetrical layout in the source and drain regions. A second level via(s) re-routes the ESD current to the desired first level vias. The uniformity of the current flow in the GGNMOS is improved.

(FIG. 4)