A TEST METHOD ON THE SUPPORT SUBSTRATE OF A SUBSTRATE OF THE "SEMICONDUCTOR ON INSULATOR" TYPE.

The invention is located in the field of manufacturing of electronic components, in particular a substrate known under the acronym of "SeOI", from the expression "*Semiconductor On Insulator*".

The present invention more particularly relates to a test method which comprises the fact of making an electric connection contact on the support substrate of a substrate of the SeOI type.

In the following of the description and of the claims, by substrate of the "SeOI" type, is meant a substrate which successively comprises a support substrate in a semiconducting material, entirely covered with an insulator layer, notably of oxide or nitride, and another layer of semiconducting material, a so-called "active layer", in or on which electronic components are or will be formed. A portion of this insulator layer is thus buried between said active layer and one of the faces of the support substrate, a so-called a "front face".

Such a substrate 1 is illustrated in the enclosed Fig. 1.

It comprises a support substrate 2 in a semiconducting material entirely covered with an insulator layer 3 and an active layer 4 of semiconducting material.

The portion of the insulator layer 3 located facing one of the faces of the support substrate 2, a so-called "front face 21", is referenced as 31. As this may be seen in the figure, part of the portion 31 of the insulator layer 3 is buried between the active layer 4 and the front face 21 of the support substrate 2.

The opposite face of the support substrate 2, called "rear face", bears reference 22. The portion of the insulator layer 3 located facing the rear face 22 bears the numerical reference 32, while the one located at the periphery of the support substrate 2 is referenced as 33.

The insulator 3 may for example be formed with an oxide, nitride or oxynitride. In the case when the semiconducting material forming the support substrate 2 and/or the active layer 4 is silicon, the insulator advantageously is silicon oxide (SiO_2) or silicon nitride (Si_3N_4).

Informatively, it will be noted that all the SeOI substrates do not have an insulating layer over the whole surface of the support substrate. This notably concerns “thick” SeOIs, i.e. SeOIs for which it is desired to have a relatively thick buried insulator thickness (from 1 micron to a few micrometers). For this type of SeOI substrates, it is customary to form an insulator (for example by oxidation) both on the "support" substrate and on the "donor" substrate before their assembling by bonding, so that after thinning the donor substrate, the support of the SeOI is entirely covered with an insulator. This type of substrate is

directed to power applications, for example the formation of components which process high power signals.

The invention applies to SeOI substrates, the support substrate of which is entirely covered with an insulator layer.

During the processes for manufacturing electronic components, it is sometimes useful to have access to the rear face 22 of the support substrate 2, for example in order to carry out electric tests of the components elaborated on the front face 21; these tests may notably require application of electric voltage at the rear face 22. To do this, it is then necessary to remove the insulator layer 32 present on the rear face of the support substrate.

Now, the applicant has seen that when the insulator layer 32 on the rear face is removed, the SeOI substrate deforms and assumes a slightly cambered shape.

This deformation or "camber" is known under the name of "*warp*" or "*warpage*" and it increases with the increase in the thickness of the buried insulator 31.

In other words, the forces or stresses in presence, inside the SeOI substrate, are no longer compensated when the insulator 32 of the rear face is removed.

The enclosed Fig. 2 illustrates the substrate of Fig. 1 after removing a portion of the insulator layer by wet chemical etching, this substrate exhibiting the "warpage" phenomenon. The stresses exerted by the insulator layer 31 are no longer compensated by the presence of the layer 32 and the SeOI substrate 1 tends to deform by becoming concave with concavity oriented towards the rear face 22 of the

support substrate 2, notably in the case of a BSOI structure (support and active layer in silicon and insulator in silicon oxide).

The "warpage" is measured at the concave portion of the support 2. It corresponds to the distance **a** between a plane **P** passing through the edges of the concavity, i.e. the edges of the support substrate 2 and the deepest point of the concavity, generally located in the centre of the support substrate 2.

"Warpage" **a** is measured by different techniques well known to one skilled in the art, i.e. optical or mechanical profilometry or capacitive thickness measurement techniques.

As an example, mention may be made of capacitive measurements using a piece of equipment known under the name of "Wafersight" from the manufacturer ADE (henceforth called KLA Tencor) which allow measurement of the thickness and deformation of a substrate. The warpage may also be measured by an optical measurement, for example with a piece of equipment known as FLEXUS, produced by the same manufacturer, which allows the surface of the support substrate to be scanned.

As an example, reference may be made to a substrate known to the person skilled in the art under the acronym of "BSOI", which means "Bonded Silicon On Insulator" and designates a substrate of the "Silicon on insulator" type obtained by bonding two silicon substrates, at least one of which (the support) has an oxidized surface, and then by thinning one of the two substrates in order to form the active layer. It was possible to measure that such a substrate, for example comprising buried oxide 31 with a thickness of the 2.5 µm, may attain a warpage of the order of 150 µm

when the oxide 32 of the rear face is removed, while it has a warpage a of less than 30 µm in the case when this oxide remains in place.

Now, significant warpage induces problems for gripping the substrates with robots, as well as problems for positioning the substrates on retaining members or planar supports, during their subsequent use.

This warpage occurrence phenomenon is described in document US 5,780,311, in the case of an SOI type substrate after disappearance of the oxide layer present on the rear face of the support substrate. However, the recommended solution only consists of protecting this oxide layer by depositing a protective layer made in polycrystalline or amorphous silicon, in nitride or in photosensitive resin.

Now, this solution cannot be applied in a test method which has exactly the goal of forming insulator-free electric connection contact areas.

The object of the invention is therefore to provide a test method with which an electric connection contact may be made on an SeOI substrate, and an electric voltage may be applied to the support substrate, while limiting to a maximum the warpage phenomenon of this substrate.

Preferably, the object of the invention is to limit the phenomenon of warpage to a value of less than 100 µm, still preferably less than 50 µm.

This object is achieved by a test method comprising an electrical connection contact on the support substrate of a substrate of the "semiconductor on insulator" type.

According to the invention, this method comprises the steps of:

- a) taking a substrate of the "semiconductor on insulator" type comprising a support substrate in a semiconducting material entirely covered with an insulator layer and a so-called "active" layer of semiconducting material, positioned on said support substrate so that a portion of said insulator layer is buried between said active layer and one of the faces, a so-called "front" face, of the support substrate,

- b) removing a portion of said insulator layer which extends at the periphery of the front face of the support substrate and/or which extends on its so-called "rear" opposite face, so as to delimit at least one insulator-free area of the support substrate, a so-called "accessible area", while retaining at least one portion of the insulator layer on the rear face,

- c) applying an electric voltage to said one or to said at least some of said accessible areas, so as to make said electric connection contact on the support substrate of the "semiconductor on insulator" substrate.

According to other advantageous and non-limiting characteristics of the invention, taken alone or as a combination:

- the portion of the insulator layer which is removed in step b) is taken at the annular insulator area extending at the periphery of the rear face of the support, and/or at the annular insulator layer which extends at the periphery of the front face of the support around the active layer;

- at least 50% of the surface area of the insulator layer of the rear face is retained, during application of step b);

- step b) consists of carrying out routing of the annular region of said insulator layer extending at the periphery of the front face of the support

substrate, this routing being carried out over a width comprised between 0.5 mm and 5 mm and/or of carrying out routing of the annular region of said insulator layer extending at the periphery of the rear face of the support substrate, this routing being carried out over a width comprised between 0.5 mm and 15 mm;

- removal of the insulator is carried out by grinding and/or polishing;

- removal of the insulator is carried out by lithography and/or chemical etching;

- removal of the insulator is carried out during the manufacturing of electronic components on and/or in said active layer;

- removal of the insulator is carried out after manufacturing the semiconductor-on-insulator substrate and before manufacturing electronic components on and/or in said active layer;

- the semiconductor-on-insulator substrate is obtained by bonding the support substrate covered with the insulator layer and a source substrate from which stems said active layer and in that the removal of the insulator is carried out during the manufacturing of said semiconductor-on-insulator substrate, after heat treatment for stabilizing the bond of both substrates;

- the insulator is an oxide, nitride or oxynitride.

The invention also relates to a test substrate of the "semiconductor on insulator" type comprising a support substrate in a semiconducting material covered with an insulator layer and a so-called "active" layer of semiconducting material, positioned on said support substrate so that a portion of said insulator layer is buried between said active layer and one of the faces, a so-called "front" face, of the support substrate.

According to the invention, a portion of said support substrate is free of insulator so that it is exposed, at least one portion of the rear face of the support substrate being covered with said insulator layer and said substrate has warpage (a) of less or equal to 50 µm.

Further, advantageously:

- the insulator layer which extends on the rear face of the support substrate extends over at least 50% of the surface area of this rear face,
- the buried insulator layer of this test substrate has a thickness greater than or equal to 0.2 µm, still preferably greater than or equal to 1 µm.

Other characteristics and advantages of the invention will become apparent from the description which will now be made of it, with reference to the appended drawings, which illustrate as an indication but not as a limitation, several possible embodiments thereof.

In these drawings:

- the aforementioned Fig. 1 is a diagram illustrating an SeOI type substrate, in a sectional view,
- the aforementioned Fig. 2 is a diagram illustrating the warpage phenomenon observed on the substrate of Fig. 1, after removing a portion of the insulator layer by wet chemical etching,
- Figs. 3-5 are diagrams illustrating SeOI type substrates in sectional views, after formation of areas providing an electric connection contact on the support substrate, according to three different embodiments of the method according to the invention,
- Fig. 6 is a top view of the SeOI substrate of Fig. 3, at a smaller scale,

- Fig. 7 is a bottom view of the substrate of Fig. 5, at a smaller scale, and

- Fig. 8 is a bottom view of an SeOI type substrate illustrating an alternative of Fig. 7.

The aforementioned figures are schematic and the dimensions and thicknesses of the different layers are not illustrated at their actual relative values.

The test method according to the invention may be applied to any type of SeOI substrate, whether the latter has been obtained by the aforementioned BSOI type method or by another method, for example one of the methods known under the name of SMART CUT or SIMOX, provided that the support substrate is actually surrounded by an insulator layer initially.

The test method according to the invention comprises the following steps:

- a) taking a substrate 1 of type SeOI,

- b) removing at least one portion of the annular region of the insulator layer 3 located at the periphery of the front face 21 or removing only a portion of the insulator layer 3 extending on the rear face 22 of the support substrate 2, in order to avoid occurrence of the warpage phenomenon,

- c) applying an electric voltage to said area of the support substrate cleared during step b) (or to at least at some of them if there are several of them), so as to make an electric connection contact on the support substrate 2 of the SeOI substrate 1.

A first embodiment of step b) of the method according to the invention will now be described with reference to Figs. 1, 3 and 6.

In Fig. 1, the active layer 4 is of a diameter slightly smaller than that of the support 2, typically of less than 2-5 mm. This is due to the use of chamfered wafer for making an SeOI substrate, which

do not allow bonding of both initial substrates up to the extreme edge. A so-called "exclusion" area, located on the front face, therefore does not include any active layer. Accordingly, the front face 21 of the support substrate 2 is covered with an insulator layer which extends beyond the edges of the active layer 4, and which has an annular shape. This annular shape is referenced as 310.

Step b) consists of removing at least one portion of the annular region 310 of said insulator layer, so as to delimit at least one area of the support substrate 2 which is found free of insulator. This so-called "accessible" area bears the numerical reference 210.

Of course, this removal is not possible if the diameter of the active layer 4 is identical with that of the support substrate 2 covered with the insulator layer.

The surface area of said accessible area should be sufficiently large so as to allow an electric connection contact for example of at least a few square millimeters.

This routing operation allows either removal of the totality of the annular insulator area 310, as illustrated in Fig. 6, or only of a portion, according to an alternative not shown in the figures. In the latter case, at least one accessible area 210, possibly several of them, are obtained on the periphery of the substrate. Fig. 8 illustrates a similar result obtained on the peripheral annular region of the rear face insulator 32.

As illustrated in Fig. 3, it is possible depending on the technique used for removing the annular insulator layer 310, that a small thickness of

the support substrate 2 located immediately below this annular region 310 should also be removed.

The annular region 310 preferably extends over a width **L1** comprised between 0.5 and 5 mm starting from the edge of the substrate 1.

As an example, this width **L1** is generally comprised between 1 and 3 millimeters for a substrate with a 6 inch (about 15 centimeters) diameter and between 1 and 4 millimeters for an 8 inch (about 20 centimeters) substrate.

The depth of the removed area **e1** is at least of the thickness of the insulator 310 i.e. of the order of a few micrometers, for example 2 µm, and may attain 15 µm if a portion of the support substrate 2 is also removed, or even a few tens of micrometers.

A first technique for removing the insulator consists of carrying out grinding and/or polishing of the latter.

This grinding or polishing may be mechanical and/or chemical. In the case of mechanical grinding, the substrate 1 may for example be held on a support driven into rotation and an also rotating tool is brought in contact with the annular region in order to grind the latter. In the case of polishing, it is possible to use a polishing shoe combined with a suitable chemical solution.

The grinding technique generally results in the removal of the insulator layer and of a portion of the support substrate 2, while with polishing, it is possible to more specifically only remove the insulator layer.

A second technique consists of using lithographic steps followed by dry or wet chemical etching steps. This more selective technique enables removal of only the annular insulated layer 310,

without etching the portion of the support substrate 2 located just below.

Finally, it will be noted that the insulator layer 32 is preferably retained on the rear face, which avoids the warpage phenomenon or else if a portion of it is removed, it is removed as explained hereafter.

A second embodiment of step b) will now be described with reference to Figs. 4 and 7.

In this case, step b) consists of removing a portion of the insulator layer 32 of the rear face of the support substrate 2, while retaining at least one portion of this insulator layer on the rear face. Preferably, the retained portion corresponds to at least 50% of the total surface area of the insulator layer 32 covering the rear face 22 of the support substrate 2.

Preferentially, step b) consists of removing the totality (see Fig. 7) or a portion (see Fig. 8) of an annular region of the insulator layer 32, this annular region extending at the periphery of the rear face of the support 2.

This annular region, visible before its removal on Fig. 1, bears numerical reference 320. This removal of the annular insulator layer 320 has the effect of clearing an accessible area 220 extending on the rear face of the support substrate 2.

This removal is applied by retaining at least the central portion of the insulator layer on the rear face. This central portion bears numerical reference 321.

The **L2** of the removed annular region is preferably comprised between 0.5 mm and 15 mm starting from the edge of the substrate 1.

As an example, **L2** is comprised between 2 and 10 mm for a substrate with a diameter of 6 inches

(about 15 cm) and between 2 and 15 mm for a an 8 inch (about 20 cm) substrate.

The thickness **e2** of the removed area corresponds to that of the insulator layer 32, i.e. of the order of a few micrometers, for example 2 µm.

Fig. 5 illustrates an alternative in which a portion of the rear face 22 of the support substrate 2, located under the annular insulator portion 320 is also removed. In this case, the thickness **e3** may attain 15 µm.

The techniques used for removing a portion of the annular insulator area 320 and possibly of the support substrate 2, are the same as those described earlier for the first embodiment.

In the embodiment illustrated in Fig. 8, only a portion of the annular region 320 of the insulator located on the rear face of the support substrate 2 has been removed. Two point-like accessible areas referenced as 221 are delimited.

The number of these cleared areas depends on subsequent tests to be conducted, it is for example related to the constraints of the equipment used or to the connection contact configurations.

The shape of the cleared areas is arbitrary and may be round, square or of another shape.

The point-like accessible areas 221 are preferably obtained by chemical etching through a mask comprising apertures which correspond to the shape of the areas 221 to be obtained.

A fourth embodiment not shown in the figures may consist of clearing the edges of the support substrate at the periphery, (area 33).

In all the embodiments which have just been described, the step for removing at least one portion

of the annular insulator region 310, 320 may be carried out and inserted in different stages of the method.

Thus, this removal may be carried out after manufacturing the semiconductor-on-insulator substrate 1, but before manufacturing electronic components on and/or in the active layer 4.

This removal may also be carried out during the manufacturing of electronic components on and/or in the active layer 4.

Finally, this removal may also be carried out during the manufacturing of the semiconductor-on-insulator substrate 1, after the support substrate 2 covered with the insulator layer 3 has been bonded on a source substrate and after heat treatment for stabilizing the bonding of both of these substrates, but before thinning the source substrate by which the active layer 4 may be obtained. It is also possible to contemplate preparation of the support substrate 2 in order to form the exposed areas before its bonding on the source substrate.

The last step of the method consists of applying an electric voltage to said accessible area and to at least some of said accessible areas, for example by means of an electrode, as illustrated in Fig. 8, and this, with the purpose of making an electric connection contact.

The main advantages of the method according to the invention are:

- that access to contact areas 210, 220 made on the support substrate 2 may be facilitated, while avoiding the warpage phenomenon on the SeOI substrate, the SeOI substrates obtained according to the method of the invention actually have warpage **a** of less than or equal to 50 µm;

- that addition of an additional step for forming accessible areas 210, 220 is accomplished without modifying existing manufacturing processes, whether these are the methods for manufacturing the SeOI substrate or those for electronic components.

CLAIMS

1. A test method comprising an electrical connection contact on the support substrate (2) of a substrate of the "semiconductor on insulator" type (1), characterized in that it comprises the steps of:

- a) taking a substrate (1) of the "semiconductor on insulator" type comprising a support substrate (2) in a semiconducting material entirely covered with an insulator layer (3) and a so-called "active" layer (4) of semiconducting material, positioned on said support substrate so that a portion (31) of said insulator layer (3) is buried between said active layer (4) and one of the faces (21), a so-called "front" face, of the support substrate (2),
- b) removing a portion of said insulator layer (3, 31, 32) which extends at the periphery of the front face (21) of the support substrate (2) and/or which extends on its opposite face (22), a so-called "rear" face, so as to delimit at least one insulator-free area (210, 220) of the support substrate (2), a so-called "accessible area", while retaining at least one portion (321) of the insulator layer (3) on the rear face,
- c) applying an electrical voltage to said one or at least some of said accessible areas (210, 220), so as to make said electrical connection contact on the support substrate (2) of the "semiconductor on insulator" substrate (1).

2. The method according to claim 1, characterized in that the portion of the insulator layer (3, 31, 32) which is removed in step b) is taken at the annular insulator area (320) extending at the

periphery of the rear face (22) of the support (2), and/or at the annular insulator area (310) which extends at the periphery of the front face (21) of the support (2) around the active layer (4).

3. The method according to claim 1 or 2, characterized in that at least 50% of the surface area of the insulator layer (32) of the rear face is retained during application of step b).

4. The method according to any of the preceding claims, characterized in that step b) consists of carrying out routing of the annular region (310) of said insulator layer (3) extending at the periphery of the front face (21) of the support substrate (2), this routing being carried out over a width (**L1**) comprised between 0.5 mm and 5 mm, and/or of carrying out routing of the annular region (320) of said insulator layer (3) extending at the periphery of the rear face (22) of the support substrate (2), this routing being carried out over a width (**L2**) comprised between 0.5 mm and 15 mm.

5. The method according to any of the preceding claims, characterized in that the removal of the insulator (310, 320) is carried out by grinding and/or polishing.

6. The method according to any of claims 1 to 4, characterized in that the removal of the insulator (310, 320) is carried by lithography and/or chemical etching.

7. The method according to any of the preceding claims, characterized in that the removal of

the insulator (310, 320) is carried out during the manufacturing of electronic components on and/or in said active layer (4).

8. The method according to any of claims 1 to 6, characterized in that the removal of the insulator (310, 320) is carried out after manufacturing the semiconductor-on-insulator substrate (1) and before manufacturing electronic components on and/or in said active layer (4).

9. The method according to any of claims 1 to 6, characterized in that the semiconductor-on-insulator substrate is obtained by bonding the support substrate (2) covered with the insulator layer (3) and a source substrate from which stems said active layer (4) and in that the removal of the insulator (310, 320) is carried out during the manufacturing of said semiconductor-on-insulator substrate, after heat treatment for stabilizing the bonding of both substrates.

10. The method according to any of the preceding claims, characterized in that the insulator (3) is an oxide, nitride or oxynitride.

11. A test substrate (1) of the "semiconductor on insulator" type comprising a support substrate (2) in a semiconducting material covered with an insulator layer (3) and a so-called "active" layer (4) of semiconducting material positioned on said support substrate so that a portion (31) of said insulator layer (3) is buried between said active layer (4) and one of the faces (21), a so-called "front" face, of the support substrate (2), characterized in

that one portion of said support substrate (2) is free of insulator so that it is exposed, at least one portion of the rear face (22) of the support substrate (2) being covered with said insulator layer and in that said substrate has warpage (a) of less than or equal to 50 µm.

12. The substrate according to claim 11, characterized by the fact that the insulator layer (321) which extends on the rear face (22) of the support substrate (2) extends over at least 50% of the surface area of this rear face (22).

13. The test substrate (1) according to claim 11 or 12, characterized in that the buried insulator layer (3) has a thickness larger than or equal to 0,2 µm.