

CLAIMS

1. A semiconductor structure, comprising:
a first semiconducting channel comprising a plurality of vertical nanowires; and
a second semiconducting channel comprising a plurality of vertical nanowires;
wherein the first semiconducting channel and the second semiconducting channel are configured to be in a stacked configuration;
wherein the plurality of vertical nanowires of the first semiconducting channel are configured to be in alternating positions relative to the plurality of vertical nanowires of the second semiconducting channel.
2. The semiconductor structure of claim 1, wherein the first semiconducting channel is disposed on a bulk substrate.
3. The semiconductor structure of claim 2, wherein the bulk substrate comprises silicon.
4. The semiconductor structure of claim 3, wherein the plurality of vertical nanowires of the first semiconducting channel and the plurality of vertical nanowires of the second semiconducting channel each comprise the silicon of the bulk substrate.
5. The semiconductor structure of claim 1, wherein the plurality of vertical nanowires of the first semiconducting channel are disposed in a first oxide layer and the plurality of vertical nanowires of the second semiconducting channel are disposed in a second oxide layer.
6. The semiconductor structure of claim 1, wherein the first semiconducting channel is configured to be stacked directly on the second semiconducting channel.
7. The semiconductor structure of claim 1, wherein the first semiconducting channel is an n-channel and the second semiconducting channel is a p-channel.
8. The semiconductor structure of claim 1, wherein the first semiconducting channel is a p-channel and the second semiconducting channel is an n-channel.
9. The semiconductor structure of claim 1, further comprises a liner disposed on a portion of each of the plurality of vertical nanowires of the first semiconducting channel and the plurality of vertical nanowires of the second semiconducting channel.
10. A logic device, comprising at least one semiconductor structure as claimed in any preceding claim.

11. An integrated circuit, comprising a logic device as claimed in claim 10.:
12. A method, comprising:
 - forming a first semiconducting channel comprising a plurality of vertical nanowires and a second semiconducting channel comprising a plurality of vertical nanowires on a semiconductor substrate;
 - wherein the first semiconducting channel and the second semiconducting channel are formed in a stacked configuration;
 - wherein the plurality of vertical nanowires of the first semiconducting channel are formed in alternating positions relative to the plurality of vertical nanowires of the second semiconducting channel.
13. The method of claim 12, wherein the semiconductor substrate comprises a layered silicon–insulator–silicon substrate.