[0029] The reactor 100 may include upper and lower liners 134, 136 disposed within the processing chamber to prevent reactions between the gas 110 and the chamber walls 130, 132 (which are typically fabricated from metallic materials, such as stainless steel). The liners 134, 136 may be fabricated from suitably non-reactive materials, such as quartz.

[0030] The reactor 100 is exemplary and generally any reactor which permits a semiconductor structure 104 to be processed (e.g., etched) according to the methods of the present disclosure may be used unless stated otherwise.

[0031] In accordance with methods of the present disclosure, the processing reactor 100 is conditioned prior to processing the semiconductor structure 104 by depositing an engineered polycrystalline silicon surface layer 135 (FIG. 4) or "film" on the preheat ring 126 and susceptor 120. In a first step S_1, any existing surface layer or coating is stripped from the preheat ring 126 and susceptor 120 (i.e., a "clean etch" is performed). A stripping etchant such as hydrogen chloride (HCl) may be introduced into the reactor 100 without a semiconductor structure being disposed on the susceptor 120 to strip any previous polycrystalline silicon surface layer from the susceptor 120 and preheat ring 126. In some embodiments, the stripping step S_1 may be eliminated (e.g., if the susceptor 120 and/or preheat ring 126 is not coated with a previously-deposited polycrystalline silicon surface layer).

[0040] Generally, the semiconductor structure 104 may be any structure in which it is desirable to etch the structure. Referring now to FIG. 6, in some embodiments the semiconductor structure is a silicon-on-insulator (SOI) structure 104. The silicon-on-insulator structure 104 includes a handle structure 110, a silicon top layer 125, and dielectric layer 115 disposed between the handle structure 110 and the silicon layer 125. The silicon-on-insulator structure 104 may be produced by any of methods known to those of skill in the art. In some embodiments, the semiconductor structure 104 has an amount of oxide on the edge of the semiconductor structure.

[0041] Once the semiconductor structure 104 (which may be referred to herein as a "first" semiconductor structure) is contacted with a smoothing etchant, additional structures may be processed according to embodiments of the present disclosure. The first semiconductor structure 104 is removed from the susceptor 120 after it has been etched (e.g., smoothed). The susceptor 120 is contacted with a stripping etchant (i.e., step S_1 above) to strip the surface-modified polycrystalline silicon surface layer 135 from the susceptor 120. A second polycrystalline silicon surface layer is deposited on the susceptor 120 and preheat ring 126 (step S_2). In some embodiments, the second polycrystalline silicon surface layer is deposited at a relatively low temperature to decrease the grain size of the deposited surface layer as described above (e.g., less than 1150°C, less than 1125°C, less than 1100°C, less than 1075°C, less than 1050°C, less than 1000°C or less than 900°C).

[0042] Alternatively or in addition to depositing the second polycrystalline silicon surface layer 135 at a relatively low temperature to decrease the grain size of the second polycrystalline silicon surface layer, in some embodiments, the second polycrystalline silicon surface layer is contacted with the first etchant (i.e., a separate gas having the same or close concentration to the first etchant described above) to produce a second surface-modified polycrystalline silicon surface layer. A second semiconductor structure (e.g., same type of structure as structure 104 described above) is loaded onto the susceptor 120 (e.g., which has a polycrystalline silicon surface layer deposited at the relatively lower temperatures described above and/or which is surface-modified as described above). The second semiconductor structure is contacted with the second etchant (i.e., a separate gas having the same or close concentration to the second etchant described above) to etch the second semiconductor structure.

[0043] Compared to conventional methods for etching a semiconductor structure, the methods of the present disclosure have several advantages. In embodiments in which the temperature at which the polycrystalline silicon surface layer is deposited on the susceptor is relatively low (e.g., less than 1150°C, less than 1125°C, less than 1100°C, less than 1075°C, less than 1050°C, less than 1000°C or less than 900°C), the grain size of the polycrystalline silicon may be reduced which increases the surface area of the surface layer. In embodiments in which the polycrystalline surface layer is surface-modified such as by contacting the polycrystalline surface layer with a

polycrystalline silicon layer. As can be seen from FIG. 7, reducing grain size and increasing grooving factor drive the surface area increase up to 2 orders or magnitude.

Example 2: Edge Roll-Off Effect of Use of Polycrystalline Silicon Susceptor Coatings Engineered by Reduced Temperature Deposition and/or Grooving

[0047] Several polycrystalline silicon engineered coatings were formed on a susceptor and the edge thickness effect was evaluated. Deposition temperature was used to control the grain size as shown in Table 1. Grooving in H_2 and H_2+HCl mixture were employed to further increase the total exposed surface area.

[0048] The semiconductor structures were 300 mm SOI wafers. Edge thickness roll-off from the 147 mm radial position to the wafer edge was evaluated. The azimuthal thickness range at the 147 mm radial position was also evaluated (i.e., the thickness variation across wafer rotation angles at 147 mm).

[0049] As shown in FIG. 8, the difference between the reference coating process (with temperature ramping down from 1150°C to 1000°C and a thickness of 1 μm) and the other runs shows increasing the thickness of the polycrystalline silicon coating layer from 1 to 2 μm reduces the edge thickness range by more than 50%. Without being bound by any particular theory, it is believed that the increase in uniformity may be attributed to the increased surface area from roughness. As layer thickness increases, the surface roughness increases and total surface area increases. Grooving the polycrystalline silicon coating (Run B and Run C) by contacting the coating

with an etchant also reduced edge roll-off and increased uniformity resulting in an additional improvement in the thickness range by 10 Å. In Run D, lowering the coating temperature from 1150°C to 1000°C reduced the grain size by about 2-3 times and further improved the thickness range by additional 5 Å.

Coating	Temperature	Thickness (μm)	Grooving time (s)
Reference Run	1150-->1000 dynamic	1	0
Coating Run A	1150°C	2	0
Coating Run B	1150°C	2	30 (in H_2)
Coating Run C	1150°C	2	30 (in H_2+HCl)
Coating Run D	1000°C	2	0

Table 1: Polycrystalline Silicon Coating Conditions

[0050] As used herein, the terms “about,” “substantially,” “essentially” and “approximately” when used in conjunction with ranges of dimensions, concentrations, temperatures or other physical or chemical properties or characteristics is meant to cover variations that may exist in the upper and/or lower limits of the ranges of the properties or characteristics, including, for example, variations resulting from rounding, measurement methodology or other statistical variation.

[0051] When introducing elements of the present disclosure or the embodiment(s) thereof, the articles "a," "an," "the," and "said" are intended to mean that there are one or more of the elements. The terms "comprising," "including," “containing,” and "having" are intended to be inclusive and mean that there may be

CLAIMS:

1. A method for etching a semiconductor structure in a processing reactor comprising a susceptor which supports the semiconductor structure, the method comprising:

depositing a polycrystalline silicon surface layer on the susceptor;

contacting the polycrystalline silicon surface layer with a first etchant to produce a surface-modified polycrystalline silicon surface layer;

loading a semiconductor structure onto the susceptor having the surface-modified polycrystalline silicon surface layer disposed thereon; and

contacting the semiconductor structure with a second etchant to etch the semiconductor structure.

2. The method as set forth in claim 1 wherein the first etchant is hydrogen, hydrogen chloride or a mixture of hydrogen and hydrogen chloride.

3. The method as set forth in claim 1 wherein the polycrystalline silicon surface layer is deposited on the susceptor at a temperature less than 1150°C.

4. The method as set forth in claim 3 wherein the polycrystalline silicon surface layer is deposited by introducing trichlorosilane into the processing reactor.

5. The method as set forth in claim 1 wherein the polycrystalline silicon surface layer is deposited on the susceptor at a temperature less than 1100°C.

6. The method as set forth in claim 1 wherein the processing reactor comprises a preheat ring having an opening in which the susceptor is disposed, the method further comprising:

depositing a polycrystalline silicon surface layer on the preheat ring; and

contacting the polycrystalline silicon surface layer disposed on the preheat ring with the first etchant to produce a surface-modified polycrystalline silicon surface layer.

7. The method as set forth in claim 1 wherein the susceptor is made of silicon carbide or silicon-carbide coated graphite.

8. The method as set forth in claim 1 wherein, prior to depositing the polycrystalline silicon surface layer on the susceptor, the susceptor is contacted with a stripping etchant to strip a previously deposited polycrystalline silicon surface layer from the susceptor.

9. The method as set forth in claim 1 wherein the semiconductor structure is a silicon-on-insulator structure having a handle structure, a silicon top layer and a dielectric layer disposed between the handle structure and the silicon top layer.

10. The method as set forth in claim 1 wherein the second etchant is hydrogen, hydrogen chloride or a mixture of hydrogen and hydrogen chloride.

11. The method as set forth in claim 1 wherein the polycrystalline silicon surface layer has a thickness of at least 1.25 µm.

12. The method as set forth in claim 1 wherein the semiconductor structure is a first semiconductor structure, the method further comprising:

removing the first semiconductor structure from the susceptor after the first semiconductor structure has been etched;

contacting the susceptor with a stripping etchant to strip the surface-modified polycrystalline silicon surface layer from the susceptor;

depositing a second polycrystalline silicon surface layer on the susceptor;

contacting the second polycrystalline silicon surface layer with the first etchant to produce a second surface-modified polycrystalline silicon surface layer;

loading a second semiconductor structure onto the susceptor having the second surface-modified polycrystalline silicon surface layer disposed thereon; and

contacting the second semiconductor structure with the second etchant to etch the second semiconductor structure.

13. A method for etching semiconductor structures in a processing reactor comprising a susceptor which supports a semiconductor structure within a recess of the susceptor, the method comprising:

depositing a first polycrystalline silicon surface layer on the susceptor at a temperature of less than 1150°C;

loading a first semiconductor structure onto the susceptor having the first polycrystalline silicon surface

layer disposed thereon, the first semiconductor structure being disposed within the recess; and

contacting the first semiconductor structure with an etchant to etch the semiconductor structure, the first semiconductor structure that is etched being the first semiconductor structure loaded onto the susceptor after the first polycrystalline silicon surface layer is deposited on the susceptor;

removing the first semiconductor structure from the susceptor after the first semiconductor structure has been etched;

contacting the susceptor with a stripping etchant to strip the first polycrystalline silicon surface layer from the susceptor;

depositing a second polycrystalline silicon surface layer on the susceptor at a temperature of less than 1150°C;

loading a second semiconductor structure onto the susceptor having the second polycrystalline silicon surface layer disposed thereon, the first and second semiconductor structures being semiconductor structures that are consecutively loaded onto the susceptor; and

contacting the second semiconductor structure with the etchant to etch the second semiconductor structure.

14. The method as set forth in claim 13 wherein the first polycrystalline silicon surface layer and the second polycrystalline silicon surface layer are each deposited by introducing trichlorosilane into the processing reactor.

15. The method as set forth in claim 13 wherein the first polycrystalline silicon surface layer and the second polycrystalline silicon surface layer are each deposited on the susceptor at a temperature less than 1100°C.

16. The method as set forth in claim 13 wherein, prior to depositing the first polycrystalline silicon surface layer on the susceptor, the susceptor is contacted with a stripping etchant to strip a previously deposited polycrystalline silicon surface layer from the susceptor.

17. The method as set forth in claim 13 wherein the first and second semiconductor structures are each a silicon-on-insulator structure having a handle structure, a silicon top layer and a dielectric layer disposed between the handle structure and the silicon top layer.

18. The method as set forth in claim 13 wherein the first polycrystalline silicon surface layer and the second polycrystalline silicon surface layer each has a thickness of at least 2 μm.

19. The method as set forth in claim 13 wherein the susceptor is made of silicon carbide.

20. The method as set forth in claim 13 wherein the susceptor is made of opaque graphite coated with silicon carbide.

21. The method as set forth in claim 13 wherein the first polycrystalline silicon surface layer and the second polycrystalline silicon surface layer are each deposited by contacting the susceptor with trichlorosilane at a temperature of 900°C to 1050°C.

22. A method for conditioning a processing reactor for treating a single semiconductor structure, the reactor comprising a susceptor for supporting a semiconductor structure within a recess of the susceptor, the method comprising:

introducing a stripping etchant into the processing reactor without a semiconductor structure being disposed on the susceptor to strip a polycrystalline silicon surface layer from the susceptor;

depositing a polycrystalline silicon surface layer on the susceptor without a semiconductor structure being disposed on the susceptor; and

introducing a grooving etchant into the processing reactor without a semiconductor structure being disposed on the susceptor, the grooving etchant contacting the polycrystalline silicon surface layer to produce a surface-modified polycrystalline silicon surface layer.

23. The method as set forth in claim 22 wherein the grooving etchant is hydrogen, hydrogen chloride or a mixture of hydrogen and hydrogen chloride.

24. The method as set forth in claim 22 wherein the polycrystalline silicon surface layer is deposited on the susceptor at a temperature less than 1150°C.

25. The method as set forth in claim 22 wherein the polycrystalline silicon surface layer has a thickness of at least 1.5 μm.

26. The method as set forth in claim 22 wherein the susceptor is made of silicon carbide or is coated with silicon carbide.

27. The method as set forth in claim 22 wherein:

the stripping etchant removes the polycrystalline silicon surface layer from an upper surface of the susceptor, the upper layer being higher than the recess relative to a longitudinal axis of the processing reactor; and

the polycrystalline silicon surface layer is deposited on the upper surface of the susceptor.

28. The method as set forth in claim 22 wherein the semiconductor structure has a diameter less than diameter of the susceptor.

29. A method for conditioning a processing reactor for treating a single semiconductor structure, the reactor comprising a susceptor for supporting a semiconductor structure and a preheat ring that surrounds the susceptor, the preheat ring and susceptor being separated by a gap, the method comprising:

introducing a stripping etchant into the processing reactor without a semiconductor structure being disposed on the susceptor to strip a polycrystalline silicon surface layer from the susceptor, wherein an upper surface of the preheat ring and upper surface of the susceptor are aligned relative to a vertical axis of the processing reactor;

depositing a polycrystalline silicon surface layer on the susceptor without a semiconductor structure being disposed on the susceptor; and

introducing a grooving etchant into the processing reactor without a semiconductor structure being disposed on the susceptor, the grooving etchant contacting the

polycrystalline silicon surface layer to produce a surface-modified polycrystalline silicon surface layer.

30. The method as set forth in claim 29 wherein:

the susceptor is made of silicon carbide or is coated with silicon carbide; and

the preheat ring is made of silicon carbide or is coated with silicon carbide.

31. The method as set forth in claim 29 wherein the stripping etchant strips a polycrystalline silicon surface layer from the preheat ring, the method comprising depositing a polycrystalline silicon surface layer on the preheat ring without a semiconductor structure being disposed on the susceptor.

32. The method as set forth in claim 29 wherein the susceptor comprises a recess to support a semiconductor structure.

33. A method for conditioning a processing reactor to reduce edge roll-off of a single semiconductor structure during etching of the semiconductor structure, the reactor comprising a susceptor for supporting the semiconductor structure and a one-piece preheat ring that surrounds the susceptor, the one-piece preheat ring and susceptor being separated by a gap, the semiconductor structure being supported within a recess of the susceptor, the method comprising:

introducing a stripping etchant into the processing reactor without a semiconductor structure being disposed on the susceptor to strip a polycrystalline silicon surface layer from the susceptor and the one-piece preheat ring; and

depositing a polycrystalline silicon surface layer on the susceptor and one-piece preheat ring without a semiconductor structure being disposed on the susceptor to reduce edge roll-off of the semiconductor structure during etching of the semiconductor structure, the polycrystalline silicon surface layer being deposited by contacting the susceptor with trichlorosilane at a temperature of 900°C to 1050°C.

34. The method as set forth in claim 33 wherein the polycrystalline silicon surface layer has a thickness of at least 2 µm.

35. The method as set forth in claim 33 wherein the semiconductor structure has a diameter less than diameter of the susceptor.

36. The method as set forth in claim 33 wherein the susceptor is made of silicon carbide or is coated with silicon carbide.