

IMPROVEMENTS IN OR RELATING TO SOLID STATE  
IMAGE SENSORS FOR USE IN RANGEFINDERS  
AND RANGEFINDERS USING SAME

5       The present invention relates to solid state image sensors for use in rangefinders and to rangefinders using such solid state image sensors.

10       An automatic rangefinder is known which projects a beam of light upon an object in a scene to form a small illuminated area on the object. An image of the scene, including the illuminated area, is formed on a linear image sensor. The location of the image of the illuminated area along the image sensor is determined by the range of the object in the scene. Conversely, the location of the image of the illuminated area along the image sensor is an indication of the range of the object. Such a range-finding device finds application, for example, in an automatic focusing camera.

20       The general arrangement of elements and mode of operation of such a known rangefinding device will be described with reference to FIG. 1. Means for projecting a beam of light is shown by way of example as a light emitting diode (LED) 10 and a lens 12. The beam is projected along a path 14 to illuminate a small area on an object  $O_1$  in a scene. The scene is imaged by a second lens 16 onto an image sensor comprising a linear array 17 of photosensors. The signals produced by the photosensors are analyzed by control electronics 20 to determine the position of the illuminated spot in the scene and produce a signal 19 representing the range of the object.

30       As shown by example in FIG. 1, the apparent position of the illuminated area in the scene is a function of distance along light path 14 to the object. For an object  $O_1$  located at a distance  $D_1$  from the rangefinding device, the image of the

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illuminated area will fall on the image sensor at a location  $S_1$ . For an object  $O_2$  at a further distance  $D_2$ , the image of the area will fall on the image sensor at a location  $S_2$ . By examining the output of the image sensor, the control electronics 20 determines (for example, by comparing the outputs of the elements to determine that output which is a maximum) the location of the illuminated area in the scene and thereby the range of the object.

10 When the ambient illumination is relatively bright, the scene itself, regardless of the illuminated area, will produce substantial modulation of the photosensor array. Under such circumstances, it may not be possible to determine the location of the  
15 illuminated area merely by examining the outputs of the photosensors. The effects of ambient scene light can be removed however by operating the sensor with the beam off and again with the beam on, and subtracting the signals produced thereby. The information in the difference signal is solely from the  
20 illuminated area. One way of accomplishing this subtraction is shown in US-A-4274735. US-A-4274735 describes a device having a pair of memory capacitors associated with each photosensor in the array. The  
25 capacitors are selectively connectable to the photosensors by field effect transistor (FET) switches, and each pair is further connectable to an associated differential amplifier. In operation, a photosensor is first connected to one of the capacitors while the  
30 light beam is off. The photosensor is then connected to the other capacitor while the light beam is on. Both the capacitors are then connected to the differential amplifier to produce a difference signal free from information derived from ambient scene light.  
35 The signals are compared in an array of comparators to determine the location of the illuminated area by

sensing the largest difference signal produced by the array of differential amplifiers.

To effectively remove the relatively large signal derived from ambient scene light from the relatively small signal component due to the illuminated area, each of the differential amplifiers must have very good common mode rejection. Furthermore, so that the amplifiers themselves do not introduce overwhelming pattern noise into the signals, they must be very closely matched. The need for a plurality of closely matched differential amplifiers exacts a high price on any attempt to increase the signal-to-noise ratio of the device. Furthermore, the use of an array of comparators to determine the maximum difference signal from the differential amplifiers complicates the signal processing circuitry.

According to the present invention there is provided a rangefinder for finding the range of an object in a scene, comprising a light source selectively energizable for projecting a beam of light to illuminate a small area on the object, a solid state image sensor comprising a linear array of  $N$  photosensitive elements, each responsive to light for generating a signal indicative of the amplitude of light incident on it, analog shift register means, adjacent said linear array, for receiving the  $N$  signals in parallel into  $N$  alternate cells and shifting the signals serially toward an output location, said shift register means having  $2N$  cells, and transfer means responsive to a control signal for transferring said  $N$  signals from the array of photosensitive

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elements into alternate cells of said shift register means, means for forming an image of a portion of the scene containing the illuminated small area on the array of photosensitive elements, and control means for 1) sending a control signal to said transfer means for transferring a first set of N signals into the shift register means from the array, 2) supplying clock control signals to the analog shift register means to shift the signals by one cell, 3) energizing the light source, 4) de-energizing the light source, 5) sending a control signal to said transfer means to transfer a second set of N signals, created with the light source on, into the shift register means, and 6) supplying clock signals to the shift register means to shift the signals therein serially to the output location, and signal processing means, including means for 1) receiving the signals serially from the output location of the image sensor and forming a series of difference signals representative of the difference between the signals of each pair of adjacent signals derived from the same photosensitive element and 2) detecting the location of the image of the small illuminated area on the basis of the magnitudes of the difference signals, and forming a range signal on the basis of the detected location of the small illuminated area.

Means may be provided for establishing a predetermined signal content in the photosensitive elements prior to generating signals in the array. Such a predetermined signal content may be a zero signal or a constant non-zero signal.

In a preferred embodiment, said photosensitive elements are photodiodes, said analog shift register means is a buried channel charge coupled device (CCD) shift register having  
5 alternate cells aligned with said photodiodes, said transfer means is a first transfer gate responsive to a control signal for forming surface channels between said photodiodes and said alternate cells of said CCD shift register, and wherein the means  
10 for establishing a predetermined signal content in the photosensitive elements comprises drain means adjacent the array of photodiodes and a second transfer gate responsive to a control signal for coupling the photodiodes to the drain means.  
15 Advantageously, the means for detecting the location of the image of the small illuminated area comprises peak detector means responsive to the difference signals for producing a pulse each time a new greater difference signal is received.  
20 The peak detector means comprises a storage capacitor for storing the last greatest difference signal. Comparator means are provided for comparing the voltage on the storage capacitor with the next difference signal and producing an output  
25 pulse whenever the next difference signal is greater than the value on the storage capacitor. Switching means are responsive to the output pulse for replacing the signal on the storage capacitor with the greater difference signal.  
30 Means may be provided for introducing a threshold value onto the storage capacitor prior to the operating of the means for detecting.

The present invention will now be described, by way of example, with reference

to Figs. 2 to 9 of the accompanying drawings, in which:-

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FIG. 2 is a schematic diagram of an image sensor including a photosensor array and an analog shift register, in accordance with the present invention;

FIG. 3 is a partial plan view showing the electrode and channel structure of the image sensor shown in FIG. 2;

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FIG. 4 is a schematic cross-sectional view and potential diagram of the image sensor taken along line IV-IV in FIG 2;

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FIG. 5 is a schematic block diagram showing the signal processing and control electronics of a rangefinder according to the present invention;

FIG. 6 is an electrical circuit schematic diagram showing the signal processing electronics for differencing and peak detecting;

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FIG. 7 is a flow chart showing the general operation of the rangefinder; and

FIGS. 8 and 9 are timing diagrams useful in explaining the operation of the rangefinder.

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FIG. 2 shows a linear image sensor 18 according to the present invention. The image sensor 18 includes a linear array of N photosensors 22, such as photodiodes, and a charge coupled device (CCD) shift register 24. The CCD shift register has 2N cells labelled 1a, 1b, 2a, 2b, Na, and Nb. A transfer gate 26 between the array of photosensors 22 and CCD shift register 24 is actuatable for transferring charge (in the direction of arrows X) from the photosensors 22 into alternate cells (those subscripted with an "a") of the shift register 24. A second transfer gate 32 between the array of photosensors 22 and a reset drain 28 (to which is applied a voltage  $V_{OD}$ )

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is actuable for transferring charge (in the direction of arrows Y) from the photosensors 22 into the reset drain 28. The CCD shift register 24 is of the buried channel variety to maximize its transfer efficiency and hence the signal-to-noise ratio of the device, and the transfer channels created by the transfer gate 26 are surface channels.

The signals in the CCD shift register 24 are shifted serially in the direction of arrow Z to an output diode 34 by applying four-phase clock signals  $\Phi_1$ -4 to transfer electrodes (not shown in FIG. 2) of the CCD shift register 24. The signals are detected at the output diode 34 by a preamplifier 36.

FIG. 3 is a partial plan view illustrating the electrode and channel structures of the image sensor 18, showing the linear array of photosensors 22 and the associated buried channel CCD readout shift register 24. The device was constructed using well-known MOS fabrication techniques on a p-type silicon substrate 38. The buried channel for the CCD shift register 24 comprising, for example, an n-type region 40 in the p-type silicon substrate 38, is shown by broken lines. Channel stopping regions 42 and 42' confine the CCD shift register 24 and photosensors 22 and comprise, for example, (p+)-type regions under a thickened field oxide (shown by the shaded regions). The photosensors 22, in this case photodiodes, are formed by (n+)-type diffusions in the areas defined between the channel stopping regions 42'. Reset drain 28 and a scavenger drain 30 (which also receives voltage  $V_{OD}$ ) are formed by (n+)-type regions in the substrate.

Two levels of polysilicon, overlying the channels, define the electrode structure of the device. A first level of polysilicon defines the phase-2 and phase-4 electrodes (44 and 46 respectively) of the CCD shift register 24, and the transfer gate

32. A second level of polysilicon defines the phase-1 and phase-3 electrodes (48 and 50 respectively) of the CCD shift register 24 and the transfer gate 26. Alternate phase-2 electrodes 44 and the transfer gate 26 form surface channels that couple the photodiodes to alternate cells of the CCD shift register 24. The transfer gate 32 forms a surface channel coupling the photodiodes to the reset drain 28.

FIG. 4 is a partial, cross-sectional view of the image sensor taken along line IV-IV in FIG. 3, showing the channel structure of the sensor array. A layer of silicon dioxide 52 overlies the doped regions of the device.

Solid line 54 depicts the potential profile across the device when 0 volts is applied to the transfer gates 26 and 32 and 5 volts is applied to the phase-2 electrode 44. Potential barriers 56 and 58 keep charge generated in the photodiode from flowing into either the CCD shift register 24 or the drain 28. If approximately 5 volts is applied to either transfer gate 26 or 32, the potential barrier thereunder is lowered to the position shown by broken lines 60 or 62 respectively and allows the charge in the photodiode to flow into the CCD shift register 24 beneath the phase-2 electrode 44 via the surface channel created under transfer gate 26 or into the drain 28 via the surface channel created under transfer gate 32. When the 5-volt potential is removed from transfer gate 26 and the phase-2 electrode 44, the potential well thereunder collapses as shown by broken line 64. Charge in the shift register 24 is moved in a direction perpendicular to the plane of the drawing by pulsing the 4-phase transfer

electrodes in the conventional manner for moving charge in a CCD shift register.

Referring now to FIG. 5, overall control of the rangefinder is provided by a programmed micro-processor 100 via conventional driver circuits 102. The microprocessor 100 is supplied with timing signals from a clock circuit 104 and with power via a main power switch 106 from a battery 108. Four-phase clock signals  $\phi_1$ - $\phi_4$ , transfer signals  $T_1$  and  $T_2$  and drain bias voltage  $V_D$  are supplied to the linear image sensor 18 from driver circuits 102 under control of microprocessor 100 to produce output signals from the CCD shift register of the sensor 18. The signals from the CCD shift register are supplied to a differencing circuit 110. Difference signals produced by the differencing circuit 110 are supplied to a peak detector circuit 114. The output of the peak detector circuit 114 is supplied to a latch circuit 116. Latch circuit 116 is connected to the outputs of a digital counter 118. Counter 118 receives a reset signal R and a timing signal  $\phi_T$  having the same frequency as the four-phase clock signals  $\phi_1$ - $\phi_4$ . The output of the latch circuit 116 is supplied to an input port of microprocessor 100.

The driver circuits 102 also power LED 119 and an output device 120 such as a range display or a range servo. LED 119 preferably emits infra-red light.

FIG. 6 is a more detailed circuit schematic of the signal processing electronics shown in FIG. 5. A portion of the CCD shift register 24 showing output gate 122 and output diode 34 is included.

The output preamplifier 36 is an on-chip, sense and reset amplifier including a sense FET 124 and a reset FET 126. The sense FET 124 is a surface channel device and the reset FET 126 is a buried



channel device. A buried channel FET 128 is connected between the drain of the FET 124 and earth in a constant current configuration for converting the sensed charge on diode 34 to a voltage at node A.

5           The differencing circuit 110 comprises a first sampling FET 130 for sampling the output at node A, a detection capacitor 132, a clamping FET switch 134, and an amplifier 136. Differencing circuit 110 also includes a sample and hold portion comprising a second sampling FET 138, a storage capacitor 140 and an amplifier 142.

10           The peak detector circuit 114 comprises a differential amplifier 146, a reference capacitor 148, a sampling FET switch 150, and a timing FET switch 152. The peak detector circuit 114 also contains a threshold setting portion comprising a preset FET switch 154 connecting capacitor 148 to earth, and a threshold setting FET switch 156 connecting the supply voltage  $V_{DD}$  to capacitor 148 through a resistor 158.

15           The operation of the rangefinder will now be described with reference to FIGS. 7, 8 and 9. FIG. 7 is a flow chart showing a control program for the microprocessor 100 (see FIG. 5). Upon closure of  
20           main power switch 106 at time  $t_0$ , (see FIG. 8) the microprocessor 100 initializes the photosensor array by transferring any accumulated charge from photosensors 22 into drain 28 by applying a  $T_2$  transfer pulse to transfer gate 32 (FIG. 8b). At time  
25            $t_1$  after the  $T_2$  transfer pulse, the microprocessor 100 executes a time delay of period  $\tau_1$  to accumulate background charge due to ambient scene illumination in the photosensor array. After time delay period  $\tau_1$ , at time  $t_2$ , the "background" charge is  
30           transferred to the CCD shift register 24 by holding  $\phi_2$  high and pulsing transfer gate 26 with a  
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T<sub>1</sub> pulse (see FIGS. 8a and c).

The microprocessor 100 then commands a sequence of four-phase clock signals to advance all the signals in the CCD shift register 24 by one cell, leaving the signals under them in the alternate phase-2 electrodes between the photosensors (see FIG. 8c). The photosensor array is again initialized by applying a T<sub>2</sub> transfer pulse to transfer gate 32 (see FIG. 8b).

Next, at time t<sub>3</sub>, the microprocessor 100 turns on LED 119 (see FIG. 5), while  $\phi_2$  is held high (see FIGS. 8c and 8f). LED 119 is kept on for a period  $\tau_1$  during which the signal processing circuitry is initialized to set the threshold of the peak detector circuit 114. FET switch 154 (see FIG. 6) is turned on momentarily by generating a  $\phi_{\text{preset}}$  pulse (see FIG. 8d) to earth capacitor 148. Then, a pulse  $\phi_{\text{TH}}$  is applied to the threshold setting FET switch 156 for a period  $\tau_2$  (see FIG. 8e) to charge capacitor 148 to a value determined by the time constant of resistor 158 and capacitor 148. At time t<sub>4</sub>, the LED 119 is turned off and the "background plus LED" signals generated by the sensor array are transferred to the CCD shift register 24 by applying a pulse T<sub>1</sub> to transfer gate 26 (see FIG. 8a). The CCD shift register 24 now contains signals representing background illumination, interlaced with signals representing background plus LED illumination. The CCD shift register 24 is then read out to generate the range signal by applying the four-phase clock signals  $\phi_{1-4}$  to the four-phase transfer electrodes 44, 46, 48, and 50 (see FIG. 8c).

The effects of varying ambient light levels, such as the flicker experienced under fluorescent illumination, may be removed by a synchronous detection scheme. The image sensor is operated once

with the light beam on and once with the light beam off as described above, but then the accumulated charges are shifted back one cell in the shift register, and the whole cycle is repeated several times, thereby averaging out any fluctuation in the ambient illumination.

Processing of the signals from the CCD shift register 24 will now be described with reference to FIG. 9. The four-phase clock signals  $\phi_1$  -  $\phi_4$  are shown in FIGS. 9a-d. While the signal charges reside under the phase-3 and phase-4 electrodes, 50 and 46 respectively, ( $\phi_3$  and  $\phi_4$  simultaneously high) a reset pulse  $\phi_R$  is applied to buried channel reset FET 126 to prepare the output diode 34 to receive the first signal charge. The first signal charge that is read out represents the background illumination sensed by the Nth photosensor in the array. When the reset pulse  $\phi_R$  is applied to the FET 126, the voltage at node A goes to a high level (200 in FIG. 9f). When the phase-3 transfer gate 50 goes low, some of the signal charge spills over the output gate onto the output diode 34, and the output goes to the intermediate level 202 in FIG. 9f. Finally, when the phase-four transfer gate 46 goes low, all the signal charge is moved to the output diode 34 and the output signal at node A goes to its final signal level 204 as shown in FIG. 9f.

While the final signal level 204 is present at node A a pulse  $\phi_E$  (see FIG. 9g) is applied to first sampling FET 130, thereby storing the "background" level at node A on capacitor 132. Immediately thereafter, a pulse  $\phi_{CL}$  (see FIG 9h) is applied to clamping FET switch 134 to establish this voltage as a reference on capacitor 132.

The next signal charge is then read out, representing the "background plus LED" signal. The

final voltage 206 (see FIG. 9f) at node A represents the "background plus LED" signal. This voltage is applied to capacitor 132 by pulsing FET 130 with a pulse  $\phi_E$ . The resulting voltage 208 appearing at node B (see FIG. 9i) is the difference between the "background" signal and the "background plus LED" signal. The voltage 208 is sampled and held on the output of amplifier 142 at node C by pulsing FET 138 with a sampling pulse  $\phi_{S/H}$  (see FIG. 9j).

The voltage at node C is a step-wise smooth curve representing the successive values of the difference signal (see FIG. 9k). Differential amplifier 146 compares the first difference signal value with a threshold value  $V_{TH}$  (see FIG. 9k) stored on capacitor 148. If the sampled value is less than the threshold value  $V_{TH}$ , the output of amplifier 146 at node D remains low. However, if the sampled value exceeds the threshold value  $V_{TH}$ , the output at node D goes high. At a point during the sample period, a sampling signal  $\phi_s$  (see FIG. 9l) is applied to FET switch 152. If the voltage at node D is low at this time, the low value will be applied to the gate of FET switch 150 and will have no effect upon the state of the circuit. If, however, the voltage at node D is high, the high value will be applied to the gate of FET switch 150, thereby applying the new higher reference voltage to capacitor 148. The new reference value is equal to the input at node C, thereby causing the output at node D of differential amplifier 146 to go low (see FIG. 9m). This process continues, producing a pulse at node D each time a new greater difference signal is received from the differencing circuit 110.

At the start of the sequence, counter 118 is initialized. Each time a new charge packet is read

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from the CCD shift register 24, counter 118 is advanced (see FIG. 5). The pulse train produced by the peak detector circuit 114 at node D is applied to latch circuit 116 which latches the output of counter 118 whenever a new pulse is produced by the peak detector circuit 114. After all the charge packets in the CCD shift register 24 have been read out, the count held by latch 116 is indicative of the location of the photosensor 22 having the greatest illumination from the LED, above the threshold level. At this point, the microprocessor 100 retrieves the range data from the latch 116 by interrogating its input port.

The range data are then used in known manner to drive an output device such as a range display or a range servo.

At low ambient light levels, the signal-to-noise ratio of the linear image sensor 18 is limited by the interface state traps in the surface channels connecting the photosensors 22 to the CCD shift register 24. These traps capture some of the charge carriers in each signal as the signals are transferred from the photosensors 22 into alternate cells of the CCD shift register 24. At high ambient light levels, this has little or no effect on the signal-to-noise ratio, since the number of traps is a small percentage of the total number of charge carriers. About the same number of charge carriers are trapped from the "background" signal and from the "background plus LED" signal, leaving no net effect on the difference signals.

On the other hand, at low ambient light levels, the number of traps represents a substantial percentage of the total number of charge carriers produced in a photosensor 22, and may exceed the number of carriers produced. When this occurs, the signal-to-noise ratio is reduced, thereby decreasing

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the likelihood of correctly detecting the location of the LED-illuminated area in the scene.

5       The signal-to-noise ratio of the ranging device may be further improved by initializing the photosensors 22, prior to each operation of the image sensor, with a constant charge. This has the effect of increasing the background illumination, thereby improving the signal-to-noise ratio of the sensor.

10       Referring now to FIGS. 4 and 8, when the photosensors 22 are initialized, a transfer pulse  $T_2$  is applied to transfer gate 32, to lower the potential barrier thereunder to the level 220 shown in FIG. 4. The voltage of transfer pulse  $T_2$  is chosen such that the level 220 is slightly higher than  
15       the level 60 to which the barrier under transfer gate 26 is lowered when transferring charge from the photosensor 22 into the CCD array. With the potential barrier under transfer gate 32 lowered to level 220, the bias voltage  $V_D$  is momentarily changed on drain  
20       28 (e.g. from 5 volts to 2 volts, see pulses indicated in phantom in FIG. 8g) to fill the photodiode 22 with charge, up to level 222 shown in FIG. 4. The bias voltage  $V_D$  is then returned to its normal  
25       value (e.g. 5 volts) and excess charge spills from photodiode 22 over barrier 220, leaving behind a constant charge 224, indicated by shading in FIG. 4. This spill and fill technique is employed each time the photosensors 22 are initialized. This alternative step is indicated in phantom in FIG. 7.

30       Alternatively, a constant charge can be accumulated in the photosensors 22 by emptying the photosensors 22 of charge, then exposing the photosensors 22 directly to a source of illumination, such as an LED, for a predetermined constant time, or by uniformly illuminating the scene, for example, by electronic flash, each time the image sensor 18 is operated.  
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Another means for providing an initial charge in the photosensors 22 is to sense the ambient illumination level, and when it is low, to operate the sensor 18 for longer times, thereby allowing dark current to accumulate in the photosensors 22.

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**CLAIMS:**

1. A rangefinder for finding the range of an object in a scene, comprising a light source selectively energizable for projecting a beam of light to illuminate a small area on the object, a solid state image sensor comprising a linear array of N photosensitive elements, each responsive to light for generating a signal indicative of the amplitude of light incident on it, analog shift register means, adjacent said linear array, for receiving the N signals in parallel into N alternate cells and shifting the signals serially toward an output location, said shift register means having 2N cells, and transfer means responsive to a control signal for transferring said N signals from the array of photosensitive elements into alternate cells of said shift register means, means for forming an image of a portion of the scene containing the illuminated small area on the array of photosensitive elements, and control means for 1) sending a control signal to said transfer means for transferring a first set of N signals into the shift register means from the array, 2) supplying clock control signals to the analog shift register means to shift the signals by one cell, 3) energizing the light source, 4) de-energizing the light source, 5) sending a control signal to said transfer means to transfer a second set of N signals, created with the light source on, into the shift register means, and 6) supplying clock signals to the shift register means to shift the signals therein serially to the output location, and signal processing means, including means for 1) receiving the signals serially from the output location of the image sensor and forming a series of difference signals representative of the difference between the signals of each pair of adjacent signals derived from the same photosensitive element and 2) detecting the location



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of the image of the small illuminated area on the basis of the magnitudes of the difference signals, and forming a range signal on the basis of the detected location of the small illuminated area.

5           2. A rangefinder as claimed in claim 1, further comprising means for establishing a predetermined signal content in said photosensitive elements prior to generating signals in said array.

10           3. A rangefinder as claimed in claim 2, wherein said predetermined signal content is a zero signal.

          4. A rangefinder as claimed in claim 2, wherein said predetermined signal content is a constant, non-zero signal.

15           5. A rangefinder as claimed in claim 2, wherein said photosensitive elements are photodiodes, said analog shift register means is a buried channel charge coupled device (CCD) shift register having alternate cells aligned with said photodiodes, said  
20           transfer means is a first transfer gate responsive to a control signal for forming surface channels between said photodiodes and said alternate cells of said CCD shift register, and wherein said means for  
25           establishing a predetermined signal content in the photosensitive elements comprises drain means adjacent the array of photodiodes and a second transfer gate responsive to a control signal for coupling the photodiodes to said drain means.

30           6. A rangefinder as claimed in any one of claims 1 to 5, wherein said means for detecting the location of the image of said small illuminated area comprises peak detector means responsive to the difference signals for producing a pulse each time a new greater difference signal is received, said peak  
35           detector means comprising a storage capacitor for storing the last greatest difference signal, comparator means for comparing the voltage on said



storage capacitor with the next difference signal and  
producing an output pulse whenever said next  
difference signal is greater than the value on said  
storage capacitor, and switching means responsive to  
5 said output pulse for replacing the signal on said  
storage capacitor with said greater difference signal.

7. A rangefinder as claimed in claim 6,  
further comprising means for introducing a threshold  
value onto said storage capacitor prior to the  
10 operating of said means for detecting.

8. A rangefinder as claimed in claim 1  
substantially as hereinbefore described with reference  
to FIGS. 2 to 9 of the accompanying drawings.

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