

DIFFERENTIAL SENSE AMPLIFIER

The present invention relates to differential sense amplifiers, for example ones suitable for use in a semiconductor memory device.

In order to read out data stored in its memory cells, a semiconductor memory device requires a circuit for decoding addresses to select a series of memory cells, an amplifier for amplifying the data read out from the selected memory cells, and a circuit to output the amplified data. Generally, when fabricating a highly integrated semiconductor memory device with high speed performance, improvements to reliability as well as power consumption are primarily considered.

Particularly, as such a semiconductor memory device becomes more highly integrated, both the operating voltage level of the memory device and the voltage difference between its data lines reduce, so that there is required a sense amplifier which can reliably sense the reduced voltage difference. Amplifiers generally used in such semiconductor memory devices, and particularly in a static random access memory (SRAM), are differential sense amplifiers having two inputs, each one connected to a respective data line of a data line (bit line) pair. The differential sense amplifiers are used to amplify a small voltage difference which occurs between voltages on each of the bit lines.

Such a conventional sense amplifier is generally of a current mirror type, whose fundamental structure is disclosed in U. S. Patent No. 4,697,112 and an article entitled "A 28ns CMOS SRAM With Bipolar Sense Amplifiers", PP. 224-225, IEEE. ISSCC. published on February 23, 1984.

Operation of a various conventional differential sense amplifiers will now be described, with reference to Figures 1, 2, 3, and 6 of the accompanying drawings in which;

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Figure 1 illustrates a basic form of a conventional differential sense amplifier circuit;

10 Figure 2 illustrates a practical form of a conventional differential sense amplifier circuit;

Figure 3 illustrates another practical form of a conventional differential sense amplifier circuit; and

15 Figure 6 shows a graph in which one curve (61) representing a voltage gain versus input voltage characteristic of the conventional differential sense amplifier shown in Figure 2 is shown, and one curve (63) representing a voltage gain versus input voltage
20 characteristic of the other conventional differential sense amplifier as shown in Figure 3 is shown.

Referring to Figure 1 of the accompanying drawings, there is illustrated the conventional sense amplifier
25 circuit disclosed in the above publications. The circuit amplifies a difference between input voltages applied to first and second input terminals 1 and 2. Output voltages appear at first and second output terminals 3 and 4. Since there is no substantial voltage difference between
30 the gate and drain of PMOS transistor 6 where the gate and drain are commonly connected with each other, the output voltage of the first output terminal 3 does not change considerably, in spite of variation of the input signal levels.

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Thus, the effective output of the circuit is obtained through only the second output terminal 4. This circuit

is known as a single ended current mirror type sense amplifier circuit.

5 Because one output terminal does not incur any appreciable changes in output voltage, a practical conventional memory device uses two of the single ended current mirror type sense amplifier circuits for one pair of bit lines, as shown in Figure 2 of the accompanying drawings.

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In Figure 1 or 2 of the accompanying drawings, an NMOS transistor 11 has a source coupled to ground voltage Vss. The transistor 11 is turned off in response to a sense amplifier control signal 10 of a logic "low" state at its gate when the sense amplifier circuit is not operated, thus preventing power consumption by the sense amplifier circuit.

20 An equalization signal 12 applied to an equalization transmission gate 13 connected between a pair of bit lines (or data lines) 15 and 16 equalizes the bit lines 15 and 16 before and after operation of the sense amplifier circuit. During operation of the sense amplifier circuit the equalization signal 12 goes to a logic "high" state so as to cause the output signals of the sense amplifier circuit to appear in the bit lines (or data lines) during the operation thereof.

30 Using the above conventional current mirror type sense amplifier circuits involves the following problems.

35 Firstly, if the voltage levels of the input signals are relatively low or high, the gain of the output voltages becomes small. The reason for this is that although no problem would be caused if a voltage difference were formed between the input voltages which included the threshold voltages of the NMOS transistors 8

and 9 (See Figure 1 of the accompanying drawings), in fact the voltage difference between the first and second output terminals 3 and 4 becomes insignificant because the NMOS transistors have almost the same conductivity as each other if the levels of the two inputs are different but below or above the threshold voltage.

Secondly, operation speed is very low. If the signal received through the first input terminal 1 has a level higher than the level of the signal received at the second input terminal 2, the NMOS transistor 8 reaches a conductive state (compared with its normal state), faster than NMOS transistor 9, thereby lowering the voltage of the first output terminal 3. Consequently, the PMOS transistor 7 is turned on, and charges the second output terminal 4 with the power supply voltage V_{cc} , so that variation between output voltages is caused. The time taken for the output voltage variation depends on the conductivity of the transistor 7 itself, which works in its saturation region, so that the effective output appears relatively slowly.

There has been proposed another conventional sense amplifier, as shown in Figure 3 of the accompanying drawings, which is known as a latch type sense amplifier.

Referring to Figure 3 of the accompanying drawings, the latch type sense amplifier has first and second output terminals 53 and 54 cross-coupled respectively to the gates of PMOS transistors 57 and 56. This structure compensates for a deficiency in positive feedback effect of the above described prior art sense amplifier which is caused by the PMOS transistors 6, 7 coupled to the power supply in the circuit of Figures 1 and 2 working in the saturation region.

However, the sense amplifier of Figure 3 also shows a dropping off of output voltage gain at a low or high level of input signal.

5 Referring to the graph of Figure 6 of the accompanying drawings, it will be readily appreciated from voltage gain curves 61 and 63 respectively representing the voltage gain characteristics of the circuits of Figures 2 and 3, that voltage gain rapidly drops when the
10 level of the input voltage is below 2V or over 3V. The reason for this is that NMOS transistors are used for receiving the input voltages in the circuits of Figures 2 and 3. Thus, the range of input voltage levels or "window" for maintaining a high output voltage gain as
15 described above is narrow.

Moreover, in the conventional circuits of Figures 1, 2 or 3, if the sense amplifier control signal 10 goes logic "low" in order to prevent power consumption when the
20 sense amplifier is not operating, the NMOS transistor 11 is turned off, thereby disconnecting the currents flowing through the NMOS transistors 8, 9 or 58, 59 as appropriate, and the voltages of the first and second output terminals 3, 4 or 53, 54 rise until the PMOS
25 transistors 6, 7 or 56, 57 are turned off.

Thus, when above sense amplifiers are in an unoperated condition, the voltage levels of both output terminals in each of the above sense amplifiers tend
30 towards the same value as each other, so that a loss of the original output signal of the sense amplifier will occur.

Accordingly, specific embodiments of the present
35 invention aim to provide a differential sense amplifier for a semiconductor memory device, which has a high operating speed as well as a high voltage gain.

Specific embodiments of the present invention also aim to provide a differential sense amplifier wherein power consumption is prevented during periods when the sense amplifier is not being operated and wherein an additional latch circuit is not required for maintaining an output voltage level when the sense amplifier is not operated.

It is still another object of the specific embodiments of the present invention to provide a differential sense amplifier, whereby a stable and effective output voltage gain is obtained even at a low or high level of input voltage.

According to the present invention there is provided a differential sense amplifier for amplifying a voltage difference between voltage levels of a pair of input signals, said amplifier comprising;

a pair of first complementary drive means, each first complementary drive means having an output, said pair of first complementary drive means arranged to produce a pair of output signals in response to said pair of input signals, each output signal of the output signal pair arranged to adopt a different state to a state of the other output signal of said pair;

a pair of output terminals respectively connected with the outputs of said pair of complementary drive means and for carrying said pair of output signals;

a pair of second complementary drive means connected with said pair of output terminals to respectively respond to said output signals of different states of said first complementary drive means, wherein an input (or output) of one of said pair of second complementary drive means is coupled to an output (or input) of the other of one of

said pair of second complementary drive means and to one of said pair of output terminals.

5 Said pair of first complementary drive means may be arranged to be connected to a ground voltage by a first switching means coupled between the ground voltage and said pair of first complementary drive means, said first switching means being operated according to a control signal.

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Said pair of first complementary drive means may be arranged to be connected to a supply voltage by a second switching means coupled between said pair of first complementary drive means and the supply voltage, said
15 second switching means being arranged to be switched according to a control signal.

Preferably, a said complementary drive means comprises at least two insulated gate transistors
20 connected in series, said insulated gate transistors having different operating voltages.

Preferably, each second complementary drive means of said pair of second complementary drive means comprises at
25 least two insulated gate transistors connected in series.

Said pair of second complementary drive means may be connected between a power supply voltage and a ground voltage.

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Preferably, the differential sense amplifier has first and second output terminals, in which at least one pair of insulated gate field effect transistors are arranged to be complementarily driven according to
35 voltage(s) of the first and/or second output terminals.

Specific embodiments of the present invention will now be described, by way of example only, with reference to Figures 4 to 8 of the accompanying drawings, in which:

5 Figure 4 illustrates a differential sense amplifier circuit according to a first specific embodiment of the present invention;

10 Figure 5 shows operational waveforms of a differential sense amplifier circuit, for example one as described herein with reference to Figure 4;

15 Figure 6 shows a graph in which a curve representing a voltage gain versus input voltage characteristic of the first specific embodiment illustrated in Figure 4 is compared with voltage gain versus input voltage characteristics of conventional circuits; and

20 Figures 7 to 8 illustrate other various specific embodiments of the present invention.

Referring to Figure 4 of the accompanying drawings, a differential sense amplifier circuit 100 includes a first complementary input inverter 124 having a first
25 input terminal 101, and a second complementary input inverter 125 having a second input terminal 102. The first complementary input inverter 124 consists of PMOS and NMOS transistors 105 and 106 coupled in series. The second complementary input inverter 125 consists of PMOS
30 and NMOS transistors 107 and 108 coupled in series. The first complementary input inverter 124 also has an output connected with a first output terminal 103 which in turn is coupled to the output of a first complementary inverter 126 and the input of a second complementary inverter 127.
35 The second complementary input inverter 125 has an output connected with a second output terminal 104, which in turn is connected with the output of the second complementary

inverter 127 and the input of the first complementary inverter 126.

5 The first complementary inverter 126 consists of PMOS
and NMOS transistors 110 and 111 connected in series. The
second complementary inverter 127 consists of PMOS and
NMOS transistors 112 and 113 connected in series. To the
common sources of PMOS transistors 105 and 107 of the
first and second complementary input inverters 124 and 125
10 respectively, is connected power supply Vcc from which is
supplied power through the channel of a PMOS transistor
109 having a gate which may receive a negative sense
amplifier control signal $\overline{SAE}$. Also between the common
source of NMOS transistors 106 and 108 of the first and
15 second complementary input inverters 124 and 125
respectively and the ground voltage Vss, is connected the
channel of an NMOS transistor 115 having a gate which may
receive a positive sense amplifier control signal SAE.
The first and second output terminals 103 and 104 are
20 respectively connected with data lines 119 and 120 which
form a data line pair.

 An equalization circuit 123 is connected between the
data lines 119 and 120. The equalization circuit 123 may
25 be a conventional equalisation circuit, functioning
similarly as hereinbefore described with reference to
Figures 1, 2 or 3 above.

 Hereinafter, for convenience of description, the
30 terms "differential sense amplifier" and "sense amplifier"
are used interchangeably to mean the same thing.

 The PMOS and NMOS transistors 109 and 115,
respectively connected with the power supply Vcc and the
ground voltage Vss, are turned off in response to the
35 positive sense amplifier control signal SAE of a logic
"low" state (or the negative sense amplifier control

signal $\overline{SAE}$ of a logic "high" state) so as to prevent power consumption when the differential sense amplifier is not operated (i.e. when it is in a standby state). Additionally, the first and second complementary inverters
5 126 and 127 serve as a latch circuit for maintaining the logic states of the output terminals 103 and 104 when the sense amplifier is in the standby state.

Referring to Figure 5 of the accompanying drawings
10 illustrating the operational waveforms of the sense amplifier circuit of Figure 4, reference letter A represents an address signal, B represents the level of an input signal, C represents an equalization signal EQ applied to the equalization circuit 123 to equalize the
15 data line pair, D represents positive sense amplifier control signal SAE, and E represents the output signals on data lines 119 and 120.

Figure 6 of the accompanying drawings compares
20 voltage gain versus input voltage characteristics of the conventional sense amplifiers of Figures 2 and 3 of the accompanying drawings with those of the sense amplifier circuit of Figure 4 of the accompanying drawings. The voltage gain of each sense amplifier circuit is
25 represented on a y-axis of the graph, and an input voltage level to the respective sense amplifier is represented on an x-axis of the graph. The curves 61, 63 and 65 respectively represent characteristics obtained for the sense amplifiers of Figures 2, 3 and 4 of the accompanying
30 drawings. The characteristics were obtained using the same power supply voltage in each case.

Operation of the first sense amplifier circuit will now be described with reference to Figures 4, 5 and 6 of
35 the accompanying drawings.

Before a sensing operation of the sense amplifier 100, the equalization signal (EQ) C goes to a logic "low" state, enabling the equalization circuit 123 to equalize the pair of data lines 119 and 120 to a given equalization level. In the case of a SRAM, the equalization level of the data lines is generally the level of the power supply voltage Vcc, or thereabouts.

If the data lines are equalized, the sense amplifier control signal (SAE) D, going to a logic "high" state, enables the sense amplifier 100 to perform the sensing function.

Assuming the signal level of the first input terminal 101 is higher than that of the second input terminal 102, the output of the first complementary input inverter 124 gradually goes to a low level, while the output of the second complementary input inverter 125 goes to a level which is higher than the output of the first complementary input inverter 124. Namely, the NMOS transistor 106 of the first complementary input inverter 124 conducts more current to ground via the NMOS transistor 115 than the NMOS transistor 108 of the second complementary input inverter 125, which also conducts current to ground via the NMOS transistor 115, but less so than NMOS transistor 106.

Then, the voltage level of the first output terminal 103 becomes lower than that of the second output terminal 104, and therefore because the input of the second complementary inverter 127 is connected to the first output terminal 103, the output of the second complementary inverter 127 reaches a "higher" state than the output of the first complementary inverter 126. Thus, the second output terminal 104, which is connected to the output of the second complementary inverter 127 goes to a higher state due to the effect of positive feedback.

Since the output of the second complementary inverter 127 is also coupled to the input of the first complementary inverter 126, the output of the first complementary inverter 126 goes more and more to the logic "low" state. As a result, the present states of the output terminals are kept stable as long as the voltage levels of the first and second input terminals 101 and 102 are not changed.

In addition, when the voltage level of the first output terminal 103 is decreased and that of the second output terminal 104 is increased, the NMOS transistor 113 of the second complementary inverter 127 and the PMOS transistor 110 of the first complementary inverter 126 are turned off, so that the DC current consumed via the first and second complementary inverters 126 and 127 is reduced. Alternatively, if the voltage level of the first input terminal 101 is lower than that of the second input terminal 102, a similar effect is obtained, whereby NMOS transistor 111 of the first complementary inverter 126, and PMOS transistor 112 of the second complementary inverter are turned off.

Thus, an amplified output signal E is loaded onto the pair of bit lines (or data lines) 119 and 120 via the first and second output terminals 103 and 104. The output voltage gain of the sense amplifier circuit of Figure 4 is kept stable and does not substantially change even at a low or high level (lower than about 2V or higher than about 3V) of the input voltage, as shown by the curve 65 in the graph of Figure 6 of the accompanying drawings.

Figure 7 of the accompanying drawings illustrates a second differential sense amplifier circuit, according to a second embodiment of the present invention. The second differential sense amplifier differs from the first embodiment shown in Figure 4 in that first and second

complementary inverters 126 and 127 of the second differential amplifier are connected through NMOS transistor 115 (of which only the terminal is shown) to the ground voltage, together with the first and second complementary input inverters 124 and 125. However, operations of the circuits shown in Figure 4 or 7 are substantially the same or similar.

The second sense amplifier circuit of Figure 7 is operated in substantially the same or similar manner as that of Figure 4 except for the ground connections of the first and second inverters 126 and 127, which are disconnected from ground by transistor 115 (not shown) when the second sense amplifier circuit is not performing a sensing function.

Referring to Figures 4 and 7 of the accompanying drawings, illustrating sense amplifier circuits according to various embodiments of the present invention, the sense amplifier circuit shown in Figure 4 is similar to the sense amplifier circuit shown in Figure 7, except for the ground connection arrangements of first and second complementary inverters 126 and 127.

The sense amplifier circuits of Figures 4 and 7 each receive input signals via CMOS inverter circuits (i.e.) the complementary input inverters 124, 125).

Referring to Figure 8 of the accompanying drawings illustrating a third differential sense amplifier circuit according to a third embodiment of the present invention, there is provided a sense amplifier circuit similar to the first and second sense amplifier circuits, but which has no PMOS transistor 109 for connection of a power supply voltage.

The sense amplifier circuit of Figure 8 works substantially in the same manner as those of Figure 4 or 7.

5 Besides the above described specific embodiments, it will be readily appreciated by one skilled in this art that various other embodiments may be obtained without departing from the scope of the present invention.

10 As described above, certain embodiments of the present invention use CMOS inverter circuits for receiving input signals so as to amplify a voltage difference between the input signals. Thus these embodiments may expand the effective operation region of a sense amplifier
15 circuit.

 Additionally, embodiments of the present invention may respond to the voltage levels of a pair of output terminals so as to maintain a stable output signal with a
20 large gain and may increase the speed of operation of a sense amplifier circuit.

 Moreover, specific embodiments of the present invention may provide means for preventing DC current
25 flowing between a power supply and ground in an inoperative state of a sense amplifier, thus reducing power consumption.



CLAIMS

1. A differential sense amplifier for amplifying a voltage difference between voltage levels of a pair of input signals, said amplifier comprising;

10 a pair of first complementary drive means, each first complementary drive means having an output, said pair of first complementary drive means arranged to produce a pair of output signals in response to said pair of input signals, each output signal of the output signal pair arranged to adopt a different state to a state of the other output signal of said pair;

15 a pair of output terminals respectively connected with the outputs of said pair of complementary drive means and for carrying said pair of output signals;

20 a pair of second complementary drive means connected with said pair of output terminals to respectively respond to said output signals of different states of said first complementary drive means, wherein an input (or output) of one of said pair of second complementary drive means is coupled to an output (or input) of the other of one of said pair of second complementary drive means and to one of said pair of output terminals.

2. A differential sense amplifier as claimed in Claim 1, wherein said pair of first complementary drive means is arranged to be connected to a ground voltage by a first switching means coupled between the ground voltage and said pair of first complementary drive means, said first switching means being operated according to a control signal.

35 3. A differential sense amplifier as claimed in Claim 1 or 2, wherein said pair of first complementary drive means

is arranged to be connected to a supply voltage by a second switching means coupled between said pair of first complementary drive means and the supply voltage, said second switching means being arranged to be switched
5 according to a control signal.

4. A differential sense amplifier as claimed in any preceding claim, wherein a said complementary drive means comprises at least two insulated gate transistors
10 connected in series, said insulated gate transistors having different operating voltages.

5. A differential sense amplifier as claimed in claim 4 wherein each second complementary drive means of said pair
15 of second complementary drive means comprises at least two insulated gate transistors connected in series.

6. A differential sense amplifier as claimed in any one of the preceding claims, wherein said pair of second
20 complementary drive means is connected between a power supply voltage and a ground voltage.

7. A differential sense amplifier according to any one of the preceding claims, having first and second output
25 terminals, in which at least one pair of insulated gate field effect transistors are arranged to be complementarily driven according to voltage(s) of the first and/or second output terminals.

8. A differential sense amplifier substantially as
30 hereinbefore described with reference to Figure(s) 4, 7 and/or ⁸~~12~~ of the accompanying drawings.

