Improved Semiconductor Sensor Structures with Reduced Dislocation Defect Densities and Related Methods for the Same

TECHNICAL FIELD OF THE DISCLOSURE

[0001] The technical field of this disclosure relates to the art of semiconductor devices; and more particularly to the art of methods of making semiconductor devices using aspect-ratio-trapping techniques and semiconductor devices made thereof.

BACKGROUND OF THE DISCLOSURE

[0002] There is a constant drive within the semiconductor industry to increase the performance and reduce the cost of semiconductor devices, such as photodetectors, diodes, light-emitting diodes, transistors, latches, and many other semiconductor devices. This drive has resulted in continual demands for integrating one type of semiconductor devices into another semiconductor process.

[0003] For example in photodetectors that are comprised of an array of ***p-n*** junctions or **p-i-n** structures, it is advantages to make the ***p-n*** junctions and/or **p-i-n** structures with low band-gap materials, such as germanium (Ge) and InGaAs, because the photodetectors are able to detect infrared light. In favor of the cost-efficiency, it is desired to produce a thin film of III-V or other non-silicon materials on low-cost large-size silicon wafers to reduce the cost of high performance III-V devices. It is further desired to integrate non-silicon ***p-n*** junctions and/or **p-i-n** structures (*e.g.* Ge or InGaAs based) into a silicon process such that other circuitry in a systems, such as a photodetector, can be fabricated using a standard silicon process, such as a standard CMOS (complementary-metal-oxide-semiconductor) process. It is also desirable to fabricate the non-silicon devices and silicon CMOS in a co-planar manner, so that the interconnection and integration of the whole system can be conducted in a manner compatible with standard and low-cost CMOS process. Further, it is desirable to increase a size of non-silicon regions configured to output electrons generated by light absorption therein.

BRIEF DESCRIPTION OF DRAWINGS

[0004] FIG. 1a through FIG. 1d diagrammatically illustrate an exemplary method of making a semiconductor device;

[0005] FIG. 2 diagrammatically illustrates a cross-sectional view of an exemplary structure having an epitaxial-lateral-overgrowth at or in which a semiconductor device can be fabricated;

[0006] FIG. 3 diagrammatically illustrates a cross-sectional view of an exemplary structure having a large lateral intrinsic region;

[0007] FIG. 4 diagrammatically illustrates a top view of an exemplary layout of multiple trenches in a substrate capable for growing epitaxial crystalline materials;

[0008] FIG. 5 diagrammatically illustrates an exemplary structure having non-silicon semiconductor devices integrated in a silicon process;

[0009] FIG. 6 diagrammatically illustrates an exemplary structure having a ***p-i-n*** structure formed in a shallow-trench-insulator region;

[0010] FIG. 7 diagrammatically illustrates another exemplary structure having a ***p-i-n*** structure formed in a shallow-trench-insulator region;

[0011] FIG. 8 is a diagram of a portion of an exemplary array of photodetectors;

[0012] FIG. 9 diagrammatically illustrates an energy-band structure of a ***p-i-n*** structure at zero bias voltage;

[0013] FIG. 10 diagrammatically illustrates the energy-band structure of the ***p-i-n*** structure in FIG. 9 at a bias voltage;

[0014] FIG. 11 is a diagram showing a portion of the array of photodetectors in FIG. 8;

[0015] FIG. 12 diagrammatically illustrates an exemplary configuration of the transistors in the photodetector array in FIG. 8;

[0016] FIG. 13 diagrammatically illustrates another exemplary configuration of the transistors in the photodetector array in FIG. 8;

[0017] FIG. 14 diagrammatically illustrates an exemplary configuration of the ***p-i-n*** structure connected to a transistor in the photodetector array in FIG. 8;

[0018] FIG. 15 diagrammatically illustrates a cross-sectional view of an exemplary semiconductor device formed at or in a coalesced region formed by adjacent ART (aspect-ratio-trapping) structures;

[0019] FIG. 16 diagrammatically illustrates a cross-sectional view of another exemplary semiconductor device formed at or in a coalesced region formed by adjacent ART (aspect-ratio-trapping) structures;

[0020] FIG. 17 diagrammatically illustrates a cross-sectional view of an exemplary structure having a semiconductor device formed on a graded buffer layer in an opening of a dielectric layer;

[0021] FIG. 18 diagrammatically illustrates a cross-sectional view of an exemplary structure having a semiconductor device formed on a graded buffer layer in a trench formed in a crystalline substrate;

[0022] FIG. 19a diagrammatically illustrates a cross-sectional view of a portion of an exemplary array of non-silicon photodetectors integrated in a silicon substrate, wherein the photodetector is capable of detecting light incident thereto from the top;

[0023] FIG. 19b diagrammatically illustrates a top view of a portion of the photodetectors in FIG. 19a;

[0024] FIG. 20a diagrammatically illustrates a cross-sectional view of a portion of an exemplary array of non-silicon photodetectors integrated in a silicon substrate, wherein the photodetector is capable of detecting light incident thereto from the side;

[0025] FIG. 20b diagrammatically illustrates a top view of a portion of the photodetectors in FIG. 20a;

[0026] FIG. 21a and FIG. 21b diagrammatically illustrate an exemplary configuration of electrical connections of photodetectors to electrical contacts; and

[0027] FIG. 22 is a cross-section of an exemplary semiconductor device having a non-isolated defect region.

DETAILED DESCRIPTION OF SELECTED EXAMPLES

[0028] Disclosed herein is a method of making semiconductor devices and semiconductor devices made thereof.

[0029] The method enables integration of non-silicon semiconductor devices into a silicon process such that silicon circuitry of the semiconductor device can be formed through standard silicon processes. This integration capability can be of great importance in using low band-width or high band-width semiconductor materials for making semiconductor device having ***p-n*** and ***p-i-n*** structures in silicon processes.

[0030] The method also enables forming ART (aspect-ratio-trapping) crystalline structures in a trench structure, such as a trench structure patterned by a trench patterning-process (*e.g.* a standard complementary-metal-oxide-semiconductor (CMOS) STI (shallow-trench-insulation) process) or a STI-like trench patterned structure. The semiconductor devices formed at or in the ART structure(s) can have any desired lateral and/or vertical dimensions that are substantially free from the aspect-ratio requirements or process limitations in most current ART techniques. For demonstration and simplicity purposes, the method will be discussed with reference to selected examples wherein ART crystalline structures are formed on STI process trench structures in some of the examples. It will be appreciated by those skilled in the art that the exemplary methods as discussed in the following can also be implemented to form ART structures on other types of trenches.

[0031] Aspect Ratio Trapping (ART) is a defect reduction and heteroepitaxy growth technique. As used herein, "ART" or "aspect ratio trapping" refers generally to the technique(s) of causing defects to terminate at non-crystalline, *e.g.*, dielectric sidewalls during heteroepitaxy growth, where the sidewalls are sufficiently high relative to the size of the growth area so as to trap most, if not all, of the defects. ART utilizes high aspect ratio openings, such as trenches or holes, to trap dislocations, preventing them from reaching the epitaxial film surface, and greatly reduces the surface dislocation density within the ART opening. Further details of example ART devices and ART techniques in which this invention are described in U.S. Patent Application Nos. 11/436,198

filed May 17, 2006, 11/493,365 filed July 26, 2006 and 11/852,078 filed September 7, 2007, all of which are hereby incorporated by reference.

[0032] Furthermore, with customized ART growth parameters, an enhanced lateral epitaxy overgrowth (ELO) mode may be realized for expanded epitaxy beyond the trenched region, e.g., regions with openings formed therein, which yields bulky "free-standing" high quality materials centered above the initial trenched seed layer. Therefore, a combined ART and ELO technology greatly increases the quality and applicable film surface area of lattice-mismatched materials on substrates such as Si substrates. The relatively simple process enables reliable and reproducible results.

[0033] The method further enables forming a large-scale ART structure in the presence of STI process trenches, which in turn enables forming a semiconductor device or an element of a semiconductor device with desired lateral or vertical dimension. In particular, a large-scale intrinsic semiconductor region can be formed in the large-scale ART structure.

[0034] The method enables forming a semiconductor device or an element of a semiconductor device on a buffer layer disposed on a semiconductor crystalline substrate, whereas the buffer layer can be graded. The buffer layer can be disposed within an opening formed in a dielectric layer or can be disposed in a trench formed in a crystalline substrate.

[0035] The method also enables forming anisotropic or isotropic ELO (epitaxial-lateral-overgrown) regions, at or in which a semiconductor element or a semiconductor device can be formed.

[0036] The method also enables forming semiconductor devices or elements of semiconductor devices in coalesced regions between adjacent ART structures.

[0037] The method also enables forming lateral ***p-n*** and ***p-i-n*** structures of semiconductor devices at or in an ART structure.

[0038] In a particular implementation, the method is capable of being used for making a semiconductor device having complementary-metal-oxide-semiconductor device with a

photodetector that is formed at or in an ART structure. Other non-silicon or silicon based circuitry can also be formed along with the photodetector.

[0039] The method and semiconductor devices made thereof will be discussed in the following with selected examples. It will be appreciated by those skilled in the art that the following discussion is for demonstration purposes and should not be interpreted as a limitation. Other variations within the scope of this disclosure are also applicable.

[0040] Referring to the drawings, FIG. 1a through FIG. 1d diagrammatically illustrate an exemplary method of making an epitaxial structure using an aspect-ratio-trapping (ART) technique. Referring to FIG. 1a, substrate 100 is provided, which can be a semiconductor crystalline substrate, such as a silicon substrate. Dielectric layer 102 comprised of a dielectric material is deposited on substrate 100. The dielectric material can be any suitable materials, which is preferably, though not required, an oxide or nitride of a semiconductor element, such as SiO_x and SiN_x. Other materials are also applicable, such as an oxide or nitride of a metal element, a metal alloy, or a ceramic material.

[0041] Screen layer 104 is deposited on dielectric layer 102. The screen layer is comprised of a material that is highly selective to the etching process to be used for etching substrate 100. For example, screen layer 104 can be comprised of TiN_x when a dry etching process is to be performed for forming trenches in substrate 100.

[0042] The substrate (100) can be etched by a selected etching process so as to form openings, such as opening 106 in FIG. 1b. Due to the selectivity of the screen layer (104) to the etching process, the trench (*e.g.* 106) in the substrate (100) can have a larger depth or width while still maintaining the desired aspect ratio for the following ART growth. In one example, the opening (106) can have a depth of 100 nanometers or larger, 200 nanometers or larger, 500 nanometers or larger, 1 micron or larger, such as 1.5 micron or larger, 2 microns or larger, 3 microns or larger, or 5 microns or larger. The opening (106) may have a width of 20 nanometers or larger, 100 nanometers or larger, 500 nanometers or larger, 1 micron or larger, such as 1.5 micron or larger, 2

microns or larger, 3 microns or larger, or 5 microns or larger. The aspect ratio of the opening (106) can be 0.5 or higher, such as 1 or higher, 1.5 or higher.

[0043] The opening can then be filled with a selected dielectric material so as to coat the sidewalls (108) of the opening for the following ART growth in the opening. In one example, dielectric layer (108) at the sidewalls of the opening can be comprised of an oxide (*e.g.* SiO_x), a nitride, (*e.g.* TiN_x), or other suitable materials. In another example, the dielectric layer (108) at the sidewall of the opening can be comprised of TiN_x or a material having a free- surface energy substantially equal to or higher than that of TiN_x.

[0044] After coating the sidewalls of the opening (106), the dielectric layer can be etched so as to remove the dielectric material at the bottom portion (110) of the opening for exposing the underneath substrate (100), as diagrammatically illustrated in FIG. 1c.

[0045] In the formed opening 106 as shown in FIG. 1c, an ART process can be performed so as to form epitaxial material 112 as diagrammatically illustrated in FIG. 1d. Exemplary methods for ART processes are set forth in U.S. Patent Application Nos. 11/436,198 filed May 17, 2006, 11/493,365 filed July 26, 2006 and 11/852,078 filed September 7, 2007, all of which are hereby incorporated by reference in entirety. The ART structure is comprised of a semiconductor material. For example, the ART structure may be comprised of a group IV element or compound, a III-V or III-N compound, or a II-VI compound. Examples of group IV elements include Ge and Si; and examples of group IV compounds include SiGe (examples of III-V compounds include aluminum phosphide (AlP), gallium phosphide (GaP), indium phosphide (InP), aluminum arsenide (AlAs), gallium arsenide (GaAs), indium arsenide (InAs), aluminum antimonide (AlSb), gallium antimonide (GaSb), indium antimonide (InSb), and their ternary and quaternary compounds. Examples of III-N compounds include aluminum nitride (AlN), gallium nitride (GaN), indium nitride (InN), and their ternary and quaternary compounds. Examples of II-VI compounds includes zinc selenide (ZnSe), zinc telluride (ZnTe), cadmium selenide (CdSe), cadmium telluride (CdTe), zinc sulfide (ZnS), and their ternary and quaternary compounds.

[0046] The above method of forming ART epitaxial structures and the epitaxial ART structures made thereof have many advantages. For example wherein the substrate is a silicon substrate, a non-silicon crystalline material, such as germanium or other semiconductor materials, can be formed in the trench of the substrate. As a consequence, a non-silicon semiconductor device can be formed at or in the non-silicon crystalline ART material, such as a germanium based ***p-n*** or ***p-i-n*** structure. Other silicon circuitry of the semiconductor device can thus be formed in or at the silicon substrate using standard silicon processes, as example of which will be described afterwards with reference to FIG. 5.

[0047] In another example, the above method enables photodetector pixels to be integrated into a silicon process. A photodetector pixel comprises a ***p-n*** or ***p-i-n*** structure and associated circuitry, such as signal converting circuits. In some applications, it is desired to make the ***p-n*** or ***p-i-n*** structure using a low band-gap material, such as Ge, InGaAs, SiGe, and InP for detecting infrared light. In some other examples, a ***p-n*** junction made from a high band-gap semiconductor material, such as GaN and InP) is desired for detecting ultra-violet light. The non-silicon semiconductor elements (*e.g.* the ***p-n*** junction or ***p-i-n*** structure) can be formed at or in the ART epitaxial structure comprised of the non-silicon semiconductor material, such as Ge and InGaAs. Other circuitry of the photodetector can be formed by using standard silicon processes, such as a standard CMOS process. When the photodetector is desired to have a size larger than a critical threshold, such as equal to or larger than 2 microns, or from 2 to 5 microns, an opening in the silicon substrate can be made to have a width equal to or larger than the desired size of the photodetector, such as equal to or larger than 2 microns, or from 2 to 5 microns. The ART epitaxial crystalline structure formed in the opening can thus have a width equal to or larger than the desired size of the photodetector. Further, desired A/R can simultaneously be maintained.

[0048] In addition to forming an ART epitaxial crystalline structure within a wide opening in a substrate, an ART with a large dimension can alternatively be obtained through overgrowing, as diagrammatically illustrated in FIG. 2. Referring to FIG. 2, an opening can have a width W_b is formed in a substrate using, for example a STI technique. By overgrowing the ART crystalline

structure (114) within the opening, an overgrown crystalline portion (116) can be obtained. The overgrown crystalline portion (116) can have a height H that is 1.5 times or more, 2 times or more, 5 times or more, 10 times or more, or from 5 to 10 times of the height of the opening formed in the substrate. The overgrown crystalline portion (116) can have a width W that is 1.5 times or more, 2 times or more, 5 times or more, 10 times or more, or from 5 to 10 times of the width W_b of the opening formed in the substrate.

[0049] The large lateral dimension of the overgrown portion (116) can also be obtained from ELO (epitaxial-lateral-overgrowth). The ELO can be isotropic or anisotropic. For obtaining a flat surface of the overgrown portion (116), a CMP (chemical mechanical polishing) process can be performed. The overgrown portion (116) can further be patterned so as to obtain desired dimensions (lateral and vertical dimensions and/or the shape) using for example, a photolithography process.

[0050] A semiconductor device or an element of a semiconductor device having a large size (*e.g.* equal to or larger than 2 microns) can then be formed in the overgrown crystalline portion (116). For example, a ***p-n*** or ***p-i-n*** structure with a size of 100 nanometers or more, 500 nanometers or more, 1 micron or more, 2 microns or more, 5 microns or more, or 10 microns or more, or from 5 to 10 microns can be formed at or in the overgrown crystalline portion (116).

[0051] Large ART crystalline structures can alternatively be obtained by forming the ART crystalline structure within a large trench formed in a substrate, as diagrammatically demonstrated in FIG. 3. Referring to FIG. 3, an opening with a large width, such as 100 nanometers or larger, 500 nanometers or larger, 1 micron or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, or 100 microns or larger, and more preferably from 100 nanometers to 20 microns, and more preferably, from 2 to 5 microns, is formed in substrate 100 that can be a semiconductor crystalline substrate, such as a silicon substrate. Dielectric patterns, such as dielectric sidewall 101 and dielectric isolators 120 and 124 can be formed in the opening. The dielectric patterns are provided for enabling the following ART processes for forming ART epitaxial crystalline structures 118, 122, 126, and 128. Specifically, the dielectric patterns 101 and 120 define an opening with an aspect

ratio commensurate with the aspect ratio needed for forming an ART epitaxial crystalline structure in the opening between patterns 101 and 120. The dielectric patterns 120 and 124 define an opening with an aspect ratio commensurate with the aspect ratio needed for forming an ART epitaxial crystalline structure in the opening between patterns 120 and 124. The dielectric patterns 124 and 103 define an opening with an aspect ratio commensurate with the aspect ratio needed for forming an ART epitaxial crystalline structure in the opening between patterns 124 and 103. Such dielectric patterns can be formed in multiple layers (e.g., stacked three or more vertically).

[0052] The dielectric patterns can be formed in many ways. In one example, after forming the large trench in substrate 100 by for example, a STI process, a dielectric layer having a dielectric material for dielectric patterns is deposited in the large opening. The deposited dielectric layer can be patterned to have a depth H_d measured from the bottom of the large opening to the top surface of the patterned dielectric layer. The depth H_d can have any suitable values, which is preferably equal to or larger than the threshold height within which the ART epitaxial structure formed in an opening (*e.g.* the opening between dielectric pattern 101 and 120) has dislocation defects.

[0053] The patterned dielectric layer in the large opening can be further patterned so as to form dielectric patterns 101, 120, 124, and 103. The bottom portions of the openings between dielectric patterns 101 and 120, between 120 and 124, and between 124 and 103 are removed so as to expose the substrate 100.

[0054] With the dielectric patterns formed in the large opening, an ART process can be performed so as to form ART epitaxial structures 118, 122, and 126. By overgrowing the ART structures 118, 122, and 126, overgrown crystalline portion 128 with a large size can be obtained. The overgrown crystalline portion (128) can have a width W_{in} that is substantially equal to the width of the large opening formed in substrate 100. For example, the overgrown crystalline portion (128) can have a width W_{in} of 100 nanometers or larger, 500 nanometers or larger, 1 micron or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, or 20 microns or larger, and more preferably, from 2 to 5 microns.. A semiconductor device or an element of a semiconductor device with a desired large size (*e.g.* 100 nanometers or larger, 500 nanometers or larger, 1 micron

or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, or 20 microns or larger, and more preferably, from 2 to 5 microns) can thus be formed at or in the overgrown crystalline portion (128).

[0055] The openings formed in a substrate by using trenches, recesses, openings or the like as described above can have any desired shapes or layouts, an exemplary of which is diagrammatically illustrated in a top view in FIG. 4. Referring to FIG. 4, an opening can have other shapes such as a 90° angle shape, such as opening 130. Of course, an opening can have other shapes, such as circular, donut, polygonal, and many other possible shapes. Multiple openings can be formed in the opening with any desired layouts. For example, rectangular openings 134 and 132 can be perpendicular or parallel or can be arranged to have any desired angles therebetween.

[0056] Exemplary methods as described above with reference to FIG. 1a through FIG. 1d or FIG.2 can enable integration of non-silicon semiconductor devices into a silicon process. For demonstration purposes, FIG. 5 diagrammatically illustrates one of the examples. Referring to FIG. 5, openings are formed by using a STI process in silicon substrate 100. Germanium (or InGaAs or other semiconductor materials such as a III-V group semiconductor material) ART crystalline structures 138 and 140 are formed in the STI openings in silicon substrate 100. Germanium based (or InGaAs or other semiconductor materials such as a III-V group semiconductor material based) semiconductor devices 146 and 150, such as photodetectors are formed at ART structures 138 and 140. A buffer layer (e.g., 10-100nm) can be between the substrate 100 and the ART crystalline structures 138 and 140 for bonding, adhesion or improved device characteristics purposes. Silicon based devices or elements of semiconductor devices 144, 148 and 152 are formed at the patterns of substrate 100 using standard silicon processes, such as CMOS processes. As such, non-silicon semiconductor devices of elements of non-silicon based semiconductor devices are integrated (e.g., co-planar) in the silicon process.

[0057] In examples of forming ART epitaxial structures in STI trenches that are formed in a substrate, such as a silicon substrate, the substrate patterns, such as the silicon patterns around the openings, can be treated. For example, the substrate patterns can be intentionally passivated for

protecting the substrate patterns and the ART structures. This can be of great importance when the thermal and/or mechanical properties of the substrate and the ART structures mismatch, which may cause physical and/or chemical damages to the ART structures and/or to the substrate patterns due to the mismatch. For example, physical damages may occur to the ART structures and/or the substrate patterns when the CET (coefficient-of-thermal-expansion) of the ART structures and the substrate patterns do not match. In one example, the substrate patterns can be passivated by oxidization or nitridization so as to form a protection layers on the exposed surfaces of the substrate patterns or the interfaces between the substrate patterns and the ART structures.

[0058] As an exemplary implementation of the method and the structure as described above with reference to FIG. 2, an exemplary structure having a ***p-i-n*** structure formed in an ART epitaxial crystalline structure is diagrammatically illustrated in FIG. 6. Referring to FIG. 6, STI trench 107 is formed in semiconductor substrate 100, which can be a silicon substrate or other semiconductor substrates. Isolation patterns 154 and 155 are formed within the STI trench (107) and define opening 157 therebetween. Opening 157 can have a height that is substantially equal to or larger than the critical height under which the ART crystalline structure formed in the opening 157 has dislocation defects and above which the ART crystalline structure is substantially free from dislocation defects. An ART epitaxial crystalline structure can be grown in opening 157. By overgrowing the ART structure in opening 157, a large ART overgrown portion 156 is obtained.

[0059] A ***p-i-n*** structure having ***p***-type region 158, intrinsic region 160, and ***n***-region 162 is formed in overgrown crystalline portion 156. The ***p***-type region 158 and the ***n***-type region 162 can be obtained by doping. Because the overgrown crystalline portion 160 can have a large size, such as 100 nanometers or larger, 500 nanometers or larger, 1 micron or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, or 20 microns or larger, and more preferably, from 2 to 5 microns, the intrinsic ***i*** region 160 can be large, such as 100 nanometers or larger, 500 nanometers or larger, 1 micron or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, and more preferably, from 2 to 5 microns.

[0060] Other circuitry can be formed on the patterned semiconductor substrate 100, such as the transistor having source 164, gate 166, and drain 168, the transistor having source 170, gate 172, and drain 174, and the transistor having source 178, gate 180, and drain 182. The source, gate, and drain of a transistor can be formed by a standard silicon process, such as a CMOS process. For example, the sources and drains of the transistors can be formed by doping; and the gates of the transistors can be formed by a standard silicon based lithography process. Other features can also be formed in the substrate (100). For example, isolation unit 176 can be formed between transistors so as to isolating the transistors. In one example, the semiconductor device (*e.g.* 156) formed on the ART structure can be substantially coplanar with one or more other semiconductor devices (*e.g.* transistors) on substrate 100. For example, the top surfaces of 158, 160, and 162 of device 156 can be made substantially coplanar with the transistors formed on substrate 100.

[0061] As an exemplary implementation of the method and the structure as described above with reference to FIG. 3, an exemplary structure having a ***p-i-n*** structure formed in an ART epitaxial crystalline structure is diagrammatically illustrated in FIG. 7. Referring to FIG. 7, STI trench 109 is formed in semiconductor substrate 100, which can be a silicon substrate or other semiconductor substrates. Multiple isolation patterns, such as dielectric pattern 154 are formed within the STI trench (109) using for example the method as described above with reference to FIG. 3, which will not be repeated herein. Openings 184, 186, and 188 are defined by the isolation patterns.

[0062] ART epitaxial crystalline growth can be performed in the openings 184, 186, and 188. By overgrowing or through the combination of overgrowing and coalescing of ELO portions of the ART structures in openings 184, 186, and 188, overgrown crystalline portion 196 is obtained. The overgrown crystalline portion 196 can have a large dimension, such as a lateral and/or vertical dimensions of 100 nanometers or larger, 500 nanometers or larger, 1 micron or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, and preferably, from 2 to 5 microns.

[0063] A ***p-i-n*** structure having ***p***-type region 192, intrinsic region 190, and ***n***-region 194 is formed in overgrown crystalline portion 196. The ***p***-type region 192 and the ***n***-type region 194 can

be obtained by doping. Because the overgrown crystalline portion 196 can have a large size, the intrinsic ***i*** region 190 can be large, such as 100 nanometers or larger, 500 nanometers or larger, 1 micron or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, and more preferably from 100 nanometers to 200 microns, and preferably, from 2 to 5 microns.

[0064] Other circuitry can be formed on the patterned semiconductor substrate 100, such as the transistor having source 164, gate 166, and drain 168. The source, gate, and drain of a transistor can be formed by a standard silicon process, such as a CMOS process. For example, the sources and drains of the transistors can be formed by doping; and the gates of the transistors can be formed by a standard silicon based lithography process. Other features can also be formed in the substrate (100). For example, isolation unit 176 can be formed between transistors so as to isolating the transistors. In one example, the semiconductor device (*e.g.* 196) formed on the ART structure can be substantially coplanar with one or more other semiconductor devices (*e.g.* transistors) on substrate 100. For example, the top surfaces of 192, 190, and 194 of device 196 can be made substantially coplanar with the transistors formed on substrate 100.

[0065] As can be seen in the examples as illustrated in FIG. 6 and FIG. 7, lateral ***p-i-n*** structures or ***p-n*** junctions can be made in ART epitaxial crystalline semiconductor structures, wherein the semiconductor structures can be comprised of non-silicon materials. For example, the carrier channel from the ***p*** region to the ***n*** region of a lateral ***p-i-n*** or ***p-n*** junction is parallel to the major surface of the substrate (100) or is substantially perpendicular to the direction along which the ART epitaxial crystalline materials are formed.

[0066] The method of making a semiconductor device can be of great importance in making photodetector pixels that are comprised of an array of ***p-i-n*** structures. For demonstration purposes, FIG. 8 through FIG. 14 diagrammatically demonstrate a portion of an array of photodetector pixels that are formed by exemplary methods as described above. In particular, non-semiconductor devices (*e.g.* non-silicon semiconductor sensor 214) can be integrated with silicon semiconductor devices (*e.g.* silicon transistors 208, 209, 202, and 204) using the method as discussed above. Referring to FIG. 8, four photodetector pixels of the photodetector array are shown

for simplicity purposes. In general, the photodetector array may comprise any desired number of photodetector pixels, which is referred to as the native resolution of the photodetector array. In one example, the photodetector array may have a native resolution of 640×480 (VGA) or higher, such as 800×600 (SVGA) or higher, 1024×768 (XGA) or higher, 1280×1024 (SXGA) or higher, 1280 × 720 or higher, 1400 × 1050 or higher, 1600 × 1200 (UXGA) or higher, and 1920 × 1080 or higher, or integer multiples and fractions of these resolutions. Of course, other resolutions are also applicable depending upon specific applications.

[0067] Each photodetector can have a characteristic size of less than 500 nanometers, 500 nanometers or larger, 1 micron or larger, such as 1.5 microns or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, or from 5 to 10 microns. The pitch, which is referred to as the distance between adjacent photodetectors in the array, can be any suitable values, such as 500 nanometers or larger, 1 micron or larger, such as 1.5 microns or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, or from 5 to 10 microns.

[0068] The portion of the exemplary photodetector array 200 comprises transistors 202, 204, 206, 208, 209, 210, 212, 218, 220, 224, 226, 230, and 232, and photo-sensors 214, 216, 222, and 228. The photo-sensors convert the light energy into voltage signals, and a group of transistors amplify the voltage signals (and convert the amplified voltage signals into digital signals if necessary). Another group of transistors can be provided for addressing and reading out the outputs of individual photodetector pixels in the columns and rows of the array by column and row addressing/reading signals.

[0069] For example, sensor 214 converts the received light intensity into a voltage signal. When an active signal (column signal) is delivered to transistor 209 through transistor 204 from a column decoder (which not shown in the figure), the output voltage signal from sensor 214 is amplified by transistor 208. When a row signal (row active signal) is delivered to the gate of transistor 209 through transistor 230, the amplified voltage signal V_{DD} is read out through the output of transistor 208. The output voltage signal V_{DD} can be digitized by other devices, such as an ADC unit, which is not shown in the figure.

[0070] The sensors (214, 216, 222, and 228) each can be a ***p-i-n*** structure as diagrammatically illustrated in FIG. 9. Referring to FIG. 9, sensor 214 comprises ***p*** region 234, ***i*** region 236, and ***n*** region 238. The ***p-i-n*** structure (214) can be formed in many ways, such as those described above with reference to FIG. 5, FIG. 6, and FIG. 7. Electron transportations properties of the ***p-i-n*** structure can be interpreted by energy band diagrams as diagrammatically illustrated in FIG. 9 and FIG. 10.

[0071] Referring to FIG. 9, the conductive and covalence bands of the ***p*** region 234, ***i*** region 236, and ***n*** region 238 are substantially flat in the absence of external voltages. Fermi energy E_f is close to the covalence band of the ***p*** region such that the ***p*** region is a hole-rich region. Because the ***i*** region is an intrinsic semiconductor region, the Fermi energy E_f is around the center of the gap between the covalence and conductive bands. Fermi energy E_f is close to the conductive band of the ***n*** region such that the ***n*** region is an electron-rich region.

[0072] In the presence of external voltage $V+$ and $V-$ respectively applied to the ***n*** and ***p*** regions, as diagrammatically illustrated in FIG. 10, the conductive and covalence bands of the ***p*** region is elevated; while the conductive and covalence bands of the ***n*** region is declined. As a consequence, the conductive and covalence bands of the intermediate ***i*** region inclines. The Fermi energy E_f also inclines the energy gap of the ***i*** region. The inclined Fermi energy drives electrons in the ***i*** region towards the ***n*** region; and holes in the ***i*** region toward the ***p*** region. This transportation of electrons and holes forms current in a carrier channel connecting the ***p*** and ***n*** regions.

[0073] The transistors and sensors of the photodetectors illustrated in FIG. 8 can be formed on ART epitaxial crystalline structures, which can be better illustrated in FIG. 11. For simplicity purposes, sensor 214 and the transistors around sensor 214 are shown in FIG. 11. The exemplary connection of sensor 214 to the transistors is also applicable to other sensors and transistors.

[0074] Referring to FIG. 11, sensor 214 has ***p***, ***i***, and ***n*** regions; and sensor 214 can be a non-silicon semiconductor device. The transistors 202, 204, 208, and 209 can be silicon based transistors. The ***p*** region is grounded and is connected to the drain of transistor 202. The source of transistor 202 is connected to reset signal ***p*** region V_{RST}. The ***p*** region of sensor 214 is

connected to the gate of transistor 208. The source of transistor 208 acts as an output for outputting amplified voltage signal V_{DD}. The drain of transistor 208 is connected to the source of transistor 209. The gate of transistor 209 is connected to the source of row selection transistor 230, whose gate is connected to the row signal from a row decoder. The drain of transistor 230 is connected to amplified voltage signal V_{DD}.

[0075] The drain of transistor 209 is connected to the source of column selection transistor 204, whose gate is connected to the column signal from a column decoder. The drain of row selection transistor 204 is connected to a sense signal.

[0076] The transistors in FIG. 11 can have any suitable configurations. In particular, the non-silicon semiconductor sensor (214) can be integrated with the silicon-based transistors (*e.g.* 202, 208, 209, 204, and 230). Alternatively, the transistors such as transistor 202 can be other types of transistors, such as germanium (or other silicon or non-silicon) based transistors as diagrammatically illustrated in FIG. 12. Referring to FIG. 12, a trench 235 or an opening is formed in a silicon substrate. The sidewalls of the trench are covered with a dielectric layer, such as an oxide layer 243. The sidewall cover layer (243) can be formed in many ways. For example, the sidewall cover layer (243) can be formed by depositing or growing the sidewall cover layer in the trench followed by removing the cover layer on the bottom surface of the trench. Alternatively, the trench can be filled with the sidewall cover layer followed by patterning/etching to form the desired sidewall cover layer in the trench. A germanium (or other silicon or non-silicon semiconductor materials) epitaxial crystalline structure 234 is formed in the trench of the silicon substrate using, for example, the method as discussed above with reference to FIG. 6. Source 236 and drain 238 of the transistor are formed in the germanium epitaxial crystalline structure (234) by doping. Gate 241 is formed on the germanium crystalline structure with an oxide layer laminated therebetween.

[0077] Another exemplary configuration of the transistors in FIG. 11 is diagrammatically illustrated in FIG. 13. Referring to FIG. 13, the transistor is formed on a silicon substrate. Dielectric patterns 242 are formed so as to define an opening on the silicon substrate. The

dielectric patterns can be formed by depositing a layer of a selected dielectric material, such as TiN_x on the silicon substrate followed by patterning the deposited dielectric layer.

[0078] The opening defined by the dielectric patterns has an appropriate aspect ratio, such as 0.5 or larger, 1 or larger, 1.5 or larger or 3 or larger, such that an ART growth process can be performed within the opening. Germanium epitaxial crystalline structure 148 can then be formed in the opening through an ART process. By doping portions of the germanium crystalline structure, source 236 and drain 238 can be obtained with an intrinsic region being laminated therebetween. Gate 241 can be formed above the germanium epitaxial crystalline structure with an oxide layer disposed therebetween.

[0079] In examples wherein the sensors of the photodetectors illustrated in FIG. 11 desired large areas, such as 1 micron or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, or from 5 to 10 microns, the ***p-i-n*** structure of the sensor can be formed using methods as described above with reference to FIG. 1, FIG. 2 or FIG. 7 or the like. For demonstration purposes, FIG. 14 diagrammatically illustrates an exemplary electrical connection of the ***p-i-n*** structure of the sensor to a transistor. This connection scheme is also applicable to connections of other sensors and transistors.

[0080] Referring to FIG. 14, an array of STI process trench structures (or other types of trench structures) 244, 246, 248, 250, and 252 are formed in a silicon substrate. The STI process trench structures can be formed by multiple patterning processes. For example, a patterning process can be performed so as to define the STI process opening from the top surface of the silicon substrate to the top surfaces of STI process patterns 214 and 254. Within the defined opening, another patterning process can be performed so as to define STI process patterns 244, 246, 248, 250, and 252 within the previously defined opening 214.

[0081] The adjacent STI patterns of the array of STI patterns 244, 246, 248, 250, and 252 define a series of openings, each of which has an aspect ratio commensurate with the aspect-ratio(s) desired for the following ART processes. With the series of openings between STI patterns 244, 246, 248, 250, and 252, an ART process is performed using a germanium (or other semiconductor

materials, such as InGaAs and III-V group materials) so as to form an ART epitaxial crystalline structure. As described above with reference to FIG. 1d or FIG. 7, a large ART portion can be formed above the openings and STI patterns by overgrowing the ART structures or by coalescing the ELO portions of the adjacent ART structures. Regardless of the growing process, the ART portion (264) can have the top surface that is substantially coplanar to the substrate (*e.g.* the silicon substrate) or can be above the top surface of the silicon substrate. Accordingly, the semiconductor device (or structure) formed on the ART structure (*e.g.* 264) can be substantially coplanar to another semiconductor device (*e.g.* the transistor having source 256, gate 258, and drain 260) formed at the top surface of the substrate. The ***p-i-n*** structures can then be formed in the large ART portion. Specifically, the ***p*** and ***n*** regions can be obtained by doping the intrinsic large ART portion with appropriate dopants. The intrinsic ***i*** region can have a large size, such as 1 micron or larger, 1.5 microns or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, or from 5 to 10 microns.

[0082] An insulation structure 254 can be formed by a STI process. Transistors having source 256, drain 260, and gate 258 can be formed on the silicon substrate by using a standard silicon process, such as a CMOS process. The ***p*** region of the ***p-i-n*** structure of the sensor (214) is grounded. The ***n*** region of the ***p-i-n*** structure is connected to the gate of transistor 208.

[0083] Other than forming a semiconductor device, such as a photodetector, a transistor, a LED or a laser, on a dislocation-free region in an epitaxial crystalline ART structure, the semiconductor device can alternatively be formed on a coalesced region between adjacent ART structures, an example of which is diagrammatically illustrated in FIG. 15. Referring to FIG. 15, substrate 269, which can be a semiconductor substrate, such as a silicon substrate is provided. Dielectric layer 270 is deposited on the substrate followed by patterning so as to generate openings in the dielectric layer. An ART process can be performed to form ART epitaxial crystalline structures 280 and 282. By overgrowing the ART structures, the ELO portions of the adjacent ART structures 280 and 282 can be coalesced to form a coalesced region 272. Semiconductor device 276, such as a ***p-i-n*** structure or ***p-n*** junction, a transistor, or other semiconductor devices can be formed at or in the

coalesced region (272). Element 276 can alternatively be a member of semiconductor device 274 that further comprises member 278, which can be formed at the non-coalesced ART region, such as the non-coalesced region of ART structure 280.

[0084] Alternative to forming semiconductor devices on coalesced region of adjacent ART structures that are formed in openings defined by dielectric patterns as described above with reference to FIG. 15, a semiconductor device can be formed at or in a coalesced region of adjacent ART structures that are formed in substrates, trenches, STI trenches or openings, an example of which is diagrammatically illustrated in FIG. 16.

[0085] Referring to FIG. 16, ART epitaxial crystalline structures 286 and 288 are formed from STI trenches in substrate 269, which can be a semiconductor substrate, such as a silicon substrate, wherein the sidewalls of the trenches are covered by dielectric layers 271 and 273, which may be comprised of an oxide material or other suitable materials. The dielectric layer can be formed in the same way as the dielectric layer 243 in FIG. 12. The ELO portions of ART structures 286 and 288 coalesce resulting in coalesced region 290. Semiconductor device 294, such as a ***p-i-n*** or ***p-n*** junction, a transistor, or other semiconductor devices can be formed at or in the coalesced region (290). Element 294 can alternatively be a member of semiconductor device 292 that further comprises member 296, which can be formed at the non-coalesced ART region, such as the non-coalesced region of ART structure 286.

[0086] In addition to the methods described above, integration of a non-silicon based semiconductor device into a silicon process can alternatively be achieved by using buffer layers. Graded buffer layers can be of great value for heteroepitaxy growth, such as heteroepitaxy growth on silicon. As a way of example, graded buffer layers can be used for heteroepitaxy (*e.g.* in silicon) in relatively larger areas as compared to the narrow trench areas (*e.g.* STI trench structures as in examples of ART). FIG. 17 diagrammatically illustrates an example. Referring to FIG. 17, in order to form a non-silicon based semiconductor device, such as a germanium (or other semiconductor materials, such as InGaAs and III-V group semiconductor materials) semiconductor device (*e.g.* a ***p-n*** or ***p-i-n*** structure) on a silicon substrate, a graded buffer layer comprised of a

selected semiconductor material is deposited on the silicon substrate. The graded buffer layer may have a size (*e.g.* the lateral or vertical dimension) such as 100 nanometers or larger, 500 nanometers or larger, 1 micron or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, or 100 microns or larger, 1 millimeter or larger, 200 millimeters or larger, 500 millimeters or larger, 1 centimeter or larger, or from 10 microns to several centimeters, such as from 10 microns to 500 microns, from 10 microns to 1 millimeter, from 10 microns to 500 millimeters or from 10 microns to 1 centimeter. The graded buffer layer may have other suitable lateral/vertical dimensions in other examples. In the particular example as illustrated in FIG. 17, dielectric patterns 302 of a selected dielectric material, such as TiN_x are formed on silicon substrate 304 and define an opening. In order to form a germanium ***p-n*** diode on the silicon substrate (304), graded buffer layer 298 for germanium is deposited in the opening on the silicon substrate (304). In other examples, the buffer can be comprised of other suitable materials, such as GaAs, a III-V group semiconductor material (*e.g.* SiGe, InGaAs, and InP), or a laminate of GaAs/InP/InGaAs. The graded buffer layer can be formed in may ways such as epitaxial techniques and other suitable techniques.

[0087] Germanium ***p-n*** diode 300 can then be formed on the graded buffer layer (298) for germanium. It is noted that depending upon different semiconductor devices to be formed on the silicon substrate (304), the graded buffer layer can be comprised of different materials to match the semiconductor device to be formed thereon.

[0088] The graded buffer layer can also be used for making semiconductor devices in trenches such as STI trenches formed in a semiconductor substrate, as diagrammatically illustrated in FIG. 18. Referring to FIG. 18, a STI trench is formed in silicon substrate 304. The sidewalls of the trench are covered by dielectric layer 299, which can be comprised of an oxide material or other suitable materials. The dielectric layer can be formed in the same way as the dielectric layer 243 in FIG. 12. A graded buffer layer 298 is disposed in the STI trench. Depending upon the semiconductor device to be formed on the buffer layer and the silicon substrate, the graded buffer layer can be comprised different materials. In the example as illustrated in FIG. 18 wherein a

germanium ***p-n*** diode is to be formed, the graded buffer layer is correspondingly comprised of a material for matching germanium. Germanium ***p-n*** diode 300 is formed on buffer layer 298.

[0089] A graded buffer layer may itself comprise a substantially defect (*e.g.* dislocation defect) free layer; and a device layer for forming a semiconductor device (*e.g.* a transistor, a photodetector, a solar cell, or other devices) can be formed on such defect free layer. The graded buffer layer may have a size (*e.g.* the lateral or vertical dimension) such as 100 nanometers or larger, 500 nanometers or larger, 1 micron or larger, 2 microns or larger, 5 microns or larger, 10 microns or larger, or 100 microns or larger, 1 millimeter or larger, 200 millimeters or larger, 500 millimeters or larger, 1 centimeter or larger, or from 10 microns to several centimeters, such as from 10 microns to 500 microns, from 10 microns to 1 millimeter, from 10 microns to 500 millimeters or from 10 microns to 1 centimeter. The graded buffer layer may have other suitable lateral/vertical dimensions in other examples. The graded buffer layer can be formed on a substrate (*e.g.* a silicon substrate), or in a region, such as a trench (*e.g.* a STI trench or other types trenches) that is formed in a substrate or in a dielectric or insulator layer above a substrate.

[0090] Referring to FIG. 19a, a cross-sectional view of a portion of an exemplary array of photodetectors is diagrammatically illustrated therein. A heavily doped ***p+*** region is formed in a silicon substrate. The ***p+*** region can then be used as a lower contact for the photodetectors. A dielectric layer, which is comprised of a low-temperature-oxide (LTO) material in this example, is deposited on the silicon substrate (*e.g.* on the ***p+*** region in the silicon substrate). The deposited LTO layer is patterned so as to form openings and expose the silicon substrate, especially, the ***p+*** region in the silicon substrate. ART epitaxial crystalline structures of a selected material, such as germanium or a III-V group semiconductor material are formed in the openings. The ART structures can be grown with in-situ doping until past the defect regions. The in-situ doped defect-regions can be formed as ***p***-type regions. The ART process can continue until the thickness (*e.g.* ***L***) is sufficient to allow for desirable levels of absorption of incident light that the photodetector is designed for detecting, such as visible light, ultraviolet light, and/or infrared light.

The top portion of the ART structures can then be doped with an appropriate material so as to form ***n***-type regions.

[0091] A top view of the photodetectors in FIG. 19a is diagrammatically illustrated in FIG. 19b. Referring to FIG. 19b, three photodetectors are shown for simplicity and demonstration purposes. As discussed above, the photodetector array may comprise any desired number of photodetectors.

[0092] The photodetectors in FIG. 19a and 19b are configured such that the ***p, i,*** and ***n*** regions of each photo sensor (*e.g.* the ***p-i-n*** structures) are vertically aligned along the growth direction of the ART structures. In photo detection application, light to be detected is directed toward the top of the sensors. In an alternative example, the light to be detected can be directed along the side of the sensors, as diagrammatically illustrated in FIG. 20a.

[0093] Referring to FIG. 20a, a heavily doped ***p+*** region is formed in an intrinsic silicon substrate. An ART epitaxial crystalline material comprised of germanium or a III-V semiconductor material is grown in openings of a dielectric layer, such as the dielectric layer comprised of a LTO material in FIG. 19a. With in-situ implantation, ***p*** region can be formed in the ART structures, especially the defect regions of the ART structures. The ART structures continue to form the intrinsic regions. By in-situ or other doping techniques, ***n***-regions can be formed in the top regions of the ART structures. A metal contact then can be formed on and physically contact to the ***n***-regions.

[0094] In light detection application, light to be detected is directed from the side of the photodetector as diagrammatically illustrated in FIG. 20a. This configuration allows for light detection to occur in-plane with the silicon substrate. Furthermore, it allows for the growth thickness of ART structures to be independent from the absorption depth.

[0095] A top view of the photodetectors is diagrammatically illustrated in FIG. 20b. Referring to FIG. 20b, germanium (or other semiconductor materials, such as a III-V semiconductor material) epitaxial crystalline ART structures are formed on a substrate (*e.g.* on the heavily doped ***p+*** region formed in the silicon substrate). The germanium ART structures in this example are deployed such that the lengths (in the top view) of the germanium ART structures are aligned to the <110>

direction of the silicon substrate, however the application is not intended to be so limited as other alignments are considered available. The incident light to be detected is directed toward the side of the germanium ART structures.

[0096] The electrical connection of the photodetectors as illustrated in FIG. 20a and FIG. 20b can have many suitable configurations, one of which is diagrammatically illustrated in FIG. 21a and FIG. 21b. Referring to FIG. 21a, the exemplary electrical connection scheme is illustrated in a top view. A contact to ***n*** region and a contact to ***p*** region are provided. Each contact comprise at least an elongated contact beam that spans across and electrically connected to substantially all regions of a particular type (*e.g.* the ***n*** or the ***p*** type) of the photodetectors. For example, metal contact 310 for contacting to ***n*** regions comprises contact beam 312. Contact beam 312 spans across substantially all ART structures; and is connected to the ***n*** regions of the ART structures. This connection is better illustrated in FIG. 21b that diagrammatically illustrates the connection of the metal contacts to the ***p*** and ***n*** regions of a ***p-i-n*** structure in a photodetector.

[0097] Metal contact 314 comprises at least one contact beam, such as contact beam 316. The contact beam spans across substantially all photodetectors; and is electrically connected to the ***p*** regions of the photodetectors. This connection is better illustrated in FIG. 21b.

[0098] In order to improve the quality and reliability of the electrical connection between the metal contacts to their designated regions, each contact may comprise multiple contact beams as diagrammatically illustrated in FIG. 21a. In the example as illustrated in FIG. 21a, the contact beams of each metal contact are uniformly deployed across the photodetectors within the light absorption range ***L***. Contact beams of different contacts can be alternately disposed. Other configurations are also applicable. For example, multiple (*e.g.* 2 or more) contact beams of one metal contact can be disposed between two adjacent contact beams of the other contact.

[0099] In another exemplary configuration, a contact beam of a metal contact can be connected to a group of photodetectors but not all photodetectors. The photodetectors not electrically connected to one contact beam can be electrically connected to another contact beam. In other words, a metal contact can have at least two contact beams that are electrically connected to two

different groups of photodetectors; whereas the two different groups have at least one different photodetector.

[00100] The method as described above can be applied to make semiconductor devices formed in or at ART structures, wherein the defect regions of the ART structures are not electrically isolated from rest of the semiconductor device. As a way of example, FIG. 22 diagrammatically illustrates a cross-sectional view of an exemplary photodetector having an ***n-p-n*** junction formed in an ART structure.

[00101] Referring to FIG. 22, a non-silicon ART material, which is a germanium (or III-V semiconductor material) in this example, is grown within an opening on a silicon substrate. The opening can be formed from patterning of a dielectric layer deposited on the silicon substrate or can be a STI trench formed in the silicon trench.

[00102] The germanium ART structure has a defect region, such as a region comprising dislocation defects, at the bottom. The ***n*** and ***p*** regions can be formed at the dislocation-defect-free top portion of the germanium ART structure. Specifically, an ***n-p-n*** junction can be formed near the top surface of the germanium ART structure. In this example, the bottom defect region in the germanium ART structure is not electrically isolated from the ***n-p-n*** junction or the germanium intrinsic region. Light to be detected is directed from the side of the photodetector.

[00103] It is noted that the semiconductor devices, such as the photodectors as discussed above with reference to FIG. 19a through FIG. 22 can be formed in trench structures, such as STI trenches or other types of trenches. The trenches can be formed in a substrate (*e.g.* with dielectric layers on the sidewalls of the trenches when necessary) or can be formed in a dielectric (or insulator) layer over the substrate.

[00104] As noted above, teachings of this disclosure have a wide variety of applications. While not limited to ART technology, teachings of this disclosure have many applications within ART technology. For example, examples of the methods disclosed in this disclosure may be used to create photodetectors (e.g., IR, UV) for semiconductor devices. Further, examples of the methods

disclosed in this disclosure may be used to create sensors using a ***p-n*** junction or a ***p-i-n*** structure in the sensing region (e.g., IR, UV) for semiconductor devices. A wide variety of devices may incorporate the invention. While not limiting to these devices, the invention may be particularly applicable to mixed signal applications, field effect transistors, quantum tunneling devices, light emitting diodes, laser diodes, resonant tunneling diodes and photovoltaic devices, especially those using ART technology. Application Serial No. 11/857047 filed 9/18/2007 entitled "Aspect Ratio Trapping for Mixed Signal Applications"; Application Serial No. 11/861931 filed 9/26/2007 entitled "Tri-Gate Field-Effect Transistors formed by Aspect Ratio Trapping"; Application Serial No. 11/862850 filed 9/27/2007 entitled "Quantum Tunneling Devices and Circuits with Lattice-mismatched Semiconductor Structures"; Application Serial No. 11/875381 filed 10/19/2007 entitled "Light-Emitter - Based Devices with Lattice-mismatched Semiconductor Structures"; and Application Serial No. 12/100131 filed 4/9/2007 entitled "Photovoltaics on Silicon" are all hereby incorporated by reference as providing examples to which aspects of this invention may be particularly suited.

[00105] A silicon CMOS device may be processed prior to embodiments of the invention, therefore, embodiment of devices such as LEDs or photovoltaic devices according to the invention integrated with CMOS process may be fabricated. Further, structures and/or methods according to disclosed embodiments can be used for integration of non-Si channel or active regions for next generation CMOS and for a wide variety of other applications.

[00106] Any reference in this specification to "one embodiment," "an embodiment," "example embodiment," "example," etc., means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of such phrases in various places in the specification are not necessarily all referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with any embodiment, it is submitted that it is within the purview of one skilled in the art to affect such feature, structure, or characteristic in connection with other ones of the embodiments. Furthermore, for ease of understanding, certain method procedures may have been

delineated as separate procedures; however, these separately delineated procedures should not be construed as necessarily order dependent in their performance. That is, some procedures may be able to be performed in an alternative ordering, simultaneously, etc. In addition, exemplary diagrams illustrate various methods in accordance with embodiments of the present disclosure. Such exemplary method embodiments are described herein using and can be applied to corresponding apparatus embodiments, however, the method embodiments are not intended to be limited thereby.

[00107] Although few embodiments of the present invention have been illustrated and described, it would be appreciated by those skilled in the art that changes may be made in these embodiments without departing from the principles and spirit of the invention. The foregoing embodiments are therefore to be considered in all respects illustrative rather than limiting on the invention described herein. Scope of the invention is thus indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein. As used in this disclosure, the term "preferably" is non-exclusive and means "preferably, but not limited to." Terms in the claims should be given their broadest interpretation consistent with the general inventive concept as set forth in this description. For example, the terms "coupled" and "connect" (and derivations thereof) are used to connote both direct and indirect connections/couplings. As another example, "having" and "including", derivatives thereof and similar transitional terms or phrases are used synonymously with "comprising" (i.e., all are considered "open ended" terms) – only the phrases "consisting of" and "consisting essentially of" should be considered as "close ended". Claims are not intended to be interpreted under 112 sixth paragraph unless the phrase "means for" and an associated function appear in a claim and the claim fails to recite sufficient structure to perform such function.

CLAIMS

We Claim:

1. A sensor, comprising:

a substrate configured with at least one depression in the substrate;

an insulator in the at least one depression in the substrate and configured to form at least two openings to the substrate, the insulator overlying sides of the at least one depression to form the at least two openings;

a first epitaxial crystalline structure in at least a portion of a first of the at least two openings;

a second epitaxial crystalline structure in at least a portion of a second of the at least two openings, the first and second epitaxial crystalline structures interfacing at a coalesced portion;

a sensing region formed at or in the coalesced portion to output electrons generated by light absorption therein; and

contacts coupled to receive the electrons to obtain an output electric signal.

2. The sensor of claim 1, wherein the first or the second epitaxial crystalline structure is substantially free from dislocation defects.

3. The sensor of claim 1, wherein the first or the second epitaxial crystalline structures is comprised of a semiconductor material.

4. The sensor of claim 1, wherein the at least two openings include trenches formed in a crystalline substrate.

5. The sensor of claim 1, wherein the sensing region comprises a ***p-n*** junction or a ***p-i-n*** structure.

6. The sensor of claim 1, wherein the sensor is a photodetector pixel of a semiconductor device; the photodetector pixel is a complementary-metal-oxide-semiconductor photodetector; and the photodetector

comprises a ***p-n*** junction or a ***p-i-n*** structure and a metal-oxide-semiconductor transistor, wherein the ***p-n*** junction or a ***p-i-n*** structure is formed in the sensing region, and wherein the photodetector is an IR or UV detector.

7. The sensor of claim 1, wherein the coalesced portion has a width of 1 micron or larger, the width of 2 microns or larger.

8. The sensor of claim 1, comprising:

a **p-i-n** structure formed within the substrate; and

an intrinsic region of the p-i-n structure is positioned to receive light in the sensing region.

9. The sensor of claim 1, wherein each of the first and second epitaxial crystalline structures are lattice mismatched to the substrate.

10. The sensor of claim 9, wherein an aspect ratio of at least one of the at least two opening is 0.5 or greater, wherein each of the openings is a trench, recess or hole.

11. The sensor of claim 9, wherein each of said first and second epitaxial crystalline structures comprise an epitaxial lateral overgrowth (ELO) region, wherein said ELO region is at least 2 times a width of the opening.

12. The sensor of claim 1, wherein the first and second epitaxial crystalline structures comprise semiconductor materials among a group II-VI compound, a group III-V compound, group III-N compound or ternary and quaternary compounds thereof or a group IV material.

13. A method, comprising:

providing a crystalline semiconductor substrate;

forming at least one depression in the substrate;

formingan insulator in the at least one depression in the substrate and configured to form at least two openings to the substrate, the insulator overlying sides of the at least one depression to form the at least two openings;

forming a first epitaxial crystalline structure in at least a portion of a first of the at least two openings;

forming a second epitaxial crystalline structure in at least a portion of a second of the at least two openings, the first and second epitaxial crystalline structures interfacing at a coalesced portion; and

making a photodetector formed at or in the coalesced portion to output electrons generated by light absorption therein.

14. The method of claim 13, wherein the substrate is a silicon substrate; and the first and second epitaxial crystalline structures are comprised of a non-silicon semiconductor material.

15. The method of claim 13, wherein the at least one depression has a width of 2 microns or larger.

16. The method of claim 13, wherein each of the first and second epitaxial crystalline structures are lattice-mismatched to the crystalline semiconductor substrate.

17. A semiconductor sensor, comprising:

a crystalline substrate having a recessed portion from a top surface of the crystalline substrate;

an insulator in the recessed portion of the crystalline substrate, the insulator having a plurality of openings to the crystalline substrate in the recessed portion;

a first crystalline material within the openings in the insulator, the first crystalline material being lattice-mismatched with the substrate;

a second different buffer crystalline material being lattice-mismatched with the crystalline substrate between the crystalline substrate and the first crystalline material;

a light-sensing device in a least a portion of the first crystalline material to output electrons generated by light absorption therein; and

contacts coupled to receive the electrons generated by light absorption to obtain an output electric signal.

18. The sensor of claim 17, wherein the second different buffer crystalline material has a thickness over the substrate less than 100nm.

19. The sensor of claim 17, wherein the first crystalline material comprises a group II-VI compound or ternary and quaternary compounds thereof, a group III-V compound or ternary and quaternary compounds thereof, group III-N compound or ternary and quaternary compounds thereof or a group IV material.