

The invention relates to a frequency-response-compensated circuit in control loops.

The d.c. voltage amplification of an operational amplifier wired in accordance with Figure 1 is $V_{out} = V_{in} * R_1 / R_0$. Internally such an integrated operational amplifier mainly consists of transistors and resistors. Capacitive couplings, so-called parasitic capacitances, exist between the connection lines and base, collector, emitter of the transistors and the substrate (= earth).

In the direction of higher frequencies, these parasitic capacitances result in increasing negative feedback, so that the amplification increasingly reduces compared to the d.c. voltage amplification. The phase response also changes with increasing frequency in a corresponding fashion. From a specified frequency onwards, e.g. 10 MHz, the phase shift is greater than 180° . However, since the amplification is still greater than 1, uncontrolled oscillations occur.

To prevent these oscillations, a capacitor is provided at a suitable location in the operational amplifier for the purpose of frequency response compensation. As a result, the phase shift remains at -90° within a specified frequency range, whereas the amplification reduces with a steeper gradient. When, at higher frequencies, the phase shift finally attains -180° , the amplification is already smaller than 1 and no more disturbing oscillations arise.

The greater the amplification, the more the frequency response must be compensated. In integrated circuits, however, a capacitor (for frequency response compensation) requires a relatively large chip surface area, for example $0.001 \text{ mm}^2/\text{pF}$. Thus a capacitor of 1000 pF would require a surface area of 1 mm^2 .

US-A-3,984,780 has described a control circuit which is frequency-response-compensated with a capacitor. In order to achieve a high degree of control accuracy, the internal amplification, and thus also the capacitor, must be of appropriate magnitude.

The aim of the invention is to generate accurate currents by means of a control circuit and to reduce the required capacitance of the frequency-response-compensation capacitor in the control circuit.

This aim is fulfilled by the features described in Claim 1. Advantageous further developments of the invention are described in the sub-claims.

In the following an exemplary embodiment of the invention will be explained making reference to the drawings wherein:

Figure 1 illustrates the wiring of an operational amplifier (known);

Figure 2 illustrates the wiring of an operational amplifier with reduced negative feedback (known);

Figure 3 illustrates a circuit for generating an accurate current with an operational amplifier in the control loop (known);

Figure 4 illustrates a circuit for the generation of an approximately accurate current (known);

Figure 5 illustrates a circuit in accordance with the invention for the generation of an accurate current;

Figure 6 illustrates a control circuit (known);

Figure 7 illustrates a control circuit in accordance with the invention;

Figure 8 is a circuit diagram of a temperature-compensated current supply.

Figure 1 illustrates the wiring of a negative feedback operational amplifier. The amplification is $V_{out} = V_{in} * R_1 / R_0$.

Figure 2 illustrates the wiring of a negative feedback operational amplifier with reduced negative feedback. C is in each case the capacitor for the frequency response compensation.

In Figure 3, R_{30} and R_{31} have the same resistance value. Because the connected, non-inverting input of the operational amplifier OP_{30} is comparatively highly ohmic, in each case half the supply voltage V_{CC} occurs across R_{30} and R_{31} . R_{32} is a reference resistor with a resistance value of for example 50 kOhm. The transistor T_{30} forms a current mirror. The connection point of R_{32} and the collector of the transistor T_{32} is connected to the inverting input of the operational amplifier OP_{30} . As a result, a reference current $I_{30} = (V_{CC} / 2) / R_{32}$ flows into the collector of T_{32} . The same current $I_{31} = I_{30}$ is formed across the collector of transistor T_{33} . As a result of the current mirror function of T_{30} and the resistor R_{35} , a current $I_{32} = (R_{35} / R_{32}) * (V_{CC} / 2) / R_{32}$ is formed through R_{35} . The capacitor C_{30} connected to the operational amplifier OP_{30} carries out the frequency response compensation of the control of the reference current I_{30} . C_{30} must possess a relatively high value and therefore requires a large chip surface area. The currents I_{30} , I_{31} , I_{32} are dependent upon the supply voltage V_{CC} . Because V_{CC} can be very accurate, the currents I_{30} to I_{32} are also correspondingly accurate.

Figure 4 illustrates a further circuit which is to generate accurate currents. R_{42} is a corresponding reference resistor and T_{40} is a current mirror. The current I_{43} is $I_{43} = (V_{CC} - 2 * V_{BE}) / R_{42}$. Because the base-emitter voltage V_{BE} is temperature-dependent, the current I_{40} is likewise temperature-dependent. In the range of $0 \dots 100^\circ\text{C}$ V_{BE} changes by approximately 200 mV. On the other hand, however, the circuitry outlay is distinctly lower compared to Figure 3. In particular, the relatively large chip surface area for the capacitor C_{30} is not now required.

Figure 5 illustrates a circuit which generates accurate currents, but in the case of which the chip surface area for a frequency-response-compensation capacitor is distinctly reduced. The circuit located on the left-hand side of A and B in Figure 3, comprising the resistors R_{30} and R_{31} , the operational amplifier OP_{30} and the capacitor C_{30} , is connected to the connection points A and B. R_{51} and R_{54} have the same value and are reference resistors. T_{50} is a current mirror. I_{53} is the reference current. Further, precisely identical reference currents, e.g. I_{59} , are formed across further transistors e.g. T_{59} , the base terminals of which are connected to the base of T_{53} . In Figure 5 the resistors R_{51} , R_{53} , R_{55} correspond to the resistors R_{42} , R_{43} , R_{44} in Figure 4, and the transistors T_{50} , T_{52} , T_{53} correspond to the transistors T_{40} , T_{42} , T_{43} in Figure 4. As a result, the reference current I_{53} is virtually pre-controlled in accordance with the reference current I_{43} . The fine control is carried out by the operational amplifier OP_{30} connected to the connection points A and B. OP_{30} is only required to adjust the temperature-dependent fluctuations caused by V_{BE} . Accordingly the control range of OP_{30} , and thus the negative feedback (as described for Figure 2), can be reduced. This

takes place in that the output of OP_{30} is connected to the emitter of T_{52} not directly but via the emitter follower T_{51} and a resistor R_{52} . The resistor R_{52} for example has the value $R_{52} = 10 * R_{53}$. Accordingly C_{30} can be reduced by the factor 10 and for example can have a value of 5 pF instead of 50 pF.

Three transistors and three resistors require, for example, a chip surface area which would correspond to the surface area for a 2 pF capacitor. It can be seen that as a result of the reduction from 50 pF to 5 pF, in spite of the increased number of components compared to Figure 3, a definite reduction is achieved in the chip surface area required for the overall control circuit, although the accuracy of the reference current I_{53} corresponds to that of I_{30} .

Figures 6 and 7 again illustrate the principle of the invention. Figure 6 shows a known control circuit. The desired value 69 is supplied to a subtraction point 60. The actual value 63 is subtracted from the desired value 69. The result is supplied via an error amplifier 61 to the control link 62 which supplies the actual value as output signal.

Figure 7 illustrates a control circuit in accordance with the invention. The desired value 79 is supplied to a subtraction point 70. The actual value 73 is subtracted from the desired value 79. The result is supplied via an error amplifier 71 and a multiplier 74 to an addition point 75. At the addition point 75 a presetting control value 76 is added, and the sum is supplied to the control stage 72 which again supplies the actual value as output signal. As a result of the addition of the presetting control value 76, the error amplification 71 can be reduced. This is effected by multiplication with a transfer value k , $k < 1$, e.g. $k = 0.1 \dots 0.5$, in the multiplier

74. As a result of the reduction in the error amplification, advantageously the frequency-response-compensation in the error amplifier 71 can be reduced by the factor $1 / k$.

The circuit according to Figure 8 supplies a current of in each case $80\mu\text{A}$ at the outputs $80_1\backslash\text{I}$, $80\text{U}_2\backslash\text{I}$ and $80\text{U}_3\backslash\text{I}$, supplies a current of $50\mu\text{A}$ at the output $50\text{U}\backslash\text{I}$ and a current of $30\mu\text{A}$ at the output $30\text{U}\backslash\text{I}$.

A reference resistor is connected between the terminals $\text{VCC}\backslash\text{I}$ and $\text{IREF}\backslash\text{I}$. If this resistor is not co-integrated, the temperature compensation for the V_{BE} -fluctuations must be somewhat intensified. The transfer value k then likewise becomes somewhat greater. Q_{12} corresponds to T_{51} , R_6 corresponds to R_{52} , R_8/R_9 correspond to R_{51} , Q_{16} corresponds to T_{50} , Q_{14} corresponds to T_{52} , R_7 corresponds to R_{53} , the reference resistor corresponds to R_{54} , Q_{18} corresponds to T_{53} , R_{12} corresponds to R_{55} , Q_{24} and R_{18} correspond to T_{59} and R_{56} . The base terminals of Q_4 and Q_7 correspond to the inputs of OP_{30} , the collector terminals of Q_{10} and Q_{11} correspond to the output of OP_{30} , and the capacitor C_1 corresponds to the capacitor C_{30} .

The terminal $\text{GND}\backslash\text{I}$ is the earth terminal. A reference voltage of 1.2 V is connected to the terminal $\text{VBG}\backslash\text{I}$, and the above mentioned outputs are connected to the terminal $\text{OFF}\backslash\text{I}$.

Q_{12} , Q_{14} , Q_{16} , R_6 , R_8 and R_9 are additionally provided in relation to a circuit corresponding to Figure 3. Overall, however, as a result of the reduction in C_1 a distinctly larger chip surface area is avoided, as described in the foregoing.

Claims



1. A frequency-response-compensated circuit with a desired value (79) which is supplied to the circuit and with an actual value (73) which is produced in the circuit, which circuit comprises a negative feedback amplification stage (71, OP30) with at least one capacitor (C_1 , C_{30}), where this amplification is smaller than one when the corresponding phase response attains 180° , and where a control value (IREF, base Q_7 ; 73-70) derived from the actual value is added to this amplification as a second negative feedback, characterised in that an unregulated control value (76, emitter current of Q_{14}) is added to the output signal (current through R_6) of the negative feedback amplification stage, where a reduced component (74; R_6 , R_7 ; R_{52} , R_{53}) of the output signal of the negative feedback amplification stage, combined with the unregulated control value, forms the actual value (73).
2. A frequency-response-compensated circuit as claimed in Claim 1, characterised in that the unregulated control value (76) is derived from at least one supply voltage (V_{CC} , $V_{CC(I)}$) of the circuit, from at least one reference resistance (R_{51} , R_{54} ; R_8 , R_9) and from at least one base-emitter voltage (V_{BE}).
3. A frequency-response-compensated circuit as claimed in Claim 1 or 2, characterised in that the negative feedback amplification stage (7) contains an operational amplifier for error signal amplification.
4. A frequency-response-compensated circuit as claimed in Claim 3, characterised in that the operational amplifier contains the capacitor (C_1) for changing the phase response.