METHODS OF FORMING A PLURALITY OF TRANSISTOR GATES, AND METHODS OF FORMING A PLURALITY OF TRANSISTOR GATES HAVING AT LEAST TWO DIFFERENT WORK FUNCTIONS

TECHNICAL FIELD

[0001] Embodiments disclosed herein pertain to methods of forming a plurality of transistor gates which may or may not have at least two different work functions.

BACKGROUND

[0002] Field-effect transistors are one type of electronic component used in the fabrication of integrated circuitry. Such include a pair of source/drain regions have a channel region received therebetween. A gate is received proximate the channel region and separated therefrom by a gate dielectric. By applying suitable voltage to the gate of the transistor, the channel region becomes electrically conductive. Accordingly, the transistor switches from a non-conductive state to a conductive state upon application of a suitable threshold voltage to the gate. It is desirable to keep threshold voltages of transistors small and also to keep power consumption of transistors low. One significant property of the gate which is determinative of threshold voltage is work function. It is the work function of the gate, together with the doping level of the channel region, which determines the threshold voltage of a field-effect transistor device. To keep threshold voltages of transistors small and power consumption low, it is desirable that the work function of the gate material be approximately equal to the work function of the material of the channel region.

[0003] Usually, not all transistors of an integrated circuit are of the same construction or materials. Accordingly, it is recognized and often desirable that different transistor gates be fabricated to have at least two different work functions. One manner of providing different work functions is to provide different gate electrodes to be formed of different materials. For example for

conductive polysilicon, using different conductivity-enhancing dopants and concentrations may provide different work functions for different transistors. For metal gates, use of different metals, or quantities of metals in metal alloys, are also known to impact work function in the finished device.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Fig. 1 is a diagrammatic sectional view of a substrate in process in accordance with an embodiment of the invention.

[0005] Fig. 2 is a view of the Fig. 1 substrate at a processing step subsequent to that shown by Fig. 1.

[0006] Fig. 3 is a view of the Fig. 2 substrate at a processing step subsequent to that shown by Fig. 2.

[0007] Fig. 4 is a view of the Fig. 3 substrate at a processing step subsequent to that shown by Fig. 3.

[0008] Fig. 5 is a view of the Fig. 3 substrate at an alternate processing step to that shown by Fig. 4.

[0009] Fig. 6 is a diagrammatic sectional view of another substrate in process in accordance with an embodiment of the invention.

[0010] Fig. 7 is a view of the Fig. 6 substrate at a processing step subsequent to that shown by Fig. 6.

[0011] Fig. 8 is a view of the Fig. 7 substrate at a processing step subsequent to that shown by Fig. 7.

[0012] Fig. 9 is a view of the Fig. 8 substrate at a processing step subsequent to that shown by Fig. 8.

[0013] Fig. 10 is a diagrammatic sectional view of another substrate in process in accordance with an embodiment of the invention.

[0014] Fig. 11 is a view of the Fig. 10 substrate at a processing step subsequent to that shown by Fig. 10.

[0015] Fig. 12 is a view of the Fig. 11 substrate at a processing step subsequent to that shown by Fig. 11.

[0016] Fig. 13 is a view of the Fig. 12 substrate at a processing step subsequent to that shown by Fig. 12.

[0017] Fig. 14 is a view of the Fig. 13 substrate at a processing step subsequent to that shown by Fig. 13.

[0018] Fig. 15 is a view of the Fig. 14 substrate at a processing step subsequent to that shown by Fig. 14.

[0019] Fig. 16 is a diagrammatic sectional view of another substrate in process in accordance with an embodiment of the invention.

[0020] Fig. 17 is a view of the Fig. 16 substrate at a processing step subsequent to that shown by Fig. 16.

[0021] Fig. 18 is a view of the Fig. 17 substrate at a processing step subsequent to that shown by Fig. 17.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0022] A first example method of forming a plurality of transistor gates having at least two different work functions is described with reference to Figs. 1-4. Referring to Fig. 1, a substrate, which may be a semiconductor substrate, is indicated generally with reference numeral 10. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Substrate 10 includes a semiconductive region 12 within which source/drain and channel regions (not shown) have or will be fabricated. An example material 12 is monocrystalline silicon suitably doped with one or more conductivity-enhancing impurities to one or more concentrations. Substrate 10 may include other layers or regions, for example trench isolation (not shown) which are not particularly material to the disclosure.

[0023] A gate dielectric 14 has been formed over substrate 12. An example thickness for gate dielectric 14 is from about 3 nanometers to about 10 nanometers, with about 5 nanometers being a specific example. A first transistor gate 16 and a second transistor gate 18 have been formed over substrate 12/14. First gate 16 has a first width 17 and second gate 18 has a second width 19, with first width 17 being narrower than second width 19. In the depicted embodiment, a plurality of first gates 16 and a plurality of second gates 18 have been formed over substrate 12/14, with first gates 16 having been formed within a first area 20 and second gates 18 having been formed within a different second area 22. Not all of the gates fabricated within first area 20 are necessarily of the same material, size, or shape, and not all of the transistor gates fabricated within second area 22 are necessarily of the same material, size, of shape. An example first width 17 is from about 20 nanometers to about 75 nanometers, with about 50 nanometers being a specific example. An example

width 19 is from about 40 nanometers to about 200 nanometers, with about 150 nanometers being a specific example.

[0024] In the context of this document, a "gate" or "transistor gate" alone refers to the conductive portion of a field-effect transistor gate construction, and a gate construction may include additional material, such as insulative sidewall spacers, an insulative cap, and/or a gate dielectric. The example gates 16, 18 are shown as not having insulative spacers or caps formed thereover or thereabout, and comprise a conductive region 24. However, insulative caps and/or spacers may be provided. Further, flash and other gate constructions might be used. Accordingly, conductive region 24 may comprise a control gate region or a floating gate region of a transistor. Conductive region 24 may be homogenous or non-homogenous. Example materials include conductively doped polysilicon, conductive metal compounds, and one or more elemental-form metals, including an alloy of multiple elemental-form metals. Example metals include platinum, cobalt, iridium, titanium, tungsten, tantalum, aluminum, iron, zirconium, vanadium, and hafnium.

[0025] Transistor gates 16 and 18 may be formed by any existing or yet-to-be developed manner. One technique includes photolithographic patterning and etch, with Fig. 1 depicting an etch of material 24 as having been conducted selectively relative to gate dielectric 14 such that it remains spanning between adjacent of the conductive gates over semiconductive material 12. Alternately, the processing might be conducted to not be selective, or etching continued to remove some or all of gate dielectric 14 from being received over substrate material 12 between the gates. Further, Fig. 1 depicts an example wherein the transistor gates are fabricated to be of equal thickness, although multiple thicknesses and/or configurations may also be used. An example thickness for conductive region 24 is from about 10 nanometers to about 100 nanometers, with about 75 nanometers being a specific example. Additionally, Fig. 1 depicts the transistor orientation being planar or horizontal. Alternate configurations, such as vertical transistors and/or transistors formed in trenches, are also contemplated, and whether existing or yet-to-be developed.

[0026] Referring to Fig. 2, a material 28 has been deposited over substrate 10, including over first and second gates 16, 18, respectively. Material 28 may be insulative, conductive (including conductively doped semiconductive materials), or semiconductive, including any combination of such. Examples include silicon dioxide, silicon nitride, polysilicon, carbon, titanium nitride, tantalum nitride and tungsten nitride. Material 28 may be deposited to a thickness which is less than, equal to, or greater than each of first and second gates 16, 18. Regardless, material 28 may be deposited substantially conformably or non-conformably over each of the first and second gates, and may be deposited to have a planar or non-planar outermost surface. Fig. 2 depicts an example wherein material 28 has been deposited in a substantially conformal manner to have a non-planar outermost surface 29, and to a thickness which is less than that of each of first and second gates 16, 18. In some embodiments, material 28 is of different composition from that of an outermost portion of conductive region 24 of transistor gates 16, 18.

[0027] Referring to Fig. 3, substrate 10 has been placed within an etch chamber, and material 28 has been etched from over both of first gates 16 and second gates 18. The etching of material 28 has been effective to expose conductive material of first gates 16 and to reduce thickness of material 28 received over second gates 18 yet to leave second gates 18 still covered by material 28. By way of example only, example suitable etching chambers include high temperature plasma etchers which are capable of achieving substrate temperatures of at least 300°C, for example the etching chamber of the DPSII G3 HT plasma etching reactor sold by Applied Materials, Inc. of Santa Clara, California and the etching chamber of the 2300 Kiyo plasma etching reactor sold by Lam Research Corporation of Fremont, California. Such ideally enable plasma etching which provide substrate temperature above 300°C, although other reactors might be used.

[0028] Such reactors may be operated in one embodiment to produce the example Fig. 3 depicted result wherein the etching action has completely cleared material 28 from being received over narrower width transistor gates 16 as compared to wider width transistor gates 18, with the etching action of Fig. 3

having been stopped at or shortly after exposure of narrower width transistor gates 16. Suitable conditions and etching chemistries will be selected by the artisan depending upon the transistor gate width and the composition and configuration of material 28 received over transistor gates 16, 18. The etching is ideally conducted as a plasma etch with fairly high bias and a partially physically driven etch so that facets effectively form proximate narrow width gates 16 to help expose such features more quickly than larger width gates 18. For example, where material 28 consists essentially of carbon, example conditions include substrate temperature from about 250°C to about 400°C, chamber pressure from about 20mTorr to about 100mTorr, inductive power from about 100W to about 500W, and bias power from about 200W to about 600W. Example etch gases include from 0sccm to about 500sccm of one or a combination of Ar, He, Ne, Kr, and Xe, plus from about 50sccm to about 200sccm of N_2, and from about 250sccm to about 100 sccm of O_2, with volumetric ratio of N_2 to O_2 ideally being at least 2:1. Alternate or overlapping conditions and chemistries can be determined by the artisan for materials other than carbon for material 28. The etching action may or may not clear material 28 from spanning between adjacent of the transistor gates, with Fig. 3 depicting an example wherein some thickness of material 28 remains spanning between adjacent transistor gates.

[0029] Referring to Fig. 4, and *in situ* within the etch chamber and after the etching of Fig. 3, substrate 10 has been subjected to a plasma comprising a metal at a substrate temperature of at least 300°C to diffuse said metal into first gates 16 to modify work function of first gates 16 as compared to work function of second gates 18. In the context of this document, *in situ* action requires the subjecting to be conducted in the very same chamber within which the etching occurred and without removing the substrate from the etch chamber between the etching and the subjecting to the plasma comprising the metal. The metal from the plasma may or may not be in a plasma state at the moment of starting the diffusion, and accordingly may alternately be in a gaseous state. Fig. 4 depicts the metal diffusion into conductive regions 24 by stippling in the drawing, with the dots indicating the diffused metal. Such diffusion may or may not distribute

the metal homogenously throughout conductive region 24, and regardless of whether conductive region 24 was homogenous before the exposure to the plasma containing the metal. Fig. 4 depicts an example wherein metal diffusion within conductive region 24 of first gates 26 is not homogenous throughout region 24. In such event, ideally diffusion of the metal from the plasma to within conductive region 24 is to within at least about 10 nanometers of the depicted upper surface of gate dielectric 14 to have a significant impact on work function of the gate. Further, the plasma to which the substrate is exposed may include one or more different metals such that one or more different metals might be diffused into conductive region 24 of first gates 16. Quantity of the metal diffused can be selected and determined by the artisan depending upon the impact desired on the work function of the gate. Further, such may be impacted based upon factors such as plasma composition, plasma conditions, time of exposure to the plasma, and composition of the conductive region into which the metal is diffusing.

[0030] Exposure to the plasma may or may not also diffuse the metal from the plasma into material 28 received over second gates 18, and regardless material 28 received over second gates 18 may or may not shield any of the metal from diffusing into second gates 18 during the exposure to plasma. Fig. 4 depicts an example wherein some diffusion of metal has also occurred into material 28, but not having been effective to diffuse any metal to within any of second gates 18. Fig. 5 depicts an alternate embodiment substrate 10a, like numerals from the first-described embodiment have been utilized where appropriate, with differences being indicated with the suffix "a". In the plasma exposure of Fig. 5, the diffusion of the metal has been effective to diffuse into and through material 28 into an outermost portion of conductive region 24 of second gates 18. Regardless, any such diffusion of metal to within second gates 18 is considerably less than that into first gate 16 such that work function of the first gates is modified as compared to any work function modification which may or may not occur to second gates 18.

[0031] Diffusion of example metals that will inherently increase work function include platinum, cobalt and iridium where, for example, conductive

region 24 of first gate 16 includes elemental-form metals or an alloy of elemental-form metals. Further, if conductive region 24 prior to the metal diffusion includes an alloy including one or a combination of platinum, cobalt and iridium, diffusion of more platinum, cobalt and iridium into such conductive regions will tend to increase work function. Correspondingly, examples of metals which reduce work function in metal conductive regions include titanium, tungsten, tantalum, aluminum and iron. Further, for example if the outermost portion of conductive region 24 comprises conductively doped polysilicon, diffusing of the metal may form the outermost portion of conductive region 24 to comprise a conductive metal silicide. In one ideal embodiment, the metal in the plasma is derived from an organometallic compound. Examples include tetracarbonyl nickel for nickel, ferrocene for iron, $Ti(N(CH_3)_2)_4$ and/or $Ti(N(C_2H_5)_2)_4$ for titanium, pentrkis-dimethyl amido-tantalum for tantalum, $Co_2(CO)_8$ for cobalt, and $Pt(C_2H_5C_5H_4)(CH_3)_3$ for platinum. Compounds other than organometallic might alternately be used, for example metal halides such as $TiCl_4$ and others. Example conditions in an inductively coupled high temperature etching reactor include substrate temperature from 300°C to about 400°C, chamber pressure from about 5mTorr to about 200mTorr, inductive/source power from about 100W to about 1,000W, and bias power from 0W to about 100W. Example flow rates for the metal-containing gas are from about 10sccm to about 200sccm, and from 0sccm to about 1,000sccm of a suitable inert carrier gas to perhaps improve plasma uniformity and density (i.e., Ar, He, Xe, Kr, Ne and/or N_2). Substrate temperature may be controlled by temperature of the susceptor or other support upon which the substrate rests. For example, the above described reactors may have their susceptors set to temperatures of 300°C or higher, with the substrate temperature during the exposure to plasma being from about 10°C to 50°C higher depending on conditions of the plasma.

[0032] The etching of Fig. 3 and the exposure to plasma of Figs. 4 or 5 may occur with or without any mask being received over any of material 28, with no mask being shown/received over any of material 28 in the depicted cross-section of Figs. 3-5.

[0033] Another example embodiment method of forming a plurality of transistor gates having at least two different work functions is described with reference to Figs. 6-10 with respect to a substrate 10b. Like numerals from the first-described embodiments have been utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Referring to Fig. 6, a plurality of transistor gates 32 comprising a conductive region 33 have been formed over a substrate 12/14. The transistor gates may or may not have at least two different widths, with gates 32 shown as having equal widths in Fig. 6. The transistor gates of Fig. 6 could have the example configurations of one or the other of gates 16, 18 in Fig. 1, or other configurations. Composition of conductive region 33, by way of example only, may be the same as that described above in connection with transistors 16, 18 of the first-described embodiment. Sidewall spacers and/or caps might be provided relative to transistor gates 32.

[0034] A material 34 has been provided over conductive region 33 of transistor gates 32, with such material being of different composition from that of an outermost portion of conductive region 33. Otherwise, example materials and attributes include any of those described above with respect to material 28 in the first-described embodiment.

[0035] Referring to Fig. 7, a mask 36 has been formed to cover some of transistor gates 32 and leave others of transistor gates 32 not covered by mask 36. Any suitable existing or yet-to-be developed mask might be utilized, and for example with such being either wholly or partly sacrificial. An example material includes photoresist with or without one or more anti-reflective coating layers.

[0036] Referring to Fig. 8, within a suitable etching chamber and after forming mask 36, material 34 has been etched from being received over those transistor gates 32 which are not covered by mask 36. Example chambers, chemistries and conditions include any of those described above in connection with the processing to produce the Fig. 3 substrate. Material 34 may or may not be etched to less than completely span between adjacent of the exposed transistor gates 32 which are not covered by mask 36. Fig. 8 shows some

material 34 spanning between adjacent of the exposed gates 32 after the etch. Alternately, all of material 34 not covered by mask 36 could be removed.

[0037] Referring to Fig. 9 and *in situ* within the etch chamber after the etching of Fig. 8, substrate 10b has been subjected to a plasma comprising a metal at a substrate temperature of at least 300°C. The exposure to plasma has been effective to diffuse the metal from the plasma into the conductive region of the transistor gates 32 which are not covered by mask 36 to modify work function of the uncovered transistor gates 32 as compared to work function of transistor gates 32 which are covered by mask 36. Ideally, mask 36 shields any of the metal from the plasma from diffusing into conductive region 33 of the covered/masked transistor gates 32. Example processing condition and chemistries are as described above in connection with the Figs. 4 and 5 embodiments. Accordingly, conductive region 33 may or may not be homogenous before and after the exposure to plasma, and the metal may diffuse uniformly or only partially into conductive region 33 to still have an impact upon and modify work function of transistor gates 32 which are not covered by mask 36.

[0038] Embodiments of methods of forming a plurality of transistor gates may or may not result in at least two different work functions for different gates. The example embodiments as described above resulted in at least two different work functions for different gates. One example of an embodiment not necessarily resulting in at least two different work functions is shown with respect to a substrate 10c in Figs. 10-15. Like numerals from the first-described embodiment have been utilized where appropriate, with differences being indicated with the suffix "c" or with different numerals. Referring to Fig. 10, a plurality of transistor gates 40 having conductive regions 42 has been formed over substrate 12/14. Example materials and constructions include any of those described above with respect to the Figs. 1-9 embodiments. A first material 44 has been deposited over substrate 12/14 including over and spanning between adjacent of transistor gates 40. First material 44 is of different composition from that of an outermost portion of conductive region 42 of transistor gates 40. Example materials and attributes include any of those described above with

respect to materials 28/34. Accordingly by way of example, first material 44 may or may not have a planar outermost surface, with a non-planar outermost surface being shown in Fig. 10.

[0039] Referring to Fig. 11, first material 44 has been etched to remove it from spanning between adjacent of transistor gates 40 yet leave first material 44 covering tops and sidewalls of transistor gates 40.

[0040] Referring to Fig. 12, a second material 46 has been deposited over the substrate including over and spanning between adjacent of transistor gates 40. Second material 46 may be the same or different in composition from that of an outermost portion of first material 44. Further, second material 46 may have a planar or non-planar outermost surface, with a planar outermost surface being shown in Fig. 12. Examples include any of those described above for material 28. Second material 46 may be deposited to a thickness which is less than, equal to, or greater than thickness of transistor gates 40.

[0041] Referring to Fig. 13, second material 46 has been etched from being received over at least some of transistor gates 40 but remain spanning between adjacent of transistor gates 40. Fig. 13 depicts an embodiment wherein second material 44 has been etched from being received over all of transistor gates 40. Such might be conducted with or without masking.

[0042] Referring to Fig. 14, within an etch chamber and after etching second material 46, first material 44 has been etched from being received over at least some of transistor gates 40, with Fig. 14 depicting an example wherein first material 44 has been etched from being received over all of transistor gates 40. Such etching may or may not be conducted selectively relative to second material 46 where such is of different composition from first material 44, with a selective etching having been conducted as shown in Fig. 14. Regardless, in one embodiment, etching of second material 46 as shown in Fig. 13 may be conducted within the same etch chamber as the etching depicted by Fig. 14. Further, in one embodiment, the etching of first material 44 from being received over at least some of transistor gates 40 as shown in Fig. 14 may occur *in situ* after the second material etch of Fig. 13. Example etching of first material 44 in

Fig. 14 may be conducted, for example, as described above in connection with any of the Figs. 3 and 8 embodiments.

[0043] Referring to Fig. 15, substrate 10c has been subjected to a plasma comprising a metal at a substrate temperature of at least 300°C to diffuse the metal from the plasma into conductive region 42 of transistor gates 40 to modify work function of transistor gates 40. Such subjecting/exposing has been conducted *in situ* within the etch chamber after the etching of first material 44 from being received over at least some of transistor gates 40 as was depicted in Fig. 14. Example processing may be as described above with respect to any of the Figs. 4, 5 and 9 embodiments. Where all transistor gates are exposed during the exposure to plasma as depicted by Figs. 14 and 15, work function of all transistor gates 40 will be modified. Figs. 16-18 depict an example alternate embodiment wherein at least two different work functions result, in part as a result of some of the second material remaining over some of the transistor gates during the exposure to plasma.

[0044] Specifically, Figs. 16-18 depict processing relative to an alternate embodiment substrate 10d. Like numerals from the above-described embodiments have been utilized where appropriate, with differences being indicated with the suffix "d" or with different numerals. Fig. 16 depicts processing of substrate 10d with respect to second material 46d subsequent to the Fig. 12 embodiment. In Fig. 16, second material 46d has been masked (no mask being shown) while some of second material 46d has been left outwardly exposed and etched from being received elevationally over only some of transistor gates 40 (specifically, the left three illustrated gates in Fig. 16).

[0045] Fig. 17 depicts subsequent processing whereby first material 44 has been etched from being received over the exposed, and thereby over only some of, transistor gates 40. Fig. 18 depicts subsequent processing wherein *in situ* within the etch chamber within which the Fig. 17 etching occurred, substrate 10d has been exposed to the above-described metal-containing plasma to diffuse the metal into conductive region 42 of the three left illustrated transistor gates 40.

[0046] In one embodiment, a method encompasses forming a plurality of transistor gates comprising a conductive region over a substrate. The transistor gates may or may not have at least two different widths. Any of the above-described and shown plurality of transistor gates of Figs. 1, 6 or 16 are examples of such transistor gates. A material is provided over the conductive region of the transistor gates, with such material being of different composition from that of an outermost portion of the conductive region of the transistor gates. Any one or a combination of material 28, 34, 44 and 46 are examples of such material. Further, for example, first material 44 and second material 46 in combination, regardless of whether first material 44 is removed to not span completely between transistor gates 40, is also such an example material. Accordingly, "material" as used here and elsewhere in this document does not require homogeneity and may include multiple different composition and/or density regions and/or layers.

[0047] Within an etch chamber, the material is blanketly etched from being received over the conductive region of the transistor gates. Example chambers, chemistries, and conditions are as described above with the etching of any of materials 28, 34, and 44. By way of example only, the processing in going from Fig. 13 to Fig. 14 may be considered as depicting such an embodiment whereby material 44 is shown as being as blanketly etched from being received over conductive region 42 of gates 40. Alternately by way of example only, the substrates of Figs. 2 and 6 might be blanketly etched to remove material 28 and 34, respectively, from being received over the conductive region of all of the depicted transistor gates

[0048] Then, *in situ* within the etch chamber after the blanket etching, the substrate is subjected to a plasma comprising a metal at a substrate temperature of at least 300°C to diffuse the metal from the plasma into the conductive region of the transistor gates to modify work function of the transistor gates. Example techniques, conditions, and chemistries for doing the same may be as those described above with respect to the processing of any of Figs. 4, 5, 9, 15 and 18.

Claims

1. A method of forming a plurality of transistor gates having at least two different work functions, comprising:

forming first and second transistor gates over a substrate, the first gate having a first width and the second gate having a second width, the first width being narrower than the second width;

depositing a material over the substrate including over the first and second gates;

within an etch chamber, etching the material from being over the first gate and to leave the material over the second gate; and

in situ within the etch chamber after the etching, subjecting the substrate to at least one of a gaseous or plasma metal at a substrate temperature of at least 300°C to diffuse said metal into the first gate to modify work function of the first gate as compared to work function of the second gate.

2. The method of claim 1 wherein the material received over the second gate shields any of said metal from diffusing into the second gate during the subjecting.

3. The method of claim 1 wherein the subjecting also diffuses said metal into the material received over the second gate.

4. The method of claim 3 wherein the material received over the second gate shields any of said metal from diffusing into the second gate during the subjecting.

5. The method of claim 3 wherein some of said metal also diffuses into the second gate.

6. The method of claim 1 wherein the metal is derived from an organometallic compound.

7. The method of claim 1 wherein the etching and subjecting occur without any mask being received over any of the material.

8 The method of claim 1 wherein the metal is derived from a metal halide.

9. The method of claim 1 wherein the first gate is homogenous before and after the subjecting.

10. The method of claim 1 wherein the first gate is not homogenous before the subjecting and is not homogenous after the subjecting.

11. The method of claim 1 wherein the metal does not diffuse to be homogenous within the first gate.

12. The method of claim 1 wherein the metal diffuses to be homogenous within the first gate.

13. The method of claim 1 wherein the metal comprises at least one of platinum, iridium, cobalt, titanium, tungsten, tantalum, aluminum, nickel and iron.

14. The method of claim 5 wherein the metal diffuses deeper into the first gate than into the second gate.

15. The method of claim 1 wherein the transistor gates comprise a conductive region, the respective conductive regions being homogenous before and after the subjecting.

16. The method of claim 1 wherein the transistor gates comprise a conductive region, the respective conductive regions not being homogenous before the subjecting and not being homogenous after the subjecting.

17. The method of claim 1 wherein the transistor gates comprise a conductive region, the metal not diffusing to be homogenous within the respective conductive regions.

18. The method of claim 1 wherein the transistor gates comprise a conductive region, the metal diffusing to be homogenous within the respective conductive regions.