WHAT IS CLAIMED IS:

1. A power adapter, comprising a communication interface through which the power adapter charges a battery in an electronic device and performs a data communication with the electronic device, wherein, the power adapter is configured to:

when a conventional charging or a quick charging is performed on the battery in the electronic device, determine whether an output current of the power adapter is greater than a current threshold and determine whether an output voltage of the power adapter is greater than a voltage threshold;

if the output current of the power adapter is greater than the current threshold and/or the output voltage of the power adapter is greater than the voltage threshold, turn off the direct current output of the power adapter; and

during the data communication between the main control circuit and the electronic device, if the electronic device determines that the output current of the power adapter is greater than the current threshold and/or the output voltage of the power adapter is greater than the voltage threshold, receive a charging stop instruction fed back by the electronic device, and turn off the direct current output of the power adapter according to the charging stop instruction.

2. The power adapter according to claim 1, wherein,

the power adapter comprises an EMI filtering circuit, a high-voltage rectifying and filtering circuit, an isolation transformer, an output filtering circuit, and a voltage tracking and controlling circuit;

the power adapter further comprises a power circuit, a main control circuit, a potential adjusting circuit, a current detection circuit, a voltage detection circuit and an output switch circuit;

an input end of the power circuit is connected with a secondary end of the isolation transformer; a power end of the main control circuit, a power end of the potential adjusting circuit and a power end of the current detection circuit are collectively connected with an output end of the power circuit; both a high-level end of the main

control circuit and a high-level end of the potential adjusting circuit are connected with a positive output end of the output filtering circuit; a potential adjusting end of the potential adjusting circuit is connected with the voltage tracking and controlling circuit; a direct current input end of the current detection circuit is connected with the positive output end of the output filtering circuit; a current feedback end of the current detection circuit is connected with a current detecting end of the main control circuit; a clock output end of the main control circuit is connected with a clock input end of the potential adjusting circuit; a data output end of the main control circuit is connected with a data input end of the potential adjusting circuit; a first detecting end and a second detecting end of the voltage detection circuit are connected with a direct current output end of the current detection circuit and a negative output end of the output filtering circuit respectively; a first output end and a second output end of the voltage detection circuit are connected with a first voltage detecting end and a second voltage detecting end of the main control circuit respectively; an input end of the output switch circuit is connected with the direct current output end of the current detection circuit; an output end of the output switch circuit is connected with a third detecting end of the voltage detection circuit; a ground end of the output switch circuit is connected with the negative output end of the output filtering circuit; a controlled end of the output switch circuit is connected with a switching control end of the main control circuit; a power end of the output switch circuit is connected with the secondary end of the isolation transformer; each of the negative output end of the output filtering circuit, the output end of the output switch circuit and a first communication end and a second communication end of the main control circuit is connected with the communication interface.

3. The power adapter according to claim 2, wherein the power circuit obtains power supply from the isolation transformer and provides the power supply for the main control circuit, the potential adjusting circuit and the current detection circuit; when a quick charging is performed on the battery in the electronic device, the potential adjusting circuit drives the voltage tracking and controlling circuit to adjust an output

voltage of the isolation transformer according to a control signal sent by the main control circuit; the current detection circuit detects an output current of the power adapter and feeds back a current detecting signal to the main control circuit, and the voltage detection circuit detects an output voltage of the power adapter and feeds back a voltage detecting signal to the main control circuit; the output switch circuit turns on or off a direct current output of the power adapter according to a switching control signal sent by the main control circuit.

4. The power adapter according to claim 2, wherein,

the power circuit comprises: a first capacitor, a voltage stabilizing chip, a second capacitor, a first inductor, a second inductor, a first diode, a second diode, a third capacitor, a first resistor and a second resistor;

a collective node of a first end of the first capacitor, an input power pin and an enable pin of the voltage stabilizing chip is configured as the input end of the power circuit, a second end of the first capacitor and a ground pin of the voltage stabilizing chip are collectively grounded, a switch pin of the voltage stabilizing chip and a first end of the second capacitor are collectively connected with a first end of the first inductor; an inside switch pin of the voltage stabilizing chip and a second end of the second capacitor are collectively connected with a cathode of the first diode; a feedback voltage pin of the voltage stabilizing chip is connected with a first end of the first resistor and a first end of the second resistor respectively; a second end of the first inductor and a cathode of the second diode are collectively connected with a first end of the second inductor; a collective node formed by collectively connecting a second end of the second inductor, an anode of the first diode, a second end of the first resistor and a first end of the third capacitor is configured as the output end of the power circuit, an anode of the second diode, a second end of the second resistor and a second end of the third capacitor are collectively grounded.

5. The power adapter according to claim 2, wherein,

the main control circuit comprises: a main control chip, a third resistor, a reference voltage chip, a fourth resistor, a fifth resistor, a fourth capacitor, a sixth resistor, a seventh resistor, a first NMOS transistor, an eighth resistor, a ninth resistor, a tenth resistor, an eleventh resistor, a twelfth resistor, a thirteenth resistor and a fourteenth resistor;

a power pin of the main control chip is configured as the power end of the main control circuit; a ground pin of the main control chip is grounded; a first input/output pin of the main control chip is suspended; a first end of the third resistor is connected with the power pin of the main control chip; a second end of the third resistor and a first end of the fourth resistor are collectively connected with a positive terminal of the reference voltage chip; a negative terminal of the reference voltage chip is grounded; a vacant pin of the reference voltage chip U3 is suspended; a second end of the fourth resistor is connected with a second input/output pin of the main control chip; a third input/output pin of the main control chip is configured as the current detecting end of the main control circuit; a fourth input/output pin of the main control chip is connected with a first end of the fifth resistor; a second end of the fifth resistor and a first end of the fourth capacitor are collectively connected with the power pin of the main control chip; a second end of the fourth capacitor is grounded; a fifth input/output pin of the main control chip is configured as the switching control end of the main control circuit; a sixth input/output pin of the main control chip is connected with a first end of the sixth resistor; a second end of the sixth resistor and a grid electrode of the first NMOS transistor are collectively connected with a first end of the seventh resistor; a second end of the seventh resistor and a source electrode of the first NMOS transistor are collectively grounded; a drain electrode of the first NMOS transistor is connected with a first end of the eighth resistor; a second end of the eighth resistor is configured as the high-level end of the main control circuit; a seventh input/output pin and an eighth input/output pin of the main control chip are configured as the clock output end and the data output end of the main control circuit respectively; a tenth input/output pin and a ninth input/output pin of the main control chip are configured as the first voltage detecting end and the second voltage detecting end of the main control circuit

respectively; an eleventh input/output pin and a twelfth input/output pin of the main control chip are connected with a first end of the ninth resistor and a first end of the tenth resistor respectively; a first end of the eleventh resistor and a first end of the twelfth resistor are connected with a second end of the ninth resistor and a second end of the tenth resistor respectively; a second end of the eleventh resistor and a second end of the twelfth resistor are collectively grounded; a first end of the thirteenth resistor and a first end of the fourteenth resistor are connected with the second end of the ninth resistor and the second end of the tenth resistor respectively; a second end of the thirteenth resistor and a second end of the fourteenth resistor are collectively connected with the power pin of the main control chip; the second end of the ninth resistor and the second end of the tenth resistor are configured as the first communication end and the second communication end of the main control circuit respectively.

6. The power adapter according to claim 2, wherein,

the potential adjusting circuit comprises: a fifteenth resistor, a sixteenth resistor, a digital potentiometer, a seventeenth resistor, an eighteenth resistor, a fifth capacitor, a sixth capacitor and a nineteenth resistor;

a collective node of a first end of the fifteenth resistor, a first end of the sixteenth resistor, a power pin of the digital potentiometer and a first end of the fifth capacitor is configured as the power end of the potential adjusting circuit; a second end of the fifth capacitor, a first end of the sixth capacitor, a ground pin of the digital potentiometer and a first end of the seventeenth resistor are collectively grounded; a second end of the sixth capacitor is connected with the power pin of the digital potentiometer; a collective node between a second end of the fifteenth resistor and a serial data pin of the digital potentiometer is configured as the data input end of the potential adjusting circuit; a collective node between a second end of the sixteenth resistor and a clock input pin of the digital potentiometer is configured as the clock input end of the potential adjusting circuit; an address zero pin of the digital potentiometer is grounded; a first potential wiring pin of the digital potentiometer and a first end of the eighteenth resistor are collectively connected with a second end of the seventeenth resistor; a second end of the

eighteenth resistor and a second potential wiring pin of the digital potentiometer are collectively connected with a first end of the nineteenth resistor; a second end of the nineteenth resistor is configured as the high-level end of potential adjusting circuit; a potential tap pin of the digital potentiometer is configured as the potential adjusting end of the potential adjusting circuit.

7. The power adapter according to claim 2, wherein,

the current detection circuit comprises: a twentieth resistor, a twenty-first resistor, a twenty-second resistor, a seventh capacitor, an eighth capacitor, a current detection chip, a twenty-third resistor, a ninth capacitor, a tenth capacitor and a twenty-fourth resistor;

a first end and a second end of the twentieth resistor are configured as the direct current input end and the direct current output end of the current detection circuit respectively; a first end of the twenty-first resistor and a first end of the twenty-second resistor are connected with a first end and a second end of the twentieth resistor respectively; a second end of the twenty-first resistor and a first end of the seventh capacitor are collectively connected with a positive input pin of the current detection chip; a second end of the twenty-second resistor and a first end of the eighth capacitor are collectively connected with a negative input pin of the current detection chip; a collective node between a power pin of the current detection chip and a first end of the ninth capacitor is configured as the power end of the current detection circuit; a vacant pin of the current detection chip is suspended; an output pin of the current detection chip is connected with a first end of the twenty-third resistor, a second end of the twenty-third resistor is configured as the current feedback end of the current detection circuit; a first end of the tenth capacitor and a first end of the twenty-fourth resistor are collectively connected with the second end of the twenty-third resistor; a second end of the seventh capacitor, a second end of the eighth capacitor, a second end of the ninth capacitor, a second end of the tenth capacitor, a second end of the twenty-fourth resistor, a ground pin, a first reference voltage pin and a second reference voltage pin of the current detection chip are collectively grounded.

8. The power adapter according to claim 2, wherein,

the voltage detection circuit comprises: a twenty-fifth resistor, a twenty-sixth resistor, an eleventh capacitor, a twelfth capacitor, a twenty-seventh resistor and a twenty-eighth resistor;

a first end of the twenty-fifth resistor is configured as the first detecting end of the voltage detection circuit; a collective node of a second end of the twenty-fifth resistor, a first end of the twenty-sixth resistor and a first end of the eleventh capacitor is configured as the second output end of the voltage detection circuit; a second end of the twenty-sixth resistor is configured as the second detecting end of the voltage detection circuit; a second end of the eleventh capacitor, a first end of the twelfth capacitor and a first end of the twenty-seventh resistor are collectively connected with the second end of the twenty-sixth resistor; a collective node of a second end of the twelfth capacitor, a second end of the twenty-seventh resistor and a first end of the twenty-eighth resistor is configured as the first output end of the voltage detection circuit; the second end of the twenty-eighth resistor is configured as the third detecting end of the voltage detection circuit.

9. The power adapter according to claim 2, wherein,

the output switch circuit comprises: a twenty-ninth resistor, a thirtieth resistor, a thirteen capacitor, a thirty-first resistor, a first NPN type transistor, a thirty-second resistor, a second NPN type transistor, a third diode, a voltage stabilizing diode, a thirty-third resistor, a thirty-fourth resistor, a thirty-fifth resistor, a second NMOS transistor and a third NMOS transistor;

a first end of the twenty-ninth resistor is configured as the controlled end of the output switch circuit; a second end of the twenty-ninth resistor and a first end of the thirtieth resistor are collectively connected with a base of the first NPN type transistor; a first end of the thirteen capacitor, a first end of the thirty-first resistor and a first end of the thirty-second resistor are collectively connected with a cathode of the third diode; an anode of the third diode is configured as the power end of the output switch circuit; a second end of the thirty-first resistor and a base of the second NPN type transistor are

collectively connected with a collector of the first NPN type transistor; a second end of the thirty-second resistor, a cathode of the voltage stabilizing diode and a first end of the thirty-third resistor are collectively connected with a collector of the second NPN type transistor; a second end of the thirtieth resistor, a second end of the thirteenth capacitor, an emitter of the first NPN type transistor, an emitter of the second NPN type transistor and an anode of the voltage stabilizing diode are collectively grounded; a second end of the thirty-third resistor, a first end of the thirty-fourth resistor, a first end of the thirty-fifth resistor, a grid electrode of the second NMOS transistor and a grid electrode of the third NMOS transistor are collectively connected; a second end of the thirty-fourth resistor is configured as the ground end of the output switch circuit; a drain electrode of the second NMOS transistor is configured as the input end of the output switch circuit; a source electrode of the second NMOS transistor and a second end of the thirty-fifth resistor are collectively connected with a source electrode of the third NMOS transistor; a drain electrode of the third NMOS transistor is configured as the output end of the output switch circuit.

10. The power adapter according to claim 2, wherein,

the EMI filtering circuit is configured to perform an electromagnetic interference filtering on electric supply;

the high-voltage rectifying and filtering circuit is configured to perform a rectifying and filtering process and to output a high-voltage direct current;

the isolation transformer is configured to output the high-voltage direct current to the output filtering circuit after an electrical isolation;

the output filtering circuit is configured to filter the high-voltage direct current for charging the battery; and

the voltage tracking and controlling circuit is configured to adjust an output voltage of the isolation transformer according to an output voltage of the output filtering circuit.

11. The power adapter according to claim 3, wherein,

the data communication between the main control circuit and the electronic device is performed during a charging; and the main control circuit sends the output current of the power adapter and the output voltage of the power adapter to the electronic device either in the conventional charging mode or in the quick charging mode.

12. The power adapter according to claim 4, wherein,

the power circuit outputs a voltage of +3.3V for providing power supply for the main control circuit, the potential adjusting circuit and the current detection circuit, after using the voltage stabilizing chip as a core to perform a voltage converting process on a voltage at the secondary end of the isolation transformer.

13. The power adapter according to claim 4, wherein,

the voltage stabilizing chip is a buck DC/DC converter.

14. The power adapter according to claim 5, wherein,

the main control chip is a single chip microcomputer.

15. The power adapter according to claim 6, wherein,

the digital potentiometer adjusts an internal sliding variable resistor according to a clock signal and a data signal outputted by the main control chip, such that a potential at the potential tap pin of the digital potentiometer is changed.

16. The power adapter according to claim 7, wherein,

the twentieth resistor is configured to sample an output current of the output filtering circuit, and the current detecting signal is outputted to the main control chip by the current detection chip according to a voltage between two ends of the twentieth resistor.

17. The power adapter according to claim 7, wherein,

the current detection chip is a current shunt monitor.

18. The power adapter according to claim 9, wherein,

the second NMOS transistor and the third NMOS transistor are switched on or off simultaneously so as to turn on or off the direct current output of the power adapter.

19. An electronic device, comprising a battery and further provided with a power adapter according to any one of claims 1-18.