

Description

The present invention concerns an RF signal switch for providing a high degree of isolation between sources in both the energized and de-energized condition.

5 It is common for several high frequency (RF) signal sources to be switched at the tuner inputs of an RF receiver such as a television receiver or the like. In such an arrangement it must be guaranteed, that there is sufficient de-coupling between the signal sources. In the United States, the FCC requires attenuation values of more than 80 db for frequencies up to 220 MHz. These values must also be observed in the shut-off condition. Often the RF signal sources are switched-over by the assistance of special relays. In order to make these
10 relays usable for radio frequency, they must be realized using a stripline technique. However, the stripline relay technique is very expensive, and the space required for such a relay and the measures concerning construction and circuitry are very great. Additionally, the life expectancy is limited due to the moving parts.

15 It is known by FR-A-2 612 023 a circuit for switching through several inputs to a common output by means of series and shunt diodes, which are alternately forward-biased or cut-off. But this configuration has not the effect, that there is a sufficient damping between the inputs in the case the device is switched off.

It is known by FR-A-1 519 740 that an attenuator for rf-signals uses varactor diodes in the series and shunt connections. However this configuration does not work in the sense of the present invention, because in case there is no connection to the mains for the device the series-connected varactor diodes have a great capacitance and do not have enough resistance to attenuate the signals.

20 The present invention as specified in the independent claim 1 is directed to a circuit arrangement overcoming such deficiencies.

Briefly, a circuit arrangement for switching-through (transit switching) of RF signals is provided. The signals from several RF signal sources are switched via controlled diode paths wherein the capacitance of varactor diodes in the unenergized state shunts the signals to ground thus achieving a high value of decoupling between
25 sources when the switch arrangement is not energized. Such an arrangement is particularly useful in antenna switches of television receivers and satellite installations.

Reference may be had to the drawings wherein:

Figure 1 shows an antenna switch;

Figure 2 shows the antenna switch according to the present invention.

30 The circuit arrangement comprises two branches 8 and 9 having respective input terminals IN1 and IN2, wherein signals present at the respective input terminals can be selectively switched-through via circuit S to the output terminal OUT. The decision as to which input terminal (IN1 or IN2) will be coupled to the output terminal (OUT) is provided by a logic circuit SL.

The logic circuit SL provides an L signal (low) and an H signal (high) which are arbitrarily assigned to a
35 respective one of the branches. In the exemplary embodiment, the L signal has been assigned to branch 8. The symbolically indicated contacts in the logic circuit SL are at the indicated potentials of plus and ground. For the signal at input terminal IN1 to be coupled to the output terminal OUT, the logic circuit SL would be switched into the L position as indicated by the arrow. In such a position, the positive potential is coupled to the upper branch 8 to the junction of resistor R1 and capacitor C1, and is coupled to the anode electrode of diode D1. Capacitor C1 is coupled to ground. Additionally, the positive potential is also coupled via resistor R3 to the
40 anode electrodes of diodes D2, D3 and D5. The cathode of diode D3 is coupled to the negative potential from circuit SL through resistor R4 and the cathodes of D2 and D4 are coupled to the negative potential through resistor R2. The cathode electrode of diode D3 is coupled to signal ground through resistor R4 and capacitor C2. The negative potential from circuit SL is provided through resistors R5 and R6 to the anode of diode D4 and cathode of diode D3. Thus, the longitudinal or series signal passing (or blocking) diodes D1, D2 and D3 are forward biased and input terminal IN1 is switched via said diodes and capacitors C3 and C11 to output
45 terminal OUT across resistor R16. Diodes D4 and D5 are coupled to signal ground via respective capacitors C4 and C5. The cathode of the diode D5 is supplied with a positive blocking potential via the resistor R8. During switch position L, the diodes D4 and D5 are reverse biased in a not conducting state and thus do not shunt the signal to ground. A corresponding analysis for switch position H applied to the lower branch 9 will show that the corresponding diodes are in an opposite bias state inasmuch as the corresponding diodes (D1 and D6, D4 and D5, D2 and D7, D5 and D10, and D3 and D8) are poled for opposite polarity. Thus, in switch position H of the logic circuit SL the diodes D6, D7 and D8 of the lower branch 9 are biased to block the passage of the signal from terminal IN2 to terminal OUT and the diodes D9 and D10 are biased to be conducting shunting the
50 signal to ground so that the signal at input terminal IN2 is both series blocked and shunted to ground and is de-coupled from the signal at input terminal IN1.

In the other switch position of the logic circuit SL (the H or high signal) the other input terminal IN2 is switched through to the output terminal OUT by branch 9 in a manner corresponding to the signal switched through

by branch 8 in the L position as discussed above. The ground potential reaches the cathode of diode D6 via the resistors R9 and R10 and signal coupling to ground via the capacitor C6. The cathodes of diodes D7, D8 and D10 coupled to ground potential via resistor R12. The anode of the diode D6 is coupled to positive potential via the resistor R11 so that diode D6 is conductively biased. The cathode of diode D9 and the anode of diode D10 are at AC ground potential via respective capacitors C7 and C8. The diode D7 is forward biased via the resistor R11 to the positive potential. The positive potential is also applied to diode D8 via the resistors R6 and R15, biasing the same conductively. The resistor R15 is coupled to AC ground via capacitor C9. In this case the input terminal IN2 is coupled to the output terminal OUT via the capacitors C10 and C12, and forward biased series signal passing (or blocking) diodes D6, D7 and D8. The diodes D9 and D10 are reverse biased and thus are switched "off" and do not shunt the signal to AC ground. As discussed above in connection with logic circuit SL in the L position, for the switch SL being in the H position, the corresponding diodes of the upper branch 8 are poled in opposite polarity and attenuate the signal at input terminal IN1.

The values of the resistors R2, R3 and corresponding resistors R11, R12 for respective diodes D2 and D7 are selected such that for each position of the logic circuitry SL the corresponding bias blocking voltage is produced via these diodes.

As stated above, it is desirable that isolation be maintained between input sources even when the television receiver or the like is unenergized. This embodiment, according to the present invention, is shown in Figure 2. In order to achieve the desired de-coupling in the case of a very low or no voltage provided to the circuit arrangement, the diodes D4, D5, D9 and D10 are provided as capacitive varactor diodes, which possess due to their capacity-characteristic in the current-less condition, a capacity of sufficient magnitude (e.g. 5 to 40 pF) to shunt the input signal to the required attenuation value. It should be noted that depending upon how much isolation is required, it may be sufficient for only one diode coupled to ground to be a capacitive varactor diode. In such a case, the other shunt diodes can be simple silicon switching diodes. In the exemplary embodiment, it is desirable that the series diodes have a sufficiently low internal resistance when forward biased (rs smaller than 1 Ohm) in order to minimize the insertion attenuation.

In Figure 2, the circuit is shown using varactor diodes for diodes D4, D5, D9 and D10. Varactor diodes D4, D5, D9 and D10 are switchable as are all of the other diodes according to the bias voltages applied to their respective electrodes and, when the receiver is energized, operate according to the description above in connection with Figure 1. However, when no energization voltage is provided, the varactor diodes possess a value of about 20pF - 40pF and the switching diodes D1, D2, D6 and D7, which are not forward biased, have a capacitive value of about 0,8pF, so that for source signals applied to terminals IN1 and IN2, a capacitive voltage divider results, e.g., a capacitive divider between diodes D1 and D4, D2 and D5, and correspondingly D6 and D9, D7 and D10. In such a case, there is a reciprocal ladder attenuation network between inputs IN1 and IN2 with the receiver dennergized.

The logic circuit SL in this embodiment is an inverter 10 wherein H and L signals, provided at input terminal 12, are inverted at output terminal 14. A combination of the signals taken from terminals 12 and 14 provides the logic states as symbolically shown in Figure 1 for logic circuit SL.

The following component parts have proved suitable for the circuit arrangement:

R1:	2,2 kOhm	C1:	4,7 nF
R2:	1,0 kOhm	C2:	4,7 nF
R3:	1,0 kOhm	C3:	1,0 nF
R4:	2,2 kOhm	C4:	120 pF
R5:	56 Ohm	C5:	120 pF
R6:	1,0 kOhm	C6:	4,7 nF
R7:	56 Ohm	C7:	120 pF
R8:	56 Ohm	C8:	120 pF
R9:	56 Ohm	C9:	4,7 nF
R10:	2,2 kOhm	C10:	1,0 nF
R11:	1,0 kOhm	C11:	33 pF
R12:	1,2 kOhm	C12:	33 pF
R13:	56 Ohm		
R14:	56 Ohm		
R15:	2,2 kOhm		
R16:	560 Ohm		

D1, D2, D3, D6, D7, D8: 1 SS 241 (SIEMENS)
 D4, D5, D9, D10 : BB 811 (TOSHIBA)

As used herein, receiver includes, for example, television receivers, VCR's and, satellite receivers.

Claims

1. A circuit arrangement having two input terminals (IN1, IN2) for the switching over of RF-signals to an output terminal (OUT) via a plurality of series-connected diodes (D1, D2, D3, D6, D7, D8) and at least one diode in each input circuit coupling at least one of the interconnecting nodes of the series-connected diodes to a reference potential, characterized in that from the first input terminal (IN1) a first, second and third diode (D1, D2, D3) are series-connected to the output (OUT), the cathodes of the first and second diode (D1, D2) are connected together and the anodes of the second and third diode (D2, D3) are connected together and that the cathodes of the first and second diode (D1, D2) are connected with the cathode of a first varactordiode (D4) the anode of which is coupled to the reference potential via a capacitor (C4) and that the anodes of the second and third diode (D2, D3) are connected with the anode of a second varactordiode (D5) the cathode of which is coupled to the reference potential via a capacitor (C5) and that from the second input (IN2) a fourth, fifth and sixth diode (D6, D7, D8) are series-connected to the output (OUT) the anodes of the fourth and fifth diode (D6, D7) are connected together and that the cathodes of the fifth and sixth diode (D7, D8) are connected together and that the anodes of fourth and fifth diode (D6, D7) are connected to the anode of a third varactordiode (D9) the cathode of which is coupled to the reference potential via a capacitor (C7) and that the cathodes of the fifth and sixth diode (D7, D8) are connected to the cathode of a fourth varactordiode (D10) the anode of which is coupled to the reference potential via a capacitor (C8).
2. The circuit arrangement according to claim 1 whereby isolation between the first input terminal (IN1) and the second input terminal (IN2) is provided when the circuit is de-energized.
3. The circuit arrangement according to claim 1 or 2 wherein said circuit is provided for a television set.



R1: 2,2 kOhm	C1: 4,7 nF
R2: 1,0 kOhm	C2: 4,7 nF
R3: 1,0 kOhm	C3: 1,0 nF
R4: 2,2 kOhm	C4: 120 pF
R5: 56 Ohm	C5: 120 pF
R6: 1,0 kOhm	C6: 4,7 nF
R7: 56 Ohm	C7: 120 pF
R8: 56 Ohm	C8: 120 pF
R9: 56 Ohm	C9: 4,7 nF
R10: 2,2 kOhm	C10: 1,0 nF
R11: 1,0 kOhm	C11: 33 pF
R12: 1,2 kOhm	C12: 33 pF
R13: 56 Ohm	
R14: 56 Ohm	
R15: 2,2 kOhm	
R16: 560 Ohm	

D1, D2, D3, D6, D7, D8: 1 SS 241 (SIEMENS)
 D4, D5, D9, D10 : EB 811 (TOSHIBA)

As used herein, receiver includes, for example, television receivers, VCR's and, satellite receivers.

Claims

1. A circuit arrangement having two input terminals (IN1, IN2) for the switching over of RF-signals to an output terminal (OUT) via a plurality of series-connected diodes (D1, D2, D3, D6, D7, D8) and at least one diode in each input circuit coupling at least one of the interconnecting nodes of the series-connected diodes to a reference potential, characterized in that from the first input terminal (IN1) a first, second and third diode (D1, D2, D3) are series-connected to the output (OUT), the cathodes of the first and second diode (D1, D2) are connected together and the anodes of the second and third diode (D2, D3) are connected together and that the cathodes of the first and second diode (D1, D2) are connected with the cathode of a first varactordiode (D4) the anode of which is coupled to the reference potential via a capacitor (C4) and that the anodes of the second and third diode (D2, D3) are connected with the anode of a second varactordiode (D5) the cathode of which is coupled to the reference potential via a capacitor (C5) and that from the second input (IN2) a fourth, fifth and sixth diode (D6, D7, D8) are series-connected to the output (OUT) the anodes of the fourth and fifth diode (D6, D7) are connected together and that the cathodes of the fifth and sixth diode (D7, D8) are connected together and that the anodes of fourth and fifth diode (D6, D7) are connected to the anode of a third varactordiode (D9) the cathode of which is coupled to the reference potential via a capacitor (C7) and that the cathodes of the fifth and sixth diode (D7, D8) are connected to the cathode of a fourth varactordiode (D10) the anode of which is coupled to the reference potential via a capacitor (C8).
2. The circuit arrangement according to claim 1 whereby isolation between the first input terminal (IN1) and the second input terminal (IN2) is provided when the circuit is de-energized.
3. The circuit arrangement according to claim 1 or 2 wherein said circuit is provided for a television set.



Patentansprüche

1. Schaltkreisanordnung mit zwei Eingangsanschlüssen (IN1, IN2) zum Schalten von Hochfrequenz-Signalen zu einem Ausgangsanschluß (OUT) über mehrere miteinander in Reihenschaltung verbundene Dioden (D1, D2, D3, D6, D7, D8) und mindestens eine Diode pro Eingangsschaltkreis, durch die mindestens einer der Verbindungspunkte der in Reihenschaltung verbundenen Dioden mit einem Bezugspotential gekoppelt wird, dadurch gekennzeichnet, daß vom ersten Eingangsanschluß (IN1) aus eine erste, zweite und dritte Diode (D1, D2, D3) per Reihenschaltung mit dem Ausgang (OUT) verbunden sind, daß die Kathoden der ersten und zweiten Diode (D1, D2) miteinander verbunden sind, daß die Anoden der zweiten und dritten Diode (D2, D3) miteinander verbunden sind, daß die Kathoden der ersten und zweiten Diode (D1, D2) mit der Kathode einer ersten Reaktanzdiode (D4) verbunden sind, deren Anode über einen Kondensator (C4) mit dem Bezugspotential gekoppelt ist, daß die Anoden der zweiten und dritten Diode (D2, D3) mit der Anode einer zweiten Reaktanzdiode (D5) verbunden sind, deren Kathode über einen Kondensator (C5) mit dem Bezugspotential gekoppelt ist, daß vom zweiten Eingang (IN2) aus eine vierte, fünfte und sechste Diode (D6, D7, D8) per Reihenschaltung mit dem Ausgang (OUT) verbunden sind, daß die Anoden der vierten und fünften Diode (D6, D7) miteinander verbunden sind, daß die Kathoden der fünften und sechsten Diode (D7, D8) miteinander verbunden sind, daß die Anoden der vierten und fünften Diode (D6, D7) mit der Anode einer dritten Reaktanzdiode (D9) verbunden sind, die über einen Kondensator (C7) mit dem Bezugspotential gekoppelt ist, und daß die Kathoden der fünften und sechsten Diode (D7, D8) mit der Kathode einer vierten Reaktanzdiode (D10) verbunden sind, deren Anode über einen Kondensator (C8) mit dem Bezugspotential gekoppelt ist.
2. Schaltkreisanordnung gemäß Anspruch 1, dadurch gekennzeichnet, daß die Isolierung zwischen dem ersten Eingangsanschluß (IN1) und dem zweiten Eingangsanschluß (IN2) gewährleistet ist, wenn der Schaltkreis nicht unter Spannung steht.
3. Schaltkreisanordnung gemäß Anspruch 1 oder 2, dadurch gekennzeichnet, daß der besagte Schaltkreis für ein Fernsehgerät bestimmt ist.

Revendications

1. Circuit à deux branches ayant deux bornes d'entrée (IN1 et IN2) permettant la commutation de signaux RF vers une borne de sortie (OUT) via plusieurs diodes reliées en série (D1, D2, D3, D6, D7, D8) et au moins une diode dans chaque branche d'entrée couplant au moins un des noeuds de connexion des diodes reliées en série à un potentiel de référence, caractérisé par le fait qu'à partir de la première borne d'entrée (IN1), une première, une deuxième et une troisième diode (D1, D2, D3) sont reliées en série à la sortie (OUT), et que les cathodes de la première et de la deuxième diode (D1, D2) sont reliées l'une à l'autre, que les anodes de la deuxième et de la troisième diode (D2, D3) sont reliées l'une à l'autre, et que les cathodes de la première et de la deuxième diode (D1, D2) sont reliées à la cathode d'une première diode varicap (D4), dont l'anode est couplée au potentiel de référence via un condensateur (C4), et que les anodes de la deuxième et de la troisième diode (D2, D3) sont reliées à l'anode d'une deuxième diode varicap (D5) dont la cathode est couplée au potentiel de référence via un condensateur (C5), et que, à partir de la deuxième entrée (IN2), une quatrième, une cinquième et une sixième diode (D6, D7, D8) sont reliées en série à la sortie (OUT), les anodes de la quatrième et de la cinquième diode (D6, D7) sont reliées l'une à l'autre et que les cathodes de la cinquième et de la sixième diode (D7, D8) sont reliées l'une à l'autre, et que les anodes de la quatrième et de la cinquième diode (D6, D7) sont reliées à l'anode d'une troisième diode varicap (D9) dont la cathode est couplée au potentiel de référence via un condensateur (C7) et que les cathodes de la cinquième et de la sixième diode (D7, D8) sont reliées à la cathode d'une quatrième diode varicap (D10) dont l'anode est couplée au potentiel de référence via un condensateur (C8).
2. Circuit selon la revendication 1, dans lequel l'isolation entre la première borne d'entrée (IN1) et la deuxième borne d'entrée (IN2) est assurée quand le circuit est hors tension.
3. Circuit selon la revendication 1 ou 2, utilisée dans un récepteur de télévision.