

ABSTRACT

An oscillation device and a display data processing device adjust variables such as the duty ratio of the oscillation frequency, and control autonomously timings between components such as memories. First and second switching devices disposed within charging and discharging devices are turned on and off by an output of a MOS buffer, enabling adjustment of the frequency and duty ratio of an oscillation signal. Equivalent circuits are provided corresponding to display data RAM, CGROM, and address decoders, data is read sequentially from the display data RAM and the CGROM when an EIRAM signal is enabled, and a DLAT signal is stored in a driver circuit. The equivalent circuits enable each of EIROM, EILAT, and RS signals at points when the read data is confirmed or thereafter. When the RS signal is enabled, EIRAM and other signals are sequentially disabled and the display data RAM and other components switch to a precharge operation.

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