WHAT IS CLAIMED IS:

1. A signal masking circuit, comprising:

a receiving circuit, configured to receive a signal to be processed and a chip select (CS) signal, and output an initial processing signal and an initial CS signal;

a delay control circuit, configured to perform delay and logical control operations on the initial CS signal to obtain a CS masking signal, wherein a pulse width of the CS masking signal is greater than or equal to two preset clock periods; and

a logical operation circuit, configured to perform invalid masking on the initial processing signal according to the CS masking signal to obtain a target signal.

2. The signal masking circuit according to claim 1, wherein the CS signal is a signal indicating whether a chip is selected and is an active-low pulse signal, and a pulse width of the CS signal is one preset clock period.

3. The signal masking circuit according to claim 2, wherein

the logical operation circuit is configured to mask, when the initial processing signal is a signal corresponding to a target chip, an invalid signal in the initial processing signal according to the CS masking signal, and/or mask, when the initial processing signal is a signal corresponding to a non-target chip, the initial processing signal completely according to the CS masking signal,

wherein the target chip is a chip selected by the CS signal, and the non-target chip is a chip that is not selected by the CS signal.

4. The signal masking circuit according to claim 3, wherein the signal to be processed comprises at least one of a command/address (CA) signal or a clock signal, wherein a period of the clock signal is equal to the preset clock period.

5. The signal masking circuit according to claim 4, wherein when the signal to be processed is

the CA signal, the receiving circuit comprises a first receiving module and a second receiving module, and the logical operation circuit comprises a first logical operation circuit, wherein

the first receiving module is configured to receive the CA signal and output an initial CA signal;

the second receiving module is configured to receive the CS signal and output the initial CS signal;

the delay control circuit is connected to an output terminal of the second receiving module, and is configured to perform the delay and logical control operations on the initial CS signal to obtain the CS masking signal; and

the first logical operation circuit is connected to an output terminal of the delay control circuit and an output terminal of the first receiving module, and is configured to perform a logical operation on the CS masking signal and the initial CA signal to obtain a target CA signal.

6. The signal masking circuit according to claim 4, wherein when the signal to be processed is the clock signal, the receiving circuit comprises a third receiving module and a fourth receiving module, and the logical operation circuit comprises a second logical operation circuit, wherein

the third receiving module is configured to receive the clock signal and output an initial clock signal;

the fourth receiving module is configured to receive the CS signal and output the initial CS signal;

the delay control circuit is connected to an output terminal of the fourth receiving module, and is configured to perform the delay and logical control operations on the initial CS signal to obtain the CS masking signal; and

the second logical operation circuit is connected to an output terminal of the delay control circuit and an output terminal of the third receiving module, and is configured to perform a logical operation on the CS masking signal and the initial clock signal to obtain a target clock signal.

7. The signal masking circuit according to claim 4, wherein when the signal to be processed is

the CA signal and the clock signal, the receiving circuit comprises a first receiving module, a second receiving module, and a third receiving module, and the logical operation circuit comprises a first logical operation circuit and a second logical operation circuit, wherein

the first receiving module is configured to receive the CA signal and output an initial CA signal;

the second receiving module is configured to receive the CS signal and output the initial CS signal;

the third receiving module is configured to receive the clock signal and output an initial clock signal;

the delay control circuit is connected to an output terminal of the second receiving module, and is configured to perform the delay and logical control operations on the initial CS signal to obtain the CS masking signal;

the first logical operation circuit is connected to an output terminal of the delay control circuit and an output terminal of the first receiving module, and is configured to perform invalid masking on the initial CA signal according to the CS masking signal to obtain a target CA signal; and

the second logical operation circuit is connected to an output terminal of the delay control circuit and an output terminal of the third receiving module, and is configured to perform a logical operation on the CS masking signal and the initial clock signal to obtain a target clock signal.

8. The signal masking circuit according to claim 5 or 7, wherein the first logical operation circuit comprises a first buffer, a first AND gate, and a second buffer, wherein

the first buffer is connected to the first receiving module, and is configured to perform driving enhancement and delay processing on the initial CA signal to obtain a first CA signal;

the first AND gate is connected to an output terminal of the first buffer and the output terminal of the delay control circuit, and is configured to perform an AND operation on the CS masking signal and the first CA signal to obtain a second CA signal; and

the second buffer is connected to an output terminal of the first AND gate, and is

configured to perform driving enhancement and delay processing on the second CA signal to obtain the target CA signal.

9. The signal masking circuit according to claim 6 or 7, wherein the second logical operation circuit comprises a third buffer, a second AND gate, and a fourth buffer, wherein

the third buffer is connected to the third receiving module, and is configured to perform driving enhancement and delay processing on the initial clock signal to obtain a first clock signal;

the second AND gate is connected to an output terminal of the third buffer and the output terminal of the delay control circuit, and is configured to perform an AND operation on the CS masking signal and the first clock signal to obtain a second clock signal; and

the fourth buffer is connected to an output terminal of the second AND gate, and is configured to perform driving enhancement and delay processing on the second clock signal to obtain the target clock signal.

10. The signal masking circuit according to any one of claims 1 to 9, wherein the delay control circuit comprises a delay module, a pulse width adjustment module, a first inverter, and a first OR gate, wherein

the first inverter is configured to invert the initial CS signal to obtain a first intermediate signal;

the delay module is configured to delay the initial CS signal to obtain a second intermediate signal;

the pulse width adjustment module is configured to perform pulse width extension on the second intermediate signal to obtain a third intermediate signal; and

the first OR gate is connected to an output terminal of the first inverter and an output terminal of the pulse width adjustment module, and is configured to perform an OR operation on the first intermediate signal and the third intermediate signal to obtain the CS masking signal.

11. The signal masking circuit according to claim 10, wherein the delay module comprises a

first delay unit, a second delay unit, and a second inverter, and the second inverter is located between the first delay unit and the second delay unit, wherein

the first delay unit is configured to perform a first delay processing on the initial CS signal to obtain a first delay signal;

the second inverter is configured to invert the first delay signal to obtain an inverted delay signal; and

the second delay unit is configured to perform a second delay processing on the inverted delay signal to obtain the second intermediate signal.

12. The signal masking circuit according to claim 11, wherein each of the first delay unit and the second delay unit is formed by a resistor R and a capacitor C.

13. The signal masking circuit according to claim 10, wherein the pulse width adjustment module comprises a fifth buffer and a second OR gate, wherein

the fifth buffer is connected to an output terminal of the delay module, and is configured to perform driving enhancement and delay processing on the second intermediate signal to obtain a fourth intermediate signal; and

the second OR gate is connected to the output terminal of the delay module and an output terminal of the fifth buffer, and is configured to perform an OR operation on the second intermediate signal and the fourth intermediate signal to obtain the third intermediate signal.

14. The signal masking circuit according to claim 7, further comprising: a buffer module formed by a plurality of sixth buffers, wherein

the buffer module is configured to perform driving enhancement and delay processing on the initial CS signal according to the plurality of sixth buffers to obtain a target CS signal.

15. The signal masking circuit according to claim 14, further comprising:

a sampling circuit, configured to receive the target CA signal, the target clock signal, and the target CS signal, and sample the target CA signal and the target CS signal by using the

target clock signal to obtain a sampled CA signal and a sampled CS signal; and

a decoding circuit, connected to an output terminal of the sampling circuit and configured to decode the sampled CS signal and the sampled CA signal to obtain a target command result.

16. The signal masking circuit according to claim 15, wherein the sampling circuit is formed by a plurality of D flip-flops (DFFs).

17. The signal masking circuit according to claim 8, 9, 13 or 14, wherein the buffer is formed by two inverters.

18. The signal masking circuit according to claim 8, wherein a rising edge time of the CS masking signal is earlier than a pulse start time of the first CA signal, a falling edge time of the CS masking signal is later than a pulse end time of the first CA signal, and the CS masking signal and the first CA signal correspond to a same valid pulse of the CS signal.

19. A semiconductor memory, comprising the signal masking circuit according to any one of claims 1 to 18.

20. The semiconductor memory according to claim 19, wherein the semiconductor memory is a Dynamic Random Access Memory (DRAM) chip.

~~21. The semiconductor memory according to claim 20, wherein the DRAM chip meets a 5th Double Data Rate (DDR5) memory specification.~~