CLAIMS

1. A semiconductor structure, comprising:

a pad structure disposed above a substrate; and

a capacitor structure disposed between the substrate and the pad structure, and arranged opposite to the pad structure, the capacitor structure comprising at least two capacitor units that are connected in parallel and spaced apart from each other, wherein each of the capacitor units comprises at least one capacitor device;

wherein the capacitor device comprises a first polar plate and a second polar plate that are arranged oppositely, the semiconductor structure further comprises a conductive layer, the conductive layer comprises a first conductive portion and a second conductive portion that are mutually insulated, the first conductive portion is electrically connected to the first polar plate of each of the capacitor devices; the second conductive portion is electrically connected to the second polar plate of each of the capacitor devices; and one of the first conductive portion and the second conductive portion is also electrically connected to a power end, and the other of the first conductive portion and the second conductive portion is also electrically connected to a grounding end;

wherein the second conductive portion is in an integrated structure and spans each of the capacitor devices in the capacitor structure, the first conductive portion is in a separated structure and comprises a plurality of sub-conductive portions that are electrically connected to each other, the sub-conductive portion spans adjacent capacitor devices in the capacitor structure, and orthographic projections of each of the sub-conductive portions on the substrate are spaced apart from an orthographic projection of the second conductive portion on the substrate.

2. The semiconductor structure according to claim 1, wherein an orthographic projection of the capacitor structure on the substrate is within an orthographic projection of the pad structure on the substrate.

3. The semiconductor structure according to claim 2, wherein a center of the orthographic projection of the capacitor structure on the substrate is coincided with a center of the orthographic projection of the pad structure on the substrate.

4. The semiconductor structure according to claim 1, wherein each of the capacitor units comprises at least two capacitor devices that are connected in parallel; the capacitor devices in the capacitor structure is arranged in M-row N-column array, wherein both M and N are integers greater than or equal to 2;
the sub-conductive portion comprises a first sub-portion, and the same sub-portion spans four capacitor devices that are adjacent in pairs and distributed symmetrically around a center.

5. The semiconductor structure according to claim 1, wherein the pad structure comprises a first metal layer, one end of the first metal layer is electrically connected to the power end or the grounding end, and the other end of the first metal layer is electrically connected to each of the sub-conductive portions via a first through hole.

6. The semiconductor structure according to claim 5, wherein the pad structure further comprises a second metal layer, a third metal layer, and a fourth metal layer, the third metal layer is connected to the second metal layer via a third through hole; and the fourth metal layer is connected to the third metal layer via a fourth through hole.

7. The semiconductor structure according to claim 6, wherein an orthographic projection of the second metal layer on the substrate is ring-shaped, and the orthographic projection of the second metal layer on the substrate surrounds an orthographic projection of the capacitor structure on

the substrate.

8. The semiconductor structure according to claim 7, wherein an orthographic projection of the third metal layer on the substrate is coincided with the orthographic projection of the second metal layer on the substrate.

9. The semiconductor structure according to any one of claims 6 to 8, wherein the pad structure is a power pad or a grounding pad, and the second metal layer is electrically connected to the first metal layer via a second through hole.

10. The semiconductor structure according to any one of claims 1 to 8, wherein the power end and/or the grounding end is located in an external circuit outside the pad structure.

11. The semiconductor structure according to claim 1, wherein the capacitor device comprises a transistor-type capacitor, a gate of the transistor-type capacitor forms the first polar plate of the capacitor device, and a source and a drain of the transistor-type capacitor and the substrate form the second polar plate of the capacitor device.

12. The semiconductor structure according to claim 11, wherein the first conductive portion is electrically connected to the power end, and the second conductive portion is electrically connected to the grounding end;
the semiconductor structure further comprises a protection ring, both ends of the protection ring are connected to the substrate and the second conductive portion, respectively, and an orthographic projection of the protection ring on the substrate surrounds an orthographic

projection of the capacitor structure on the substrate.

13. The semiconductor structure according to claim 11, wherein the capacitor unit comprises at least two transistor-type capacitors, and adjacent two transistor-type capacitors in the same capacitor unit share the source or the drain.