

A HIERARCHICAL BUS SIMPLE COMA ARCHITECTURE FOR SHARED MEMORY MULTIPROCESSORS

ABSTRACT

A method of maintaining cache coherency in a shared memory multiprocessor system having a plurality of nodes (H1, H2), where each node (H1, H2) itself is a shared memory multiprocessor. With this invention, an additional shared owner state (9B) is maintained so that if a cache (2) at the highest level of cache memory in the system issues a read or write request to a cache line that misses the highest cache level (2) of the system, then the owner of the cache line places the cache line on the bus (4) interconnecting the highest level of cache memories.

Fig 3