This Sheet Has Been Replaced



ABSTRACT

This invention relates to a method and device for detecting a cyclic code, and more specifically to means suitable for establishing cell synchronization in the ATM communication system.

The method subtracts the remainder of division by a generating polynomial added at the transmitting side before performing division on a serially input continuous bit sequence by the generating polynominal in advance to detect an n-bit cyclic code or shortened cyclic code contained in said bit sequence.

The device for detecting a cyclic code comprises a divider (1) which has exclusive OR circuits (12) put between the 1st and 2nd stages, the 5th and 6th stages, and the 6th and 7th stages, a shift register (10) the output of the last stage of which is input to the added exclusive OR circuits (12), and a decoder (11) which detects when the contents of individual registers of the divider (1) are all zero or form a predetermined bit pattern.

This device can detect the position of the boundary of a cyclic code or shortened cyclic code by means of a simple circuitry without need of high-speed circuits, and hence is suitable especially for the cell synchronization in the high-speed ATM communication system.