

SPECIFICATION

High voltage CMOS monolithic integrated circuit

5 This invention relates to a high voltage CMOS integrated circuit which has general application to complementary metal oxide semiconductor (CMOS) circuits and more particularly, to a CMOS circuit requiring high voltage capability.

10 A typical CMOS circuit will have an output voltage capability of approximately 30 volts, however, many CMOS circuits have been known to break down at approximately 18 volts. Occasionally the situation arises where it would be desirable to operate CMOS

15 circuits at voltages higher than the typical breakdown voltages. One application where such high voltage CMOS circuits would be desirable is for driving a multiplex vacuum fluorescent display. Generally speaking, the breakdown voltage of a

20 CMOS circuit is a function of the resistivity of its P tub and also a function of the depth of the N type drain portion of the CMOS circuit. Accordingly, when it is desired to increase the breakdown voltage of the circuit the obvious approach is to vary the resistivity of the P tub or change the depth of the N type drain

25 portion or to take both corrective steps. One of the disadvantages with most known ways of increasing the breakdown voltage of a CMOS circuit is that they involve process changes.

30 Accordingly, it is an object of the present invention to provide a CMOS circuit having high voltage capability which does not require changes to the process.

Another object of the present invention is to

35 increase the breakdown voltage of a CMOS circuit by adding an additional series N channel transistor and connecting the P tubs in a unique manner.

According to one aspect of the invention there is provided a high voltage CMOS monolithic integrated

40 circuit comprising a first MOS transistor of a first channel conductivity type having an electrode coupled to a first voltage terminal; first and second MOS transistors of a second channel conductivity type, all of said transistors being coupled in series, said first

45 and second transistors of second channel conductivity type having first and second electrodes and the gate electrodes thereof coupled together to form an inverter circuit, characterised in that said first and second transistors of second channel conductivity

50 each have a separate tub, the tub of the first transistor of second channel conductivity type being connected to both the second electrode thereof and to the first electrode of the second transistor of second channel conductivity type, and the tub of the

55 second transistor of second channel conductivity type being connected to both the second electrode thereof and a second voltage terminal.

According to a further aspect of the invention there is provided a CMOS integrated circuit having

60 high voltage capability, comprising a P channel field effect transistor having a first electrode, a second electrode and a gate electrode, the first electrode capable of being coupled to a first voltage potential; a first N channel field effect transistor having a first

65 and a second electrode and a gate electrode, the first

electrode of the first N channel transistor being coupled to the second electrode of the P channel transistor and forming an output junction for the circuit; a second N channel field effect transistor

70 having a first and a second electrode and a gate electrode, the first electrode of the second N channel transistor being coupled to the second electrode of the first N channel transistor, the second electrode of the second N channel being capable of being

75 coupled to a second voltage potential, and the gate electrodes of the P channel and first and second N channel transistors all being coupled together; and a level shift means for providing a voltage level shift to an input voltage, the level shift means providing an

80 output coupled to the gate electrodes of the P channel and first and second N channel transistors, the first and second N channel field effect transistors each having a tub being connected to the second electrode of each respective transistor.

85 The CMOS circuit of the invention has at least one P channel transistor coupled between a first voltage node and an output of the circuit. At least two N channel transistors are coupled in series between the output and a second voltage node. The at least two N channel transistors each have separate tubs which are connected to their respective sources to provide at least one tub which is isolated from the voltage nodes when the output is at a potential substantially equal to a voltage present at the first

90 voltage node.

The invention will now be described by way of example only with particular reference to the accompanying drawings wherein:

Figure 1 illustrates an embodiment of the invention in one form thereof;

Figure 2 illustrates in schematic form a voltage level shifter using the invention;

Figure 3 illustrates a schematic of another level shifter also using the invention in one form;

105 Figure 4 illustrates in schematic form a logic gate using the invention;

Figure 5 illustrates in schematic form another logic gate using the invention; and

110 Figure 6 is a pictorial representation of a cross-section of a piece of silicon to illustrate the connection to the P tubs.

In Figure 1, a low voltage input is connected to line 10. What is meant by a low voltage is an input signal normally having a voltage level between V_{DD} and V_{SS} . Line 10 is connected to the gate of an N channel transistor 11 and to the gate of an N channel transistor 12. The source of P channel transistor 11 is connected to terminal 13 which is the V_{DD} voltage terminal or node of the circuit. The source of electrode of N channel resistor 12 is connected to voltage reference 14, V_{SS} . Transistors 11 and 12 form a typical CMOS inverter and provide an output at node 16 which is the inverted input appearing at line 10. The output appearing at node 16 will be a low voltage output. In a typical CMOS circuit, V_{DD} is eighteen volts or less while V_{SS} is ground reference or 0 volts. The output at node 16 will be some voltage level between the values V_{DD} and V_{SS} . The input appearing at line 10 will also be within the

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130 same voltage range.

Output node 16 is connected to level shift circuit 17. Level shift 17 is connected to V_{DD} terminal 13 and to V_{EE} terminal 18. Level shift 17 takes the low voltage from output node 16 and converts it to a 5 level between V_{DD} and V_{EE} . The output level shift 17 appears on line 19 which is connected to the gate electrode of P channel transistor 21 and to the gate electrodes of N channel transistors 22 and 23. P channel transistor 21 is connected between V_{DD} 10 terminal 13 and output line 26. N channel transistors 22 and 23 are connected in series between output line 26 and V_{EE} terminal 18. Transistors 21, 22, and 23 form a high voltage inverter, and transistor 21 serves as a load means for the high voltage inverter. In a 15 CMOS circuit the load means could be an element other than a P channel transistor, e.g. a P-resistor, polysilicon resistor, etc. The output inverter formed by transistors 21, 22, and 23, in accordance with the present invention, performs functionally the same as 20 the prior art inverter formed by transistors 11 and 12. Voltage V_{EE} is usually a negative voltage with respect to voltage V_{DD} and can be any level so long as the potential between V_{DD} and V_{EE} does not exceed thirty-five volts. If higher voltage operation is 25 desired then additional N channel transistors will have to be placed in series with transistors 22 and 23. The series arrangement of transistors 22 and 23 will provide typical breakdown voltage of approximately sixty volts with a minimum breakdown of 30 approximately thirty-five volts. Typical gate rupture voltage for CMOS transistors is approximately eighty volts, and thus does not present a problem for the voltage ranges used as examples herein. The gate rupture voltage can be increased by increasing the 35 gate oxide thickness.

N channel transistors 22 and 23 each have separate P tubs 24 and 25 and each tub 24, 25 is connected to the source of its associated transistor. When the voltage on line 19 exceeds the threshold of 40 transistor 21 then transistor 21 is enabled and N channel transistors 22 and 23 will be disabled or nonconducting and the voltage, V_{OUT} , appearing on the output line 26 will be substantially the voltage V_{DD} . In such a situation, note that the tub of 45 transistor 22 is essentially isolated from the voltage terminals 13 and 18 and increases the breakdown voltage between output line 26 and voltage node 18. When N channel transistors 22 and 23 are nonconducting, and transistor 21 is conducting, the greatest 50 voltage potential will exist between output 26 and V_{EE} terminal 18, assuming that the voltage at V_{EE} is much greater in absolute magnitude than the voltage at V_{DD} . N channel transistor 22, with floating tub 24, increases the breakdown voltage of composite 55 transistors 22 and 23. The drain-to-tub breakdown voltage of a typical P channel transistor is approximately 150 volts already and therefore P channel transistor 21 does not suffer from the low breakdown voltage as do the N channel transistors. 60 However, it should be noted that due to different processes, or even variations within the same process, that the drain to source spacing of the P channel transistor may have to be increased slightly to raise its punch through voltage so that punch 65 through does not occur in the P channel transistor in

a high voltage CMOS circuit.

Figure 2 illustrates a level shift circuit 31 of the type that could be used for level shift circuit 17 of Figure 1. In Figure 2 the low voltage input appears at 70 input terminal 27 which is connected to the gate electrode of P channel transistor 31. P channel transistor 32 is connected between voltage terminal V_{DD} and output line 36. A P-resistor 28 is in series with N channel transistors 29 and 30 which cooperate to provide a bias voltage for N channel transistors 33 and 34. The gate of transistor 29 is connected 75 to the drain of transistor 29 to perform a function similar to a diode. N channel transistors 29 and 30 each have individual tubs and form a composite transistor arrangement for handling high voltages. 80 The gate electrodes of transistors 29 and 30 are connected together.

N channel transistors 33 and 34 are in series between output 36 and voltage terminal V_{EE} . These 85 N channel transistors also have separate tubs which are connected to the sources of their respective transistors to provide a composite high voltage handling capability. The gate electrodes of transistors 33 and 34 are connected to the gate electrodes 90 of transistors 29 and 30. Transistors 29 and 30, in conjunction with resistor 28, form a bias voltage for transistors 33 and 34. Transistors 33 and 34 act like a current sink. The P-resistor 28 sets the current 95 through composite N channel transistors 29 and 30. The gate-drain voltage of these transistors stabilizes to a voltage set by the current. When transistors 29 and 30 are conducting, the majority of the voltage drop between terminals V_{DD} and V_{EE} will appear across resistor 28. If the current tends to decrease 100 then more voltage will be applied to the gate electrodes of transistors 29 and 30 and these transistors will start to conduct more which in turn increases the voltage drop across resistor 28 thereby stabilizing the bias circuit. The voltage appearing at 105 the gate electrodes of transistors 29 and 30 is also applied to the gates of transistors 33 and 34 to form a current mirror thereby establishing the amount of current the current sink (transistors 33 and 34) can handle. It will be understood that the single bias 110 voltage source illustrated could power other output current sinks simply by connecting the gate electrodes of transistors 29 and 30 to duplicate circuits such as formed by transistors 32, 33 and 34. P channel transistor 32 is large enough to not only pull 115 up the output node to voltage V_{DD} when input 27 enables transistor 32 but also supplies enough current for the current sink formed by transistors 33 and 34. In summary, level shift circuit 31 is capable of taking a low voltage input applied to input 27 and 120 providing a high voltage output on line 36. A high voltage output as used herein, means an output signal having an amplitude between V_{DD} and V_{EE} .

Figure 3 shows another level shift circuit capable of shifting a low voltage at its input to a high voltage 125 at its output. Level shift circuit 40 receives an input at input terminal 41 and a complement of the input on input terminal 51. Input 41 is connected to the gate electrode of a P channel transistor 42 which has its source connected to terminal V_{DD} and its drain 130 connected to the drain of an N channel transistor 43.

N channel 43 is connected to N channel 44 to form a composite N channel high voltage transistor. The gate electrodes of transistors 43 and 44 are connected to output terminal 49. The source of N channel transistor 44 is connected to voltage terminal V_{EE} . N channel transistors 47 and 48 form the composite high voltage transistors coupled between output 49 and voltage terminal V_{EE} . The gate electrodes of N channel transistors 47 and 48 are connected to the drain of P channel transistor 42. The input complement connected to input terminal 51 is connected to the gate electrode of P channel transistor 46 which is connected between voltage terminal V_{DD} and output terminal 49. When an input on input terminal 41 enables transistor 42, transistor 46 is disabled since the complement of the enabling signal is applied to its gate electrode by input terminal 51. With transistor 42 enabled, voltage V_{DD} is applied to the gates of transistors 47 and 48 which enable these transistors thereby applying voltage V_{EE} to output 49. The voltage V_{EE} at output 49 is coupled to the gate electrodes of transistors 43 and 44 which hold these transistors in a nonconducting state. When the input to terminal 41 is switched, then of course transistor 42 ceases to conduct and transistor 46 commences conducting and causes the output at terminal 49 to approach voltage V_{DD} . The four N channel transistors 43, 44, 47 and 48 all have separate P tubs which are connected to their respective sources.

Figure 4 illustrates a logic NOR gate 60 embodying the present invention. Two series connected P channel transistors 61 and 62 are between voltage terminal V_{DD} and node 67. Two N channel composite transistors 65 and 66 are coupled between node 67 and voltage terminal V_{EE} . The gate electrodes of transistors 65 and 66 are connected to the gate electrode of transistor 61 which is also connected to input A. A second pair of composite N channel transistors 63 and 64 are in parallel with transistors 65 and 66. N channel transistors 63 and 64 have their gate electrodes connected to the gate electrode of transistor 62 which is also connected to input B. Output node 67 is connected to output $A + B$. It will be noted that logic gate 60 is similar to a typical prior art CMOS logic gate with the addition of composite N channel transistors to increase the breakdown voltage of the CMOS logic gate. Each of the CMOS transistors has an independent tub which is connected to the respective source of the transistor.

Figure 4 illustrates the use of the present invention in a typical 2-input CMOS logic NOR gate and it will be understood that if a logic gate with more inputs is desired, then additional composite N channel transistors can be added to provide the necessary high voltage capability.

Figure 5 is an example of the present invention being used in a 2-part CMOS NAND gate 70. NAND gate 70 has input A and B and output $A \cdot B$. Two P channel transistors 71 and 72 are in parallel between voltage terminal V_{DD} and output $A \cdot B$. Four N channel transistors 73, 74, 75 and 76 are connected in series between output $A \cdot B$ and voltage terminal V_{EE} . The gate electrodes of transistors 73 and 75 are connected to input A and to the gate electrode of

transistor 71. The gate electrodes of transistors 74 and 76 are connected to input B and to the gate electrode of transistor 72. This is a standard CMOS NAND gate configuration with the addition of the present invention, and it will be understood that if more inputs are required, the high voltage handling capability would be implemented in the same manner as illustrated.

Each of the N channel transistors 73 through 76 can have its own individual P tub, however, transistors 73 and 74 can be in the same P tub and transistors 75 and 76 can be in a separate P tub. The important point is that one tub be isolated from V_{EE} and the output of the circuit. In the case where each of transistors 73 through 76 are in separate tubs, the tub of transistor 74 is connected to its source; the tub of transistors 75 and 76 are connected together and then to the source of transistor 76. The important point is that the arrangement provide at least one tub which is isolated from voltage terminals V_{DD} or V_{EE} when either P channel transistor 71 or 72 is conducting.

A pictorial representation of a cross-sectional view of a portion of a semiconductor chip is illustrated in Figure 6 having two N channel transistors in series between V_{OUT} and V_{EE} . An N type substrate is shown having a P channel field effect transistor and two series connected N channel field effect transistors. The source of the P channel transistor is connected to voltage V_{DD} . The drain of the P channel transistor is connected to V_{OUT} and to the drain of one of the N channel transistors. The gates of the two N channel transistors are connected together. The source of each of the N channel transistors is connected to the P tub of each respective transistor. The source and P tub of one of the N channel transistors is connected to voltage V_{EE} .

By now it should be appreciated that there has been provided a high voltage CMOS circuit which does not require changes to the semiconductor process. This high voltage CMOS circuit is readily integrated into a single chip.

CLAIMS

1. A high voltage CMOS monolithic integrated circuit comprising a first MOS transistor of a first channel conductivity type having an electrode coupled to a first voltage terminal; first and second MOS transistors of a second channel conductivity type, all of said transistors being coupled in series, said first and second transistors of second channel conductivity type having first and second electrodes and the gate electrodes thereof coupled together to form an inverter circuit, characterised in that said first and second transistors of second channel conductivity each have a separate tub, the tub of the first transistor of second channel conductivity type being connected to both the second electrode thereof and to the first electrode of the second transistor of second channel conductivity type, and the tub of the second transistor of second channel conductivity type being connected to both the second electrode thereof and a second voltage terminal.
2. A CMOS integrated circuit having high voltage



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40 transistors 63 and 64 are in parallel with transistors 65 and 66. N channel transistors 63 and 64 have their gate electrodes connected to the gate electrode of transistor 62 which is also connected to input B. Output node 67 is connected to output $A + B$. It will
45 be noted that logic gate 60 is similar to a typical prior art CMOS logic gate with the addition of composite N channel transistors to increase the breakdown voltage of the CMOS logic gate. Each of the CMOS transistors has an independent tub which is connected to the respective source of the transistor.
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90 Figure 6 having two N channel transistors in series between V_{OUT} and V_{EE} . An N type substrate is shown having a P channel field effect transistor and two series connected N channel field transistors. The source of the P channel transistor is connected to
95 voltage V_{DD} . The drain of the P channel transistor is connected to V_{OUT} and to the drain of one of the N channel transistors. The gates of the two N channel transistors are connected together. The source of each of the N channel transistors is connected to the
100 P tub of each respective transistor. The source and P tub of one of the N channel transistors is connected to voltage V_{EE} .

By now it should be appreciated that there has been provided a high voltage CMOS circuit which
105 does not require changes to the semiconductor process. This high voltage CMOS circuit is readily integrated into a single chip.

CLAIMS

1. A high voltage CMOS monolithic integrated circuit comprising a first MOS transistor of a first channel conductivity type having an electrode coupled to a first voltage terminal; first and second MOS
115 transistors of a second channel conductivity type, all of said transistors being coupled in series, said first and second transistors of second channel conductivity type having first and second electrodes and the gate electrodes thereof coupled together to form an inverter circuit, characterised in that said first and
120 second transistors of second channel conductivity each have a separate tub, the tub of the first transistor of second channel conductivity type being connected to both the second electrode thereof and to the first electrode of the second transistor of
125 second channel conductivity type, and the tub of the second transistor of second channel conductivity type being connected to both the second electrode thereof and a second voltage terminal.
2. A CMOS integrated circuit having high voltage
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capability, comprising a P channel field effect transistor having a first electrode, a second electrode and a gate electrode, the first electrode capable of being coupled to a first voltage potential; a first N channel field effect transistor having a first and a second electrode and a gate electrode, the first electrode of the first N channel transistor being coupled to the second electrode of the P channel transistor and forming an output junction for the circuit; a second N channel field effect transistor having a first and a second electrode and a gate electrode, the first electrode of the second N channel transistor being coupled to the second electrode of the first N channel transistor, the second electrode of the second N channel being capable of being coupled to a second voltage potential, and the gate electrodes of the P channel and first and second N channel transistors all being coupled together; and a level shift means for providing a voltage level shift to an input voltage, the level shift means providing an output coupled to the gate electrodes of the P channel and first and second N channel transistors, the first and second N channel field effect transistors each having a tub and each tub being connected to the second electrode of each respective transistor.

3. A CMOS circuit having high voltage capability and being able to provide a voltage level shift, comprising a first N channel transistor having a first and a second electrode and a gate electrode, the gate electrode being coupled to the first electrode; a second N channel transistor having a first and a second electrode and a gate electrode, the first electrode of the second N channel transistor being coupled to the second electrode of the first N channel transistor, the second electrode of the second N channel transistor being connectable to a first voltage potential terminal, the gate electrode of the second N channel transistor being coupled to the gate electrode of the first transistor; means for providing a resistance coupled between the first electrode of the first N channel transistor and a second voltage potential terminal; a P channel transistor coupled between the second voltage potential and an output node and having a gate electrode for receiving an input to the circuit; a third N channel transistor having a first and a second electrode and a gate electrode, the first electrode of the third N channel transistor being coupled to the output node, the gate electrode of the third N channel transistor being coupled to the gate of the first N channel transistor; and a fourth N channel transistor having a first and a second electrode and a gate electrode, the first electrode of the fourth N channel transistor being coupled to the second electrode of the third N channel transistor, the second electrode of the fourth N channel transistor being coupled to the first voltage potential terminal, the gate electrode of the fourth N channel transistor being coupled to the gate electrodes of the first, second and third N channel transistors, each of the N channel transistors having a separate tub and each tub being connected to a respective second electrode.

4. A CMOS circuit having high voltage capability and providing a voltage level shift between an input

and an output of the circuit comprising a first P channel transistor coupled between a first voltage potential terminal and a first node and having a gate electrode coupled to the input of the circuit; a first and a second N channel transistor coupled in series between the first node and a second voltage potential terminal and having gate electrodes coupled to the output of the circuit; a second P channel transistor coupled between the first voltage potential terminal and the output and having a gate electrode for receiving a complement of a signal receivable by the input of the circuit; and a third and fourth N channel transistor coupled in series between the output and the second voltage potential terminal and having gate electrodes coupled to the first node, each N channel transistor having a separate tub which is connected to a source of its respective transistor.

5. A CMOS circuit having high voltage capability and capable of performing a logic gate function and having at least a first and a second input and an output, comprising: a first and a second P channel transistor coupled in series between a first voltage potential node and the output, each P channel transistor having a gate electrode serving as an input for the circuit, a first and second N channel transistor coupled in series between the output and a second voltage potential node and having gate electrodes coupled to the first input of the circuit; and a third and fourth N channel transistor coupled in series between the output and the second voltage potential node and having gate electrodes coupled to the second input of the circuit; each of the N channel transistors having a separate tub connected to a source of the respective N channel transistor.

6. A CMOS circuit having high voltage capability and having at least a first and a second input and an output and being capable of performing a logic gate function, comprising: a first and a second P channel transistor coupled in parallel between a first voltage node and the output, the first P channel transistor having a gate electrode coupled to the first input and the second P channel transistor having a gate electrode coupled to the second input; a first and a second N channel transistor connected in series and coupled to the output, the first N channel transistor having a gate electrode coupled to the first input and the second N channel transistor having a gate electrode coupled to the second input; and a third and a fourth N channel transistor coupled in series between a second voltage node and the first and second N channel transistors, the third N channel transistors having a gate electrode coupled to the first input and the fourth N channel transistor having a gate electrode coupled to the second input, each of the N channel transistors having a separate tub, the tubs of the first and second N channel transistors being connected to the source of the second N channel transistor, the tubs of the third and fourth transistors being coupled to the second voltage node to provide at least two N channel transistors in series in a nonconducting state when the output is at a potential substantially equal to a voltage present at the first voltage node.

8. A CMOS monolithic integrated circuit compris-



ing at least one load means coupled between a first voltage node and an output of the circuit and first and second MOS transistors of a first channel conductivity type coupled in series between the
5 output of the circuit and a second voltage node, said MOS first and second transistors having separate tubs connected to their respective sources to provide at least one tub free from direct connection to the voltage nodes.

10 9. A CMOS circuit as claimed in claim 8 wherein said load means is an MOS transistor of second channel conductivity type.

15 10. A CMOS circuit substantially as hereinbefore described and as shown in the accompanying drawings.

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