

52
ANALOG DELAY CIRCUIT
ABSTRACT OF THE DISCLOSURE

An analog delay circuit which includes an analog memory circuit wherein a plurality of memory cells each including a memory capacitor and a selection switch for the memory capacitor are arranged in a matrix includes row switches provided for the individual columns for individually being driven by row selection signals. A same clock signal from a clock generation circuit is supplied commonly to an X direction scanning circuit and a Y direction scanning circuit. The number of stages of registers of the X direction scanning circuit and the number of stages of registers of the Y direction scanning circuit are set so that they have no common divisor other than 1. Consequently, when the memory cells are to be selectively scanned, a same selection condition can be provided to all of the memory cells without relying upon the positions of the memory cells, and the parasitic capacitance connected to a signal write/read terminal is reduced.

Figure 12