Resistor With Reduced Leakage

[0001] This application claims the benefit of U.S. Provisional Application No. 60/496,310, filed on August 18, 2003, which application is hereby incorporated herein by reference.

CROSS-REFERENCE TO RELATED APPLICATIONS

[0002] This application relates to the following patents and co-pending, commonly-assigned patent applications. Each of these documents is incorporated herein by reference.

Patent or Serial No	Filing Date	Issue Date
10/641,813	August 15, 2003	_____
10/628,020	July 25, 2003	_____

TECHNICAL FIELD

[0003] The present invention relates generally to semiconductor devices and more particularly to a resistor with reduced leakage.

BACKGROUND

[0004] Resistors are commonly used in semiconductor integrated circuits. Resistors are used, for example, in analog and in mixed mode analog and digital circuits. Resistors are also used in input and output circuits as input and output resistors.

[0005] In integrated circuits formed on silicon-on-insulator substrates, a resistor may be formed in a portion of a single crystal silicon layer. Such a single crystal resistor has high stability and low noise, compared with conventional polycrystalline resistor structures. Resistors should also have low parasitic capacitance. Resistors formed on silicon-on-insulator

substrates have extremely low parasitic capacitance due to full dielectric isolation and the insulating substrate.

[0006] In resistors formed on silicon-on-insulator substrates, the resistor body is usually formed below a silicon oxide layer, which underlies a polycrystalline silicon layer. The polycrystalline silicon layer is usually connected to one of the two terminals of the resistor. With complementary metal-oxide-semiconductor (CMOS) technology scaling, the thickness of the silicon oxide layer is progressively reduced. As the thickness of silicon oxide layer is reduced, leakage current between the polycrystalline silicon layer and the resistor body increases. The increased leakage current results in increased noise.

[0007] In addition, resistors are sometimes used as part of an input protection circuit to provide protection of the circuit against electrostatic discharge (ESD) events. In this case, the resistor is used to both attenuate the ESD voltage and also to absorb ESD energy. Large voltages in the order of thousands of volts may appear across the two terminals of the resistor used for ESD applications. Since the polycrystalline silicon layer and the resistor body are connected to the two terminals of the resistor, the silicon oxide layer between the polycrystalline silicon layer and the resistor body may potentially breakdown.

SUMMARY OF THE INVENTION

[0008] In the preferred embodiment, a resistor with reduced leakage and noise is provided. A method of fabricating the resistor is also provided.

[0009] In accordance with a preferred embodiment of the present invention, a resistor is formed in a semiconductor layer, e.g., a silicon layer on an SOI substrate. A body region is formed in a portion of the semiconductor layer and is doped to a first conductivity type. A first contact region, which is also doped to the first conductivity type, is formed in the semiconductor layer adjacent the body region. A second contact region is also formed in the semiconductor layer spaced from the first contact region by the body region. The second contact region is doped to the first conductivity type. A dielectric layer overlies the body region and is formed from a material with a relative permittivity greater than about 8. An electrode overlies the dielectric.

[0010] According to another aspect of the invention, a silicon-on-insulator resistor includes a silicon layer that overlies an insulator layer. A body region is formed in a portion of the silicon layer and a dielectric layer overlies the body region. Preferably, the dielectric is a high permittivity dielectric layer. A top electrode overlies the dielectric layer and a pair of doped regions are formed in the silicon layer oppositely adjacent the body region. The pair of doped regions is doped to the same conductivity type as the body region.

[0011] In yet another embodiment, a silicon-on-insulator device includes a substrate and an insulator layer overlying the substrate. An active area is formed in a silicon layer overlying the insulator layer. A body region of a first conductivity type is formed in a portion of the silicon layer. An interfacial layer, e.g., SiO_2 or SiON, overlies and abuts the body region. A high-k

dielectric layer, e.g., a layer having a relative permittivity greater than about 8, overlies the interfacial layer. A top electrode overlies the high-k dielectric layer. A pair of doped regions of the first conductivity type are formed in the active area oppositely adjacent the body region.

[0012] A resistor of the preferred embodiment can be formed by providing a silicon-on-insulator substrate that includes a silicon layer overlying an insulator layer. A resistor body of a first conductivity type is formed in a portion of the silicon layer, e.g., by doping the portion of the layer. A dielectric layer, e.g., with a relative permittivity greater than about 8, overlies the body region. A top electrode is formed on the dielectric layer and a pair of doped regions are formed oppositely adjacent the body region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

[0014] Figure 1 shows a first embodiment silicon-on-insulator resistor;

[0015] Figure 2 shows a second embodiment silicon-on-insulator resistor;

[0016] Figure 3a shows a top view of a resistor of one embodiment of the invention;

[0017] Figures 3b and 3c show cross sectional views of the resistor of Figure 3a;

[0018] Figure 4 shows an SOI transistor and resistor formed on the same chip;

[0019] Figures 5a-5f show cross-sectional views of a device during various stages of fabrication;

[0020] Figure 6 shows an example of a circuit that can include a resistor of the present invention; and

[0021] Figure 7 shows an example of a diode that can be implemented on the same chip as a resistor of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0022] In aspects of this invention, resistors with reduced leakage current are taught. Such resistors may be formed on a semiconductor-on-insulator (SOI) substrate. In the preferred embodiment, the semiconductor-on-insulator substrate is a silicon-on-insulator substrate having a silicon layer overlying a silicon oxide layer which in turn overlies a substrate. The silicon layer in the silicon-on-insulator substrate may be relaxed silicon or strained silicon.

[0023] Referring now to Figure 1, a cross-section of a resistor 100 of the preferred embodiment is depicted. In this example, the device is formed on a silicon-on-insulator substrate, which includes a substrate 102, a buried insulator layer 104 and a semiconductor layer 106. The resistor has a body region 108, or resistor body 108, formed within a portion of the silicon layer 106. A pair of doped regions 110 and 112 are formed oppositely adjacent to the resistor body 108.

[0024] Although not shown in this figure, the doped regions may be silicided to form low resistance regions. In addition, to prevent the silicidation of the body region of the resistor, a stack comprising of a top electrode 114 (usually polycrystalline silicon) on a dielectric 116 is formed on the resistor body 108, as shown in Figure 1. The dielectric 116 may be formed from the same dielectric layer used by transistors formed on other portions of the integrated circuit. Therefore, the thickness of the dielectric 116 tends to be scaled towards smaller thicknesses as technology progresses.

[0025] As shown substantially in Figure 1, the doped regions 110 and 112 electrically communicate with other portions of the integrated circuit. For example, a first terminal 118 of the resistor 100 may be connected to ground potential (labeled GND), and a second terminal 120

may be connected to a circuit node with a potential V. The potential V may be at a potential higher than ground potential. As a result, a current flows through the resistor along a first current path 122. The resistor body 108 predominantly contributes to the resistance seen between the two terminals 118 and 120 of the resistor.

[0026] A second current path also exists between the two terminals 118 and 120 of the resistor. This path is labeled with reference number 124 in Figure 1. The second current path 124 shunts the first current path 122, and may adversely affect the properties of the resistor 100. The current flowing along the second current path 124 increases with reduced dielectric 116 thickness. This is because when the dielectric thickness is small, quantum mechanical tunneling of charge carriers may occur through the dielectric 116. According to the preferred embodiment of this invention, by incorporating at least a high permittivity (high-k) material in the dielectric 116, the dielectric thickness may be increased while maintaining the same capacitive properties. As a result of the increase of the dielectric thickness, the leakage current flowing along the second current path 124 may be significantly suppressed.

[0027] Therefore, in the preferred embodiment of the present invention, the dielectric 116 that overlies the resistor body 108 comprises a high permittivity (high-k) dielectric. By using a high-k dielectric, the thickness of the dielectric 116 can be significantly larger than that if a silicon oxide dielectric is employed. The high-k dielectric preferably has a permittivity of larger than about 8, and more preferably has a permittivity of larger than about 10, and even more preferably has a permittivity of larger than about 20. The high permittivity dielectric 116 may be one of the following materials: aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), hafnium oxynitride (HfON), hafnium silicate ($HfSiO_4$), zirconium oxide (ZrO_2), zirconium oxynitride (ZrON), zirconium silicate ($ZrSiO_4$), yttrium oxide (Y_2O_3), lanthanum oxide (La_2O_3), cerium

oxide (CeO_2), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), and combinations thereof. In the preferred embodiment, the high-k dielectric 116 is hafnium oxide. The dielectric 116 may additionally comprise silicon oxide (SiO_2), silicon oxynitride (SiON), or silicon nitride (Si_3N_4).

[0028] The silicon oxide equivalent thickness (EOT) of the dielectric is preferably larger than about 5 angstroms, more preferably larger than about 10 angstroms, and even more preferably larger than about 20 angstroms. The physical thickness of the dielectric may be larger than about 5 angstroms, more preferably larger than about 20 angstroms, and even more preferably larger than about 40 angstroms.

[0029] The top electrode 114 comprises a conductive material such as polycrystalline or amorphous silicon, polycrystalline silicon-germanium, a metal, a metallic nitride, a metallic silicide, or a metallic oxide, and combinations thereof. In the preferred embodiment, the top electrode 114 comprises polycrystalline silicon possibly in combination with a silicide layer.

[0030] Metals such as molybdenum, tungsten, titanium, tantalum, platinum, and hafnium may be used as the portion of the top electrode 114. Metallic nitrides may include, but will not be restricted to, molybdenum nitride, tungsten nitride, titanium nitride, and tantalum nitride. Metallic silicides may include, but will not be restricted to, nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, and erbium silicide. Metallic oxides may include, but will not be restricted to, ruthenium oxide and indium tin oxide.

[0031] It should be noted that the resistor body 108 thickness is preferably in the range of about 20 angstroms to about 1000 angstroms, and more preferably in the range of about 20 angstroms to about 400 angstroms. As such, the first current path 122 flows in close proximity to the interface between the resistor body 108 and the dielectric 116. As a result, measures should be taken to ensure that the interface 108/116 has a low interface trap density of less than

about 10^{10} cm^{-2}. Interface traps result in charge carriers flowing in the resistor to be instantaneously trapped or detrapped, causing an instantaneously decrease or increase in the current, respectively. This manifests as a current noise source in the resistor.

[0032] To reduce the amount of current noise, the dielectric 116 overlying the resistor body 108 preferably comprises of at least two layers: a high-k dielectric 126 overlying an interfacial dielectric layer 128, as shown in Figure 2. The interfacial dielectric layer 128 is preferably one that has excellent interfacial properties in contact with the resistor body 108. In the preferred embodiment, the interfacial layer 128 comprises silicon oxide (e.g., SiO_2) or silicon oxynitride (e.g., SiO_xN_y).

[0033] The resistor body 108 may be doped n-type or p-type. The doped regions 110 and 112 adjacent to the resistor body 108 are doped the same type as the resistor body 108. The doped regions 110 and 112 preferably have a high doping concentration, e.g., between about 10^{18} cm^{-3} and about $5x10^{21}$ cm^{-3}. The resistor body 108 has a doping concentration that is lower and is selected to provide the desired resistivity. Typical values are between about 10^{16} cm^{-3} and 10^{19} cm^{-3}.

[0034] Figure 3a shows a top view or layout view of a resistor 100 of an embodiment of this invention. The resistor has a width *W* and a length *L*. In the preferred embodiment, the width *W* may have a dimension of larger than about 0.1 microns, and preferably larger than about 1 micron. In the preferred embodiment, the length *L* may have a dimension of larger than about 0.1 micron, and preferably larger than about 1 micron. The detailed structure of the resistor may be seen in cross-sectional views along the lines 3b-3b' and 3c-3c'.

[0035] The detailed cross-sectional view along line 3b-3b' of Figure 3a is shown in Figure 3b. The top electrode 114 extends laterally into the isolation regions 130. The isolation region

116 may comprise isolation structures known and used in the art, such as shallow trench isolation. The shallow trench isolation structure may comprise a dielectric filling material such as chemical vapor deposited silicon oxide. The shallow trench isolation structure may also comprise trench liner oxide (not shown for simplicity) on the boundaries of the trench. The trench liner oxide may or may not contain nitrogen.

[0036] Other isolation types could alternately be used. For example, Figure 1 showed an active region 106 surrounded by mesa isolation. It is understood that the resistor may be used in a semiconductor-on-insulator technology employing trench isolation, or may be used in a semiconductor-on-insulator technology employing mesa isolation. In mesa isolation, trenches are not filled with a dielectric filling material prior to the formation of transistors or resistors.

[0037] The top electrode in Figure 3b is shown to have a thickness *t*, preferably in the range of about 200 angstroms to about 2000 angstroms. The resistor structure may additionally have spacers 132 formed on the sides of the top electrode 114. The top electrode 114 may be formed of the same material as the gate electrode of a transistor formed in another portion of the integrated circuit, as shown in Figure 4.

[0038] The cross-sectional view along line 3c-3c' is shown in Figure 3c. This view shows the doped regions 110 and 112.

[0039] Referring now to Figure 4, the resistor 100 may be formed in an active region 106c in the vicinity of an active device 140 such as a transistor. In Figure 4, transistor 140 is formed in active region 106a and includes source region 142, drain region 144, gate dielectric 146 and gate electrode 148. The resistor dielectric 116 may or may not be the same dielectric material as the transistor gate dielectric 146. The gate electrode 114 of the resistor 100 may or may not be formed of the same material as the gate electrode 148 of the transistor 140. In a typical

embodiment, the distance between doped regions 110 and 112 is typically between about 2 and 100 times greater the channel length of transistor 140 (i.e., the distance between source and drain regions 142 and 144).

[0040] Next, a method of manufacturing the resistor is to be described with respect to Figures 5a-5f, which are taken along the same cross-sectional line as Figure 3b. Referring first to Figure 5a, a semiconductor-on-insulator substrate, including substrate 102, insulator 104 and semiconductor layer 106, is provided and an active region mask 150 is used to define trenches 152 in the semiconductor layer 106. The semiconductor layer 106 preferably has a thickness of about 1000 angstroms or thinner. The insulator 104 thickness is preferably about 1200 angstroms or thinner. The mask 150 preferably comprises silicon nitride, and more preferably comprises silicon nitride on a silicon oxide layer.

[0041] Trench filling dielectric material is deposited by chemical vapor deposition to fill the trenches 152, followed by a chemical mechanical planarization process step. These steps create isolation region 130. The mask 150 is then removed to give the cross-section shown in Figure 5b.

[0042] An ion implantation process step may be performed to dope the active region, a portion of which will become the resistor body 108. The dose of the implantation will determine the resistivity of the semiconductor layer and therefore the resistance of the resistor. For example, an implant dose in the range of about 10^{13} to about 10^{16} cm^{-2} may be used.

[0043] A dielectric 116 comprising a high-k material is then formed over the active region 106, as shown in Figure 5c. The physical thickness of the dielectric may be larger than about 5 angstroms, more preferably larger than about 20 angstroms, and even more preferably larger than

about 40 angstroms. Further, the dielectric may be smaller than about 200 angstroms, preferably smaller than about 100 angstroms and most preferably smaller than about 50 angstroms.

[0044] The dielectric 116 may be formed together with the formation of a transistor gate dielectric 146 in a different portion of the semiconductor chip (see Figure 4). By forming the dielectric 116 together with the gate dielectric 146 of a transistor in a different portion of the chip, no additional process steps are introduced. High-k dielectric materials as previously described may be used. The high-k dielectric may be formed by chemical vapor deposition, sputter deposition, or other known techniques of forming high-k dielectric materials.

[0045] An interfacial layer (see Figure 2) may be formed on the body region 108 prior to the formation of the high-k dielectric material. The interfacial layer may be a silicon oxide layer or a silicon oxynitride layer, and may be formed by thermal oxidation and/or nitridation. The active region 106 may additionally be treated in a hydrogen-containing or nitrogen-containing ambient prior to the formation of the interfacial layer.

[0046] Referring now to Figure 5d, the top electrode material 114 can then be deposited over the dielectric layer 116. The top electrode 114 material can be amorphous or polycrystalline silicon, polycrystalline silicon germanium, metals, metallic silicides, or metallic nitrides, as previously described. The electrode 114 material can be deposited by conventional techniques such as chemical vapor deposition. For example, the electrode 114 may also be formed by the deposition of silicon and metal, followed by an anneal to form a metal silicide electrode that includes silicon portion 160 and silicide portion 162. The electrode material is then patterned using photolithography techniques, and etched using plasma etch processes to form the electrodes 114.

[0047] The deposition of the top electrode material may be the same process step as the deposition of gate electrode material of a transistor to be formed in a different portion of the semiconductor chip, and the etching of the top electrode may similarly be accomplished together with the etching of the gate electrode of the said transistor. The completed top electrode is shown in Figure 5d. The dielectric 118 is retained at least in the portion of the resistor covered by the electrode 114. Doping may be introduced in regions 110 and 112 (see Figures 1, 2 or 3c) adjacent to the body region 108 to make electrical contacts with the resistor body 108.

[0048] As shown in Figure 5e, spacers 132 may be additionally formed on the sides of the electrode 114. This may be followed by another implant to the doped regions (110 and 112) of the active region 106 not covered by the spacers 132 or electrode 114. A contact etch-stop layer 154 may be formed on the electrode 114 and spacers 132. An inter-layer dielectric (ILD) 156 may be formed over the resistor and contact holes etched through the ILD 156 to reach the electrode 114 and the doped regions (110 and 112) of the resistor. Conductive materials (e.g., tungsten) are then used to fill the contact holes to form contact plugs 158, as shown in Figure 5f.

[0049] The resistor of the present invention can be used in a number of circuits. Figure 6 provides but one example, namely an electrostatic discharge (ESD) protection circuit. This circuit will now be described.

[0050] Figure 6 shows an example of how concepts of the present invention can be deployed for protection of integrated circuits. In this example, resistors 100 and 100' are coupled between an I/O pad 166 and two circuit portions 168 and 170. The resistors 100 and 100' can be any of the various embodiment resistors described in this specification. In this example, the circuit portion 168 is labeled as an output circuit and the circuit portion 170 is labeled as an input

circuit. It is understood, however, that these circuit portions can be any circuit that should be shielded from high voltages.

[0051] The I/O pad 166 is provided to indicate any node that might be subject to a high voltage. The most typical of these nodes are the inputs and outputs between the chip and the outside world (e.g., external circuitry when connected to a system or handling devices when the system is being assembled). The pad 166 is indicated as being an I/O pad, which stands for input/output. It is noted, however, that in this patent the term I/O is meant to include pads for input only, output only or both input and output (or any other node that might be subject to a high voltage).

[0052] The circuit of Figure 6, also shows a first diode string 172 coupled between a supply voltage source V_{DD} (e.g., a voltage source of 5V, 3.3V, 2.5V or 1.8V) and the I/O pad 166 and a second diode string 174 coupled between a supply voltage source V_{SS} and the I/O pad 166. Each diode string 172 and 174 includes one or more diodes 176. In the preferred embodiment, the diode 176 comprises a diode of the type described in co-pending application Serial No. 10/641,813 (attorney docket TSM03-0554), which is incorporated herein by reference. For example, diode string 172 can include a diode 176 with a p-doped region coupled to I/O pad 166 and another 176 (or the same diode in a one diode string) with an n-doped region coupled to V_{DD}. The diode string 174 is coupled between the I/O pad 166 and the reference voltage V_{SS} (e.g., ground). In this case, a p-doped region is coupled to ground and an n-doped region is coupled to the pad 166.

[0053] Figure 7 shows a cross-sectional view of a gated diode 176. Except for reference numbers, Figure 7 is the same as Figure 4 in the co-pending '813 application. In the illustrated

example, the diode 176 is formed in a bulk semiconductor substrate 102. In another example, the diode can be formed in the semiconductor layer 106 (e.g., of Figure 1 or 2).

[0054] The gated diode 176 includes an n+ doped region 178 and a p+ doped region 180 that are separated by a body region 182. A gate 184 overlies the body region 182 and is separated therefrom by a dielectric 186. In the illustrated embodiment, the gate includes an n-doped portion 188 adjacent a p-doped portion 190. In other embodiments, other conductors can be used to form the gate 184. Figure 7 also shows spacers 192 and conductive regions 194 (e.g., silicide) as described previously.

[0055] In the preferred embodiment, dielectric layer 186 comprises a high-k dielectric. In fact, the dielectric layer 186 can be formed from the same layer that is used to formed dielectric layer 116 for the resistors as described above. Combining process steps in the formation of resistors 100, diodes 176 and transistors 140 (e.g., components of circuits 168 and 170) simplifies the formation of circuits, such as the ESD protection circuit of Figure 6.

[0056] While diode 176 is described herein with respect to a specific example, it is understood that any of the variations and embodiments described in the co-pending and incorporated '183 application can be utilized in the present invention.

[0057] In the foregoing specification, the invention has been described with reference to specific embodiments. However, various modifications and changes can be made by one skilled in the art without departing from the scope of the preferred embodiment. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the preferred embodiment.

WHAT IS CLAIMED IS:

1. A resistor comprising:

a semiconductor layer;

a body region formed in a portion of the semiconductor layer, the body region being doped to a first conductivity type and having a first resistivity;

a first contact region formed in the semiconductor layer adjacent the body region, the first contact region being doped to the first conductivity type;

a second contact region formed in the semiconductor layer spaced from the first contact region by the body region, the second contact region being doped to the first conductivity type;

a dielectric layer overlying the body region, said dielectric comprising a material with a relative permittivity greater than about 8; and

an electrode overlying said dielectric.

2. The resistor of claim 1 wherein the dielectric layer comprises a material selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide, cerium oxide, titanium oxide, tantalum oxide, and combinations thereof.

3. The resistor of claim 1 wherein the dielectric layer has a relative permittivity greater than about 10.

4. The resistor of claim 1 wherein the dielectric layer has a relative permittivity greater than about 20.

5. The resistor of claim 1 wherein the dielectric layer has a physical thickness greater than about 5 angstroms.

6. The resistor of claim 1 wherein the dielectric layer has a physical thickness greater than about 20 angstroms.

7. The resistor of claim 1 wherein the dielectric layer has a physical thickness greater than about 40 angstroms.

8. The resistor of claim 1 wherein the semiconductor layer comprises a silicon layer.

9. The resistor of claim 1 wherein the semiconductor comprises silicon and germanium.

10. The resistor of claim 1 wherein the semiconductor layer has a thickness in the range of about 20 angstroms to about 400 angstroms.

11. The resistor of claim 1 further comprising an insulator layer underlying the semiconductor layer.

12. The resistor of claim 11 wherein the insulator layer comprises silicon oxide.

13. The resistor of claim 1 wherein the electrode comprises a semiconductor.

14. The resistor of claim 1 wherein the electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

15. The resistor of claim 1 wherein the electrode comprises a metallic nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, and tantalum nitride, and combinations thereof.

16. The resistor of claim 1 wherein the electrode comprises a metallic silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, and erbium silicide, and combinations thereof.

17. The resistor of claim 1 wherein the electrode comprises a metallic oxide selected from the group consisting of ruthenium oxide, and indium tin oxide, and combinations thereof.

18. The resistor of claim 1 wherein the electrode has a width larger than about 0.1 microns.

19. The resistor of claim 1 wherein the electrode has a width larger than about 1 micron.

20. The resistor of claim 1 wherein the electrode has a length larger than about 0.1 microns.

21. The resistor of claim 1 wherein the electrode has a length larger than about 1 micron.

22. The resistor of claim 1 wherein the first conductivity type is n-type.

23. The resistor of claim 1 wherein the first conductivity type is p-type.

24. The resistor of claim 1 further comprising spacers formed on sides of the electrode.

25. The resistor of claim 24 wherein the spacers comprise silicon nitride.

26. The resistor of claim 24 further comprising an etch-stop layer overlying the electrode and the spacers.

27. The resistor of claim 26 wherein the etch-stop layer comprise silicon nitride.

28. A silicon-on-insulator resistor comprising:

a silicon layer overlying an insulator layer;

a body region formed in a portion of the silicon layer;

a dielectric layer overlying the body region, said dielectric comprising a high permittivity dielectric layer;

a top electrode overlying said dielectric layer; and

a pair of doped regions formed in the silicon layer oppositely adjacent the body region, the pair of doped regions being doped to the same conductivity type as the body region.

29. The resistor of claim 28 wherein the high permittivity dielectric is selected from a group comprising of aluminum oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide, cerium oxide, titanium oxide, and tantalum oxide, and combinations thereof.

30. The resistor of claim 28 wherein the permittivity dielectric layer comprises hafnium oxide.

31. The resistor of claim 28 wherein the high permittivity dielectric has a relative permittivity greater than about 8.

32. The resistor of claim 28 wherein the high permittivity dielectric has a relative permittivity greater than about 10.

33. The resistor of claim 28 wherein the high permittivity dielectric has a relative permittivity greater than about 20.

34. The resistor of claim 28 wherein the dielectric has a physical thickness greater than about 5 angstroms.

35. The resistor of claim 28 wherein the dielectric has a physical thickness greater than about 20 angstroms.

36. The resistor of claim 28 wherein the dielectric has a physical thickness greater than about 40 angstroms.

37. The resistor of claim 28 wherein the silicon layer is a strained silicon layer.

38. The resistor of claim 28 wherein the silicon layer has a thickness in the range of about 20 angstroms to about 1000 angstroms.

39. The resistor of claim 28 wherein the silicon layer has a thickness in the range of about 20 angstroms to about 400 angstroms.

40. The resistor of claim 28 wherein the insulator layer comprises silicon oxide.

41. The resistor of claim 28 wherein the electrode comprises polycrystalline silicon, polycrystalline silicon-germanium, a metal, a metallic nitride, a metallic silicide, and a metallic oxide, and combinations thereof.

42. The resistor of claim 41 wherein the metal is selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

43. The resistor of claim 41 wherein the metallic nitride is selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, and tantalum nitride, and combinations thereof.

44. The resistor of claim 41 wherein the metallic silicide is selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, and erbium silicide, and combinations thereof.

45. The resistor of claim 28 wherein the electrode has a width greater than about 0.1 microns.

46. The resistor of claim 28 wherein the electrode has a width greater than about 1 micron.

47. The resistor of claim 28 wherein the electrode has a length greater than about 0.1 microns.

48. The resistor of claim 28 wherein the electrode has a length greater than about 1 micron.

49. The resistor of claim 28 wherein the body and the doped regions are doped n-type.

50. The resistor of claim 28 wherein the body and the doped regions are doped p-type.

51. The resistor of claim 28 further comprising spacers formed on sides of the electrode.

52. The resistor of claim 51 wherein the spacers comprise silicon nitride.

53. The resistor of claim 51 further comprising an etch-stop layer overlying the electrode and the spacers.

54. The resistor of claim 53 wherein the etch-stop layer comprise silicon nitride.

55. The resistor of claim 54 further comprising an inter-layer dielectric overlying the etch-stop layer.

56. The resistor of claim 55 wherein the inter-layer dielectric comprises silicon oxide.

57. The resistor of claim 55 further comprising a contact plug formed through the inter-layer dielectric and in electrical contact with the resistor.

58. The resistor of claim 28 further comprising a shallow trench isolation region adjacent the silicon layer.

59. The resistor of claim 28 wherein the resistor is formed in an active area of the silicon layer and wherein the active area is isolated from other active areas that overlie the insulator layer by mesa isolation.

60. A method of forming a resistor, the method comprising:

providing a silicon-on-insulator substrate that includes a silicon layer overlying an insulator layer;

forming a resistor body of a first conductivity type in a portion of the silicon layer;

forming a dielectric layer overlying the body region, the dielectric layer comprising a material with a relative permittivity greater than about 8;

forming a top electrode on the dielectric layer; and

forming a pair of doped regions of the first conductivity type oppositely adjacent the body region.

61. The method of claim 60 wherein forming the resistor body comprises:

forming an active region;

forming isolation regions surrounding the active region; and

doping the active region.

62. The method of claim 61 wherein doping the active region employs an ion implantation with a dose in the range of about 10^{13} to about 10^{16} cm^{-2}.

63. The method of claim 60 wherein forming the dielectric layer comprises a chemical vapor deposition step.

64. The method of claim 60 wherein forming the dielectric layer comprises a sputtering deposition step.

65. The method of claim 60 wherein forming the dielectric layer comprises:

forming an interfacial oxide layer; and

forming a high permittivity dielectric layer.

66. The method of claim 60 wherein forming the pair of doped regions comprises:

doping a portion of the silicon layer not covered by the top electrode;

forming spacers on sidewalls of the top electrode; and

doping a portion of the silicon layer not covered by the top electrode and the spacers.

67. The method of claim 66 wherein the spacers comprise silicon nitride.

68. The method of claim 66 further comprising:

depositing an etch-stop layer over the top electrode and the spacers;

forming an inter-layer dielectric over the etch-stop layer;

forming contact holes in the inter-layer dielectric layer; and

filling the contact holes with a conductive material to form contact plugs.

69. The method of claim 68 wherein the etch-stop layer comprises silicon nitride.

70. The method of claim 68 wherein the inter-layer dielectric comprises silicon oxide.

71. The method of claim 68 wherein a first contact plug electrically contacts one of the pair of doped regions and a second contact plug electrically contacts the top electrode, said first and second contact plugs being electrically connected.

72. The method of claim 60 wherein the insulator layer comprises silicon oxide.

73. The method of claim 60 wherein the insulator layer has a thickness of less than about 1200 angstroms.

74. The method of claim 60 wherein the silicon layer has a thickness in the range of about 20 angstroms to about 1000 angstroms.

75. The method of claim 60 wherein the top electrode comprises a semiconductor.

76. The method of claim 60 wherein the top electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

77. The method of claim 60 wherein the top electrode comprises a metallic nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, or combinations thereof.

78. The method of claim 60 wherein the top electrode comprises a metallic silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, and erbium silicide, and combinations thereof.

79. The method of claim 60 wherein the top electrode comprises a metallic oxide selected from the group comprising of ruthenium oxide, and indium tin oxide, and combinations thereof.

80. The method of claim 60 wherein the dielectric layer comprises a material selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, and zirconium silicate, and combinations thereof.

81. The method of claim 60 wherein the dielectric layer has a relative permittivity of larger than about 10.

82. The method of claim 60 wherein the dielectric layer has a relative permittivity of larger than about 20.

83. The method of claim 60 wherein the dielectric has a physical thickness greater than about 5 angstroms.

84. The method of claim 83 wherein the dielectric has a physical thickness greater than about 20 angstroms.

85. The method of claim 84 wherein the dielectric has a physical thickness greater than about 40 angstroms.

86. The method of claim 60 wherein the electrode has a width greater than about 0.1 microns.

87. The method of claim 60 wherein the electrode has a width greater than about 1 micron.

88. The method of claim 60 the electrode has a length greater than about 0.1 microns.

89. The method of claim 61 wherein the electrode has a length greater than about 1 micron.

90. A silicon-on-insulator device comprising:

an active area comprising a silicon layer overlying an insulator layer;

a body region of a first conductivity type formed in a portion of the silicon layer;

a dielectric layer overlying the body region, said dielectric comprising a material selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide, cerium oxide, titanium oxide, tantalum oxide, and combinations thereof;

a top electrode overlying the dielectric layer; and

a pair of doped regions of the first conductivity type formed in the silicon layer oppositely adjacent the body region.

91. The device of claim 90 wherein the dielectric layer comprises hafnium oxide.

92. The device of claim 90 wherein the silicon layer has a thickness in the range of about 20 angstroms to about 400 angstroms.

93. The device of claim 90 and further comprising a second active area overlying the insulator layer, the second active area including a transistor formed therein.

94. The device of claim 93 wherein the transistor includes a gate dielectric formed of the same material as the dielectric layer overlying the body region.

95. The device of claim 93 wherein the transistor includes a gate dielectric formed of a different material as the dielectric layer overlying the body region.

96. The device of claim 93 wherein the transistor includes a gate electrode formed of the same material as the top electrode.

97. The device of claim 90 and further comprising an interfacial layer overlying and abutting the body region, the dielectric layer overlying the interfacial layer.

98. The device of claim 97 wherein the interfacial layer comprises silicon oxide or silicon oxynitride.

99. A silicon-on-insulator device comprising:

a substrate;

an insulator layer overlying the substrate;

an active area formed in a silicon layer overlying the insulator layer;

a body region of a first conductivity type formed in a portion of the silicon layer;

an interfacial layer overlying and abutting the body region;

a high-k dielectric layer overlying the interfacial layer, the high-k dielectric layer comprising a material having a relative permittivity greater than about 8;

a top electrode overlying the high-k dielectric layer; and

a pair of doped regions of the first conductivity type formed in the active area oppositely adjacent the body region.

100. The device of claim 99 wherein the high-k dielectric comprises a material selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide, cerium oxide, titanium oxide, tantalum oxide, and combinations thereof.

101. The device of claim 100 wherein the dielectric layer comprises hafnium oxide.

102. The device of claim 100 and further comprising a second active area overlying the insulator layer, the second active area including a transistor formed therein.

103. The device of claim 102 wherein the transistor includes a gate dielectric comprising a material having a relative permittivity greater than about 8.

104. The device of claim 103 wherein the gate dielectric and the high-k dielectric comprise the same material.

105. The device of claim 102 wherein the transistor includes a gate electrode formed of the same material as the top electrode.

106. The device of claim 99 wherein the interfacial layer comprises silicon oxide.

107. The device of claim 99 wherein the interfacial layer comprises silicon oxynitride.

108. An electrostatic discharge protection circuit comprising:

an I/O pad;

a circuit that is to be protected;

a diode coupled between the I/O pad and a reference voltage node;

a resistor coupled between the I/O pad and the circuit, the resistor including a body region, a first contact region adjacent the body region to electrically couple the body region to the I/O pad, a second contact region adjacent the body region to electrically couple the body region to the circuit, a dielectric layer having a relative permittivity greater than about 8 overlying the body region, and an electrode overlying the dielectric layer.

109. The circuit of claim 108 wherein the diode comprises:

a diode body region;

a diode dielectric having a relative permittivity greater than about 8 overlying the diode body region;

a diode electrode overlying the diode dielectric; and

a p-doped region and an n-doped region oppositely adjacent to the diode body region.

110. The circuit of claim 109 wherein the p-doped region of the diode is electrically coupled to the I/O pad and the n-doped region of the diode is electrically coupled to the reference voltage node.

111. The circuit of claim 109 wherein the n-doped region of the diode is electrically coupled to the I/O pad and the p-doped region of the diode is electrically coupled to the reference voltage node.

112. The circuit of claim 108 and further comprising a second diode coupled between the I/O pad and a second reference voltage node.

113. The circuit of claim 112 wherein the second diode comprises:

a diode body region;

a diode dielectric having a relative permittivity greater than about 8 overlying the diode body region;

a diode electrode overlying the diode dielectric; and

a p-doped region and an n-doped region oppositely adjacent to the diode body region.

114. The circuit of claim 112 and further comprising:

a second circuit; and

a second resistor coupled between the second circuit and the I/O pad, the second resistor comprising a body region, a first contact region adjacent the body region to electrically couple

the body region to the I/O pad, a second contact region adjacent the body region to electrically couple the body region to the second circuit, a dielectric layer having a relative permittivity greater than about 8 overlying the body region, and an electrode overlying the dielectric layer.

115. The circuit of claim 114 wherein the circuit comprises an output circuit and wherein the second circuit comprises an input circuit.