SOLDER BUMP FABRICATION METHODS AND STRUCTURE INCLUDING A TITANIUM BARRIER LAYER

The Government of the United States of America may have rights in this invention pursuant to Contract No. 94-50-001 awarded by the Office of the Advanced Research Projects Agency.

Field of the Invention

This invention relates to microelectronic device manufacturing methods and structures, and more particularly to methods of forming electrical and mechanical connections for a microelectronic device, and the connections so formed.

Background of the Invention

High performance microelectronic devices often use solder balls or solder bumps for electrical interconnection to other microelectronic devices. For example, a very large scale integration (VLSI) chip may be electrically connected to a circuit board or other next level packaging substrate using solder balls or solder bumps. This connection technology is also referred to as "Controlled Collapse Chip Connection - C4" or "flip-chip" technology, and will be referred to herein as solder bumps.

In the original solder bump technology developed by IBM, the solder bumps are formed by evaporation through openings in a shadow mask which is clamped to an integrated circuit wafer. For example, U.S. Patent No. 5,234,149 entitled "Debondable Metallic

Bonding Method" to Katz et al. discloses an electronic device with chip wiring terminals and metallization layers. The wiring terminals are typically essentially aluminum, and the metallization layers may include a titanium or chromium localized adhesive layer, a co-deposited localized chromium copper layer, a localized wettable copper layer, and a localized gold or tin capping layer. An evaporated localized lead-tin solder layer is located on the capping layer.

Solder bump technology based on an electroplating method has also been actively pursued. The electroplating method is particularly useful for larger substrates and smaller bumps. In this method, an "under bump metallurgy" (UBM) layer is deposited on a microelectronic substrate having contact pads thereon, typically by evaporation or sputtering. A continuous under bump metallurgy layer is typically provided on the pads and on the substrate between the pads, in order to allow current flow during solder plating.

An example of an electroplating method with an under bump metallurgy layer is disclosed in U.S. Patent No. 5,162,257 entitled "Solder Bump Fabrication Method" to Yung and assigned to the assignee of the present application. In this patent, the under bump metallurgy layer contains a chromium layer adjacent the substrate and pads, a top copper layer which acts as a solderable metal, and a phased chromium/copper layer between the chromium and copper layers. The base of the solder bump is preserved by converting the under bump metallurgy layer between the solder bump and contact pad into an intermetallic of the solder and the solderable component of the under bump metallurgy layer. Multiple etch cycles may, however, be needed to remove the phased chromium/copper layer and the bottom chromium layer. Even with multiple etch cycles, the under bump metallurgy layer may be difficult to remove

completely, creating the risk of electrical shorts between solder bumps.

Notwithstanding the above mentioned patents, there still exists a need in the art for methods for forming solder bumps and solder bump structures formed thereby wherein the exposed portion of the under bump metallurgy layer can be readily and completely removed after electroplating the solder bumps thereby reducing the possibility of electrical shorts between solder bumps. There also exists a need in the art for a method for forming solder bumps wherein the solder bump need not be significantly undercut when the exposed portion of the under bump metallurgy layer is removed thereby reducing the possibility of mechanical or electrical failure.

Summary of the Invention

It is therefor an object of the present invention to provide an improved method for fabricating solder bumps for microelectronic device contact pads, and improved solder bumps formed thereby.

It is another object of the present invention to reduce the time required to remove the exposed portion of the under bump metallurgy layer after electroplating the solder bump.

It is still another object of the present invention to reduce electrical shorts between solder bumps.

It is yet another object of the present invention to reduce the undercutting of solder bumps when the under bump metallurgy layer is removed after electroplating.

These and other objects are provided according to the present invention by depositing a continuous titanium barrier layer on the microelectronic device before forming the under bump metallurgy layer. Accordingly, the under bump

metallurgy layer can be selectively removed from the titanium layer, and the titanium layer can then be removed from the microelectronic device. The titanium layer prevents the under bump metallurgy layer from forming residues on the microelectronic device which could result in electrical shorts between solder bumps. In addition, the titanium barrier layer protects the underlying microelectronic device from the etchants used to remove the under bump metallurgy layer.

According to one aspect of the present invention, a method for forming solder bumps includes the steps of depositing a titanium barrier layer on the microelectronic device including contact pads, forming an under bump metallurgy layer on the titanium barrier layer, and then forming a solder bump on the under bump metallurgy layer. The solder bump defines exposed portions of the under bump metallurgy layer and the titanium barrier layer which are each selectively removed. Accordingly, the exposed portions of the under bump metallurgy layer can be quickly and completely removed after electroplating solder bumps without significantly undercutting the solder bumps or leaving residues which could result in shorts between solder bumps.

The exposed portion of the under bump metallurgy layer can be selectively removed using etchants which attack the under bump metallurgy layer preferentially with respect to the solder bump and the titanium barrier layer. The titanium barrier layer can then be selectively removed using an etchant that preferentially attacks the titanium barrier layer with respect to the solder bump and the portion of the under bump metallurgy layer remaining beneath the solder bump.

The under bump metallurgy layer preferably comprises a chromium layer on the titanium barrier layer, a phased layer of chromium and copper on the

chromium layer, and a copper layer on the phased layer. In this embodiment, a mixture of ammonium hydroxide and hydrogen peroxide can be used to selectively etch the copper portions of the under bump metallurgy layer; hydrochloric acid can be used to etch the chromium portions of the under bump metallurgy layer; and hydrofluoric acid buffered with ammonium fluoride can be used to selectively etch the titanium layer.

A solder dam can also be formed on the under bump metallurgy layer in areas not to be covered by the solder bump, and this solder dam is preferably removed before removing the exposed portions of the under bump metallurgy layer. The solder dam preferably includes a solder non-wettable layer such as a chromium or titanium layer. The solder dam may also include a layer of a solder wettable material, such as copper, on the solder non-wettable layer.

After formation, the solder bump can be reflowed. The step of reflowing the solder bump can generate a reaction between the solder bump and the unexposed portion of the under bump metallurgy layer adjacent the solder bump resulting in an intermetallic region wherein the etchant used to remove the copper portions of the under bump metallurgy layer attacks copper preferentially with respect to the intermetallic region.

Brief Description of the Drawings

Figures 1-6 illustrate cross-sectional views of a microelectronic device with contact pads during various steps of a first method for forming solder bumps according to the present invention.

Figures 7-12 illustrate cross-sectional views of a microelectronic device with contact pads during various steps of a second method for forming solder bumps according to the present invention.

Detailed Description of Preferred Embodiments

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. For clarity, the thickness of layers has been exaggerated. Like numbers refer to like elements throughout.

As shown in Figure 1, a microelectronic device **20** may include a substrate **22**, a plurality of contact pads **24**, and a passivation layer **26**. The substrate **22** may comprise a layer of a semiconducting material such as silicon, gallium arsenide, silicon carbide, diamond, a printed circuit board or multilayer substrate, or other substrate materials known to those having skill in the art. The contact pads **24** may comprise aluminum, copper, titanium, an intermetallic including combinations of the aforementioned metals such as AlCu and $AlTi_x$, or other materials known to those having skill in the art. The passivation layer **26** is preferably a polyimide layer but can alternately be a silicon dioxide layer, a silicon nitride layer, or layers of other passivation materials known to those having skill in the art. As shown, the passivation layer preferably covers top edge portions of each of the contact pads opposite the substrate, leaving the central surface portion of each of the contact pads **24** exposed.

It may be desired to provide solder bumps on the microelectronic device **20** so that the device can be connected, electrically and mechanically, to another microelectronic device such as a circuit board or other

next level packaging substrate. The contact pads are first pretreated to remove any native oxide as will be understood by those having skill in the art. A continuous titanium barrier layer **28** (about 500 Ångstroms thick) is formed across the passivation layer **26** and the exposed surface portions of the contact pads **24**. The titanium barrier layer **28** can be readily etched away from the passivation layer **26** without significantly etching the passivation layer. If titanium contact pads are used, the pretreatment step can be eliminated because the titanium barrier layer will getter oxygen out of a titanium contact pad.

A continuous under bump metallurgy layer is then formed on the titanium barrier layer **28**. The under bump metallurgy layer is formed from materials which provide adequate adhesion between a solder bump and a contact pad, and which can be selectively etched away from the titanium barrier layer **28** without significantly etching the titanium barrier layer. Accordingly, the under bump metallurgy layer preferably comprises a chromium layer **30** (about 1000 Ångstroms thick), a phased layer **32** of chromium and copper (about 1000 Ångstroms thick) on the chromium layer, and a copper layer **34** (about 1 micron thick) on the phased layer. Under bump metallurgy layers including a chromium layer, a phased layer of chromium and copper, and a copper layer are discussed, for example, in U.S. Patent No. 5,162,257 entitled "Solder Bump Fabrication Method" to Yung, the disclosure of which is hereby incorporated herein in its entirety by reference.

After forming the under bump metallurgy layer, a solder dam is provided. In a preferred embodiment, the solder dam includes a solder non-wettable layer **36** (about 1500 Ångstroms thick) which is preferably a layer of chromium or titanium. The solder dam may also include a solder wettable layer **38** (about 125 Ångstroms thick), such as a copper layer, on the

solder non-wettable layer 36. For example, a solder dam with a copper layer on a chromium layer allows solder to be plated thereon, while a later reflow step will dissolve the copper exposing the chromium. In this embodiment, solder can be uniformly electroplated on the solder wettable layer 38 of the solder dam. The portions of the solder wettable layer not covered by solder are then removed, thereby preventing the solder bump from expanding during the reflow step. When the solder is heated above its liquidous temperature (approximately 312°C for solder having 95% lead and 5% tin) the solder will reflow, dissolving the remaining portions of the wettable layer 38, and come into contact with the solder non-wettable layer 36. Accordingly, the reflowed solder bump will form a substantially spherical shape due to surface tension. Figure 2 shows the microelectronic device 20 with the titanium barrier layer 28; the under bump metallurgy layer having a chromium layer 30, a phased layer 32 of chromium and copper, and a copper layer 34; and the solder dam having a solder non-wettable layer 36 and a solder wettable layer 38. Each of the layers of titanium, chromium, phased chromium and copper, and copper may be formed by evaporation, sputtering, or other deposition techniques known to those having skill in the art. The phased layer of chromium and copper may be formed by co-depositing chromium and copper.

The solder dam is selectively removed, as shown in Figure 3, in areas over the contact pads 24 where solder bumps are desired. Portions of the solder dam may be selectively removed by standard photolithography/etch techniques or by a lift-off technique. If standard photolithography/etch techniques are used, titanium is preferably used for the solder non-wettable layer 36 because titanium can be selectively etched from the underlying copper layer 34 without significantly etching the copper layer. The

areas of the copper layer 34 left uncovered by the solder dam (layers 36 and 38) define the surface area of the solder bumps on the microelectronic device after the reflow step, as discussed below.

A patterned mask layer 40, such as a photoresist mask, is also formed on the solder dam to define uncovered areas over the solder dam and under bump metallurgy layer on which solder is to be electroplated. The surface areas left uncovered by the mask layer 40 can be larger than the respective surface areas left uncovered by the solder dam (layers 36 and 38) to allow the plating of solder over larger areas, as shown in Figures 3 and 4. The solder bump 42 is electroplated on the areas left uncovered by the mask layer 40, as shown in Figure 4.

The solder is plated on the uncovered portions of the solder dam and under bump metallurgy layer using electroplating techniques known to those having skill in the art. For example, the surface of the microelectronic device 20 with the mask layer 40 is exposed to a plating solution containing lead and tin, and an electrical bias is applied to the continuous under bump metallurgy layer including the chromium layer 30, the phased layer 32 of chromium and copper, and the copper layer 34. The electrical bias causes lead-tin solder to plate on the uncovered portions of the copper layers 34 and 38 forming solder bumps 42, as shown in Figure 4.

The volume of solder plated can be controlled by controlling the area left uncovered by the mask layer 42, the electrical bias applied, the concentration of the plating solution, and the duration of the plating step. Because solder may not uniformly plate on a solder non-wettable material such as chromium, the use of a solder dam with a solder wettable layer 38, such as a copper layer, over the solder non-wettable layer 36 allows the solder to be

uniformly plated over the solder dam in areas not covered by the mask layer. Accordingly, the area over which solder is to be plated, and the resulting volume plated, can be determined independently of the area left uncovered by the solder dam, which determines the surface area of the solder bump on the microelectronic device after reflow.

After completing the plating step, the mask layer **40** and the portions of the solder wettable layer **38** not covered by the solder bumps are removed, and the solder bumps **42** are heated above the liquidous temperature (approximately 312°C for solder having 95% lead and 5% tin) so that they reflow, as shown in Figure 5. If the solder wettable layer is a copper layer, a mixture of ammonium hydroxide and hydrogen peroxide can be used to remove the solder wettable layer. Where a solder bump was electroplated over the solder wettable layer **38** of the solder dam, the solder wettable layer **38** dissolves into the solder bump exposing the solder non-wettable layer **36** of the solder dam to the solder bump. Accordingly, surface tension causes the reflowed solder bumps **42** to form a substantially spherical shape on the portion of the under bump metallurgy layer not covered by the solder dam. When the solder bumps cool, the solder solidifies maintaining the substantially spherical shape.

In addition, the reflowed solder forms an intermetallic region **34'** with a portion of the under bump metallurgy layer adjacent the solder bump. In the preferred embodiment, the under bump metallurgy layer includes a chromium layer **30**, a phased layer **32** of chromium and copper, and a copper layer **34**; and the solder reacts with a portion of the copper layer **34** to form intermetallic region **34'**. This intermetallic region may include Cu_3Sn which does not significantly react with etchants commonly used to remove copper, chromium, and titanium.

As shown in Figure 5, the reflowed solder bumps **42** define exposed and unexposed portions of the under bump metallurgy layer. Accordingly, the solder bumps **42** can be used to mask portions of the under bump metallurgy layer which will be used to support the solder bumps. The portions of the under bump metallurgy layer left exposed by the solder bumps will be removed so that each solder bump **42** will be electrically isolated from each of the other solder bumps, as shown in Figure 6.

It may first be necessary to remove the solder non-wettable layer **36**. If the non-wettable layer is chromium, hydrochloric acid can be used to remove the non-wettable layer. Alternately, if titanium is used for the non-wettable layer, hydrofluoric acid buffered with ammonium fluoride can be used.

The portions of the under bump metallurgy layer left exposed by the solder bumps **42** can be efficiently removed from the titanium barrier layer **28** while the titanium barrier layer protects the underlying passivation layer **26** and contact pad **24**. The exposed portion of titanium barrier layer can then be removed using etchants which do not significantly affect the underlying passivation layer.

For example, a chemical etchant such as a mixture of ammonium hydroxide and hydrogen peroxide can be used to etch the copper layer **34** which is left exposed by the solder bumps **42**. This mixture preferentially attacks the copper layer with respect to the solder bumps, the titanium barrier layer **28**, and the intermetallic region **34'**. Accordingly, this etch will not significantly reduce the solder volume of the solder bumps or significantly undercut the solder bumps. This mixture will also remove some of the copper from the phased layer **32** of chromium and copper.

A chemical etchant such as hydrochloric acid

can be used to etch the remaining portion of the phased layer 32 and the chromium layer 30 which have been left exposed by the solder bumps. This acid preferentially attacks the phased layer and the chromium layer with respect to the solder bump, the titanium barrier layer, and the intermetallic region 34'. This acid will remove the remaining exposed portions of the under bump metallurgy layer from the titanium barrier layer without leaving significant residues.

A titanium etchant such as hydrofluoric acid buffered with ammonium fluoride can be used to etch the portion of the titanium barrier layer 28 left exposed by the solder bumps 42. This acid preferentially attacks the titanium with respect to the solder bump 42, the intermetallic region 34', the phased layer 32 of chromium and copper, and the chromium layer 30. If a polyamide layer is used as the passivation layer 26, this acid will not significantly attack the passivation layer. If silicon dioxide or silicon nitride is used for the passivation layer, this acid may attack the passivation layer to some degree. The etching of these materials can be minimized by limiting the duration of the etch to the time required to remove the titanium barrier layer. Accordingly, polyimide is the preferred material for the passivation layer. The final solder bump structure is shown in Figure 6.

Without the titanium barrier layer, the under bump metallurgy layer may be difficult to completely remove after the reflow step and undesired conductive residues may be left on the microelectronic device. Applicants theorize that the under bump metallurgy layer reacts with the passivation layer forming a conductive reactant at the interface between the two layers. This conductive reactant may be difficult to etch without undercutting the solder bump or reducing the volume of the solder bump thereby resulting in the

undesired conductive residues. These residues may result in electrical shorts between solder bumps.

The use of the titanium barrier layer allows the under bump metallurgy layer to be efficiently removed after the reflow step while reducing the incidence of residues which could form electrical shorts between solder bumps. The titanium barrier layer prevents the under bump metallurgy layer from reacting with the passivation layer thereby reducing residues. The titanium barrier layer can then be etched away from the passivation layer without leaving any significant residue.

The elimination of the undesired residues typically results in a reduction in the time required to remove the conductive layers between solder bumps despite the fact that an additional layer has been added to the structure. Because the titanium layer reduces the overall etch time thereby reducing the time that the solder bump is exposed to the etchants, the potential for under cutting is reduced. The addition of the titanium barrier layer may also increase production yields and reduce the possibility of device failures. Solder bumps formed according to the method described above also have a low electrical resistance. For example, a solder bump with a circular surface with a 50 μm diameter on a microelectronic device has demonstrated an electrical resistance of approximately 3 milliohms.

A variation of the method discussed above with regard to Figures 1-6 is shown in Figures 7-12. Figure 7 shows a microelectronic device **20** with a substrate **22**, contact pads **24**, and passivation layer **26** as discussed above with regard to Figure 1. Figure 8 shows the addition of a titanium barrier layer **28**, and an under bump metallurgy layer including a chromium layer **30**, a phased layer **32** of chromium and copper, and a copper layer **34**, as discussed above with regard to

Figure 2. In Figure 8, however, the solder dam **50** has only a single solder non-wettable layer, which is preferably a titanium layer (about 1000 Ångstroms thick).

The use of a titanium solder dam layer allows the implementation of a single mask method during solder bump formation as shown in Figure 9. Here, the mask layer **52**, such as a photoresist mask or other mask known to those having skill in the art, is patterned prior to patterning the solder dam **50**. The mask layer **52** is then used to pattern the solder dam **50**. Accordingly, only one photolithography step is required to pattern both the mask layer and the solder dam. A titanium layer is preferably used for the solder dam because it can be selectively removed from the copper layer **34** using an etchant such as hydrofluoric acid buffered with ammonium fluoride which preferentially attacks titanium with respect to copper and solder. The solder dam **50** does not require a solder wettable layer because solder is not plated on the solder dam. Here, the solder dam **50** only prevents the solder bump **54** from spreading during the reflow step.

The mask layer **52** and the solder dam **50** define an area on the under bump metallurgy layer on which solder will be plated, as shown in Figure 10. The plating step is the same as that discussed above with regard to Figure 4 except that the solder is not plated over portions of the solder dam. After plating the solder bumps, the mask layer **40** is selectively removed, and the solder bumps are heated above the liquidous temperature (about 312°C for solder having 95% led and 5% tin) to reflow the solder. The solder dam **50** prevents the reflowed solder from flowing beyond the desired areas. Surface tension causes the reflowed solder bumps **54** to form a substantially spherical shape as shown in Figure 11. When the solder bumps cool, they solidify and maintain this shape. The reflow step

may also be used to form an intermetallic region 34' in the copper layer 34 as discussed above with regard to Figure 5.

As discussed above with regard to Figures 5 and 6, the solder bumps define exposed and unexposed portions of the under bump metallurgy layer and titanium barrier layer, and the exposed portions are removed so that each solder bump is electrically isolated as shown in Figure 12. The solder dam 50 is first removed using an etchant such as hydrofluoric acid buffered with ammonium fluoride. The under bump metallurgy layer and titanium barrier layer are then removed as discussed above with regard to Figures 5 and 6.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for the purpose of limitation, the scope of the invention being set forth in the following claims.

THAT WHICH IS CLAIMED:

1. A method for forming solder bumps on a microelectronic device having a substrate and a contact pad on said substrate, wherein said contact pad has an exposed surface portion, said method comprising the steps of:

forming a titanium barrier layer on said contact pad, wherein said barrier layer covers said exposed surface portion of said contact pad and extends over said substrate;

forming an under bump metallurgy layer on said barrier layer opposite said substrate;

forming a solder bump on said under bump metallurgy layer opposite said exposed surface portion of said contact pad and said barrier layer thereby defining exposed and unexposed surface portions of said under bump metallurgy layer;

selectively removing said exposed portion of said under bump metallurgy layer thereby defining an exposed portion of said barrier layer; and

selectively removing said exposed portion of said barrier layer.

2. A method according to Claim 1 wherein said contact pad comprises a titanium contact pad.

3. A method according to Claim 1 wherein said step of selectively removing said exposed portion of said under bump metallurgy layer comprises the step of applying a chemical etchant to said under bump metallurgy layer wherein said chemical etchant attacks said under bump metallurgy layer preferentially with respect to said barrier layer and said solder bump.

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4. A method according to Claim 1 wherein said step of selectively removing said exposed portion of said titanium barrier layer comprises the step of applying a titanium etchant to said barrier layer wherein said titanium etchant attacks said barrier layer preferentially with respect to said solder bump and said under bump metallurgy layer.

5. A method according to Claim 1 wherein said step of forming an under bump metallurgy layer comprises the steps of:

forming a chromium layer on said barrier layer;

forming a phased layer of chromium and copper on said chromium layer opposite said barrier layer; and

forming a copper layer on said phased layer opposite said chromium layer.

6. A method according to Claim 5 wherein said step of selectively removing said exposed portion of said under bump metallurgy layer further comprises the steps of:

applying a copper etchant to said exposed portion of said copper layer wherein said copper etchant selectively attacks said copper layer and said copper portion of said phased layer preferentially with respect to said solder bump, said chromium layer, and said titanium barrier layer; and

applying a chromium etchant to said chromium portion of said phased layer and said chromium layer wherein said chromium etchant selectively attacks said chromium portion of said phased layer and said chromium layer preferentially with respect to said solder bump, said copper layer, and said titanium barrier layer.

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7. A method according to Claim 1 wherein said step of forming a solder bump is preceded by the step of forming a solder dam layer including a solder non-wettable layer on said exposed portions of said under bump metallurgy layer, and wherein said step of selectively removing said exposed portion of said under bump metallurgy layer is preceded by the step of removing said solder dam layer.

8. A method according to Claim 7 wherein said step of forming a solder dam layer comprises the step of forming a solder non-wettable layer selected from the group consisting of a titanium layer and a chromium layer.

9. A method according to Claim 7 wherein said step of forming a solder dam layer further comprises the step of forming a solder wettable layer on said solder non-wettable layer opposite said under bump metallurgy layer.

10. A method according to Claim 7 wherein said step of forming a solder bump comprises the steps of:

forming a patterned mask layer on said solder dam layer;

electroplating solder on said unexposed portion of said under bump metallurgy layer; and

selectively removing said patterned mask layer.

11. A method according to Claim 1 wherein said step of forming a solder bump is followed by the step of reflowing said solder bump.

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12. A method according to Claim 11 wherein said step of reflowing said solder bump results in a reaction between said solder bump and said unexposed portion of said under bump metallurgy layer to form an intermetallic region.

13. A method for forming solder bumps on a microelectronic device having a substrate and a contact pad on said substrate, wherein said contact pad has an exposed surface portion, said method comprising the steps of:

forming an under bump metallurgy layer on said contact pad, wherein said under bump metallurgy layer covers said exposed surface portion of said contact pad and extends over said substrate;

forming a solder dam on portions of said under bump metallurgy layer, said solder dam defining an uncovered portion of said under bump metallurgy layer opposite said exposed surface portion of said contact pad, said solder dam comprising a solder non-wettable layer on said under bump metallurgy layer and a solder wettable layer on said solder non-wettable layer opposite said under bump metallurgy layer; and

forming a solder bump on said uncovered portion of said under bump metallurgy layer opposite said exposed surface portion of said contact pad thereby defining exposed and unexposed surface portions of said under bump metallurgy layer, said solder bump extending onto a portion of said solder dam thereby defining exposed and unexposed portions of said wettable layer.

14. A method according to Claim 13 further comprising the steps of:

selectively removing said exposed portion of said solder wettable layer; and

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reflowing said solder bump thereby dissolving said unexposed portion of said solder wettable layer into said solder bump, said reflowed solder bump including said dissolved solder wettable layer and forming a solder ball on said unexposed portion of said under bump metallurgy layer.

15. A method according to Claim 14 wherein said reflowing step results in a reaction between said solder bump and said exposed portion of said under bump metallurgy thereby forming an intermetallic region.

16. A method according to Claim 13 wherein said solder wettable layer comprises copper.

17. A method according to Claim 13 wherein said solder non-wettable layer comprises chromium.

18. A method according to Claim 13 wherein said contact pad comprises a titanium contact pad.

19. A method according to Claim 13 wherein the step of forming an under bump metallurgy layer is preceded by the step of forming a titanium barrier layer on said contact pad, wherein said titanium barrier layer covers said exposed surface portion of said contact pad and extends over said substrate.

20. A method according to Claim 19 further comprising the steps of:

selectively removing said exposed portion of said solder dam and said under bump metallurgy layer thereby defining an exposed portion of said barrier layer; and

selectively removing said exposed portion of said barrier layer.

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21. A method according to Claim 20 wherein said step of selectively removing said exposed portion of said under bump metallurgy layer comprises the step of applying a chemical etchant to said under bump metallurgy layer wherein said chemical etchant attacks said under bump metallurgy layer preferentially with respect to said barrier layer and said solder bump.

22. A method according to Claim 20 wherein said step of selectively removing said exposed portion of said titanium barrier layer comprises the step of applying a titanium etchant to said barrier layer wherein said titanium etchant attacks said barrier layer preferentially with respect to said solder bump and said under bump metallurgy layer.

23. A method according to Claim 13 wherein said step of forming an under bump metallurgy layer comprises the steps of:

forming a chromium layer on said barrier layer;

forming a phased layer of chromium and copper on said chromium layer opposite said barrier layer; and

forming a copper layer on said phased layer opposite said chromium layer.

24. A method according to Claim 13 wherein said step of forming a solder bump comprises the steps of:

forming a patterned mask layer on said solder dam layer;

electroplating solder on said unexposed portion of said under bump metallurgy layer; and

selectively removing said patterned mask layer.

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25. A solder bump structure for a microelectronic device comprising:

a substrate;

a plurality of contact pads on said substrate, each of said contact pads having an exposed surface portion opposite said substrate;

a continuous titanium barrier layer extending across said substrate and contacting each of said exposed surface portions of each of said contact pads;

a continuous under bump metallurgy layer on said barrier layer opposite said substrate; and

a solder bump on said under bump metallurgy layer opposite one of said contact pads.

26. A solder bump structure according to Claim 25 wherein said continuous under bump metallurgy layer comprises:

a chromium layer on said barrier layer;

a phased layer of chromium and copper on said chromium layer opposite said barrier layer; and

a copper layer on said phased layer opposite said chromium layer.

27. A solder bump structure according to Claim 25 wherein said plurality of contact pads comprise a plurality of titanium contact pads.

28. A solder bump structure according to Claim 25 wherein said solder bump defines an exposed portion of said under bump metallurgy layer and further comprising a solder dam layer on said exposed portion of said under bump metallurgy layer opposite said barrier layer.

29. A solder bump structure according to Claim 28 wherein said solder dam layer comprises a solder non-wettable layer.

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30. A solder bump structure according to Claim 29 wherein said solder non-wettable layer is selected from the group consisting of a titanium layer and a chromium layer.

31. A solder bump structure according to Claim 29 wherein said solder dam further comprises a solder wettable layer on said solder non-wettable layer opposite said under bump metallurgy layer.

32. A solder bump structure for a microelectronic device comprising:

a substrate;

a plurality of contact pads on said substrate, each of said contact pads having an exposed surface portion opposite said substrate;

a continuous under bump metallurgy layer on said contact pad and extending across said substrate;

a solder dam on portions of said under bump metallurgy layer, said solder dam defining uncovered portions of said under bump metallurgy layer opposite said exposed surface portions of said contact pads, said solder dam comprising a solder non-wettable layer on said under bump metallurgy layer and a solder wettable layer on said solder non-wettable layer opposite said under bump metallurgy layer; and

a solder bump on one of said uncovered portions of said under bump metallurgy layer opposite an exposed surface portion of a respective contact pad thereby defining exposed and unexposed surface portions of said under bump metallurgy layer, said solder bump extending onto a portion of said solder dam thereby defining exposed and unexposed portions of said wettable layer.

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33. A solder bump structure according to Claim 32 further comprising a continuous titanium barrier layer between said substrate and said under bump metallurgy layer, said titanium layer extending across said substrate and contacting each of said exposed surface portions of each of said contact pads.

34. A solder bump structure according to Claim 32 wherein said continuous under bump metallurgy layer comprises:

a chromium layer on said barrier layer;

a phased layer of chromium and copper on said chromium layer opposite said barrier layer; and

a copper layer on said phased layer opposite said chromium layer.

35. A solder bump structure according to Claim 32 wherein said plurality of contact pads comprise a plurality of titanium contact pads.

36. A solder bump structure according to Claim 32 wherein said solder non-wettable layer comprises chromium.

37. A solder bump structure according to Claim 32 wherein said solder wettable layer comprises copper.

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FIG. 1

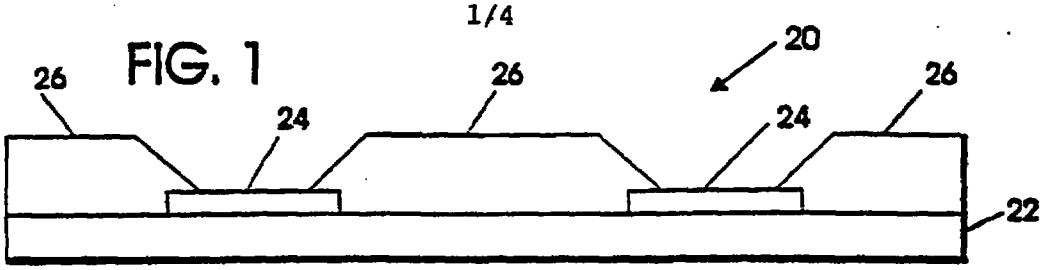


FIG. 2

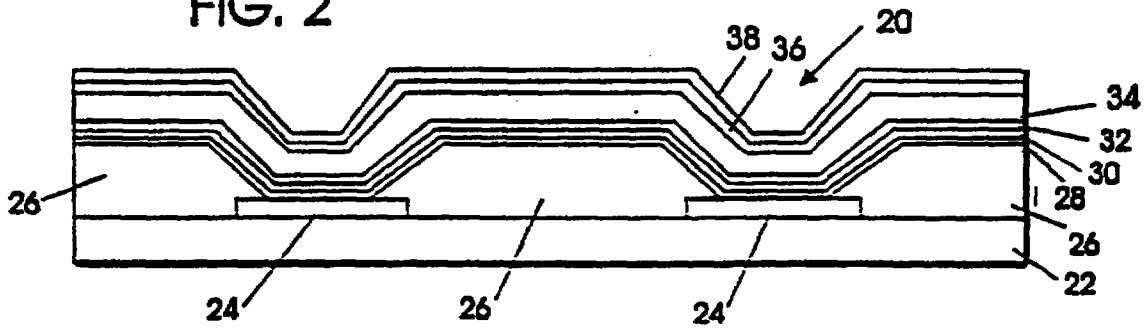


FIG. 3

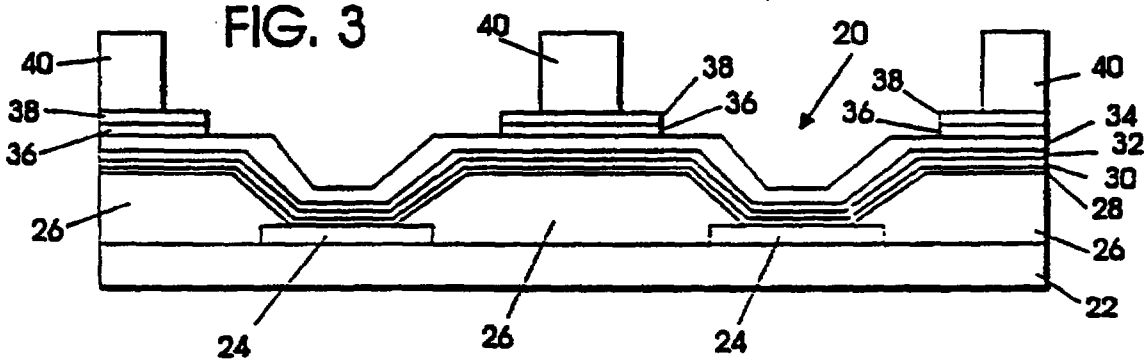


FIG. 4

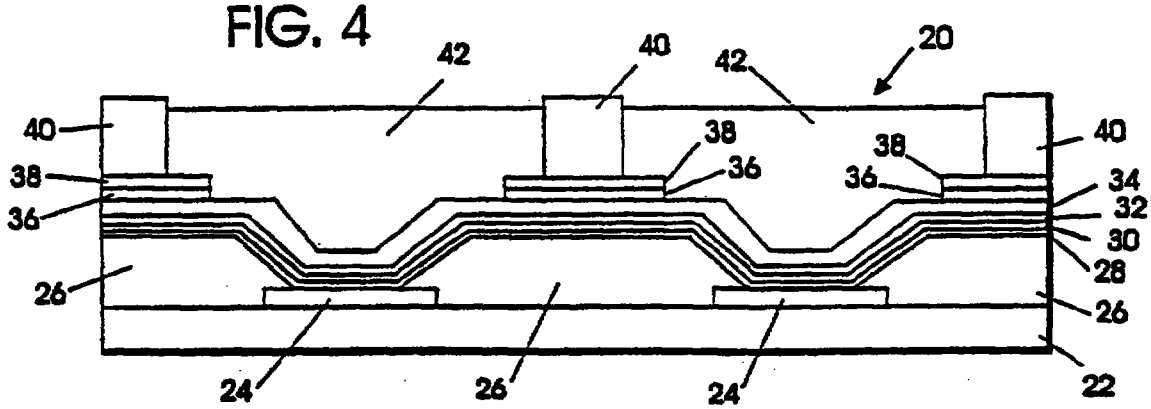


FIG. 5

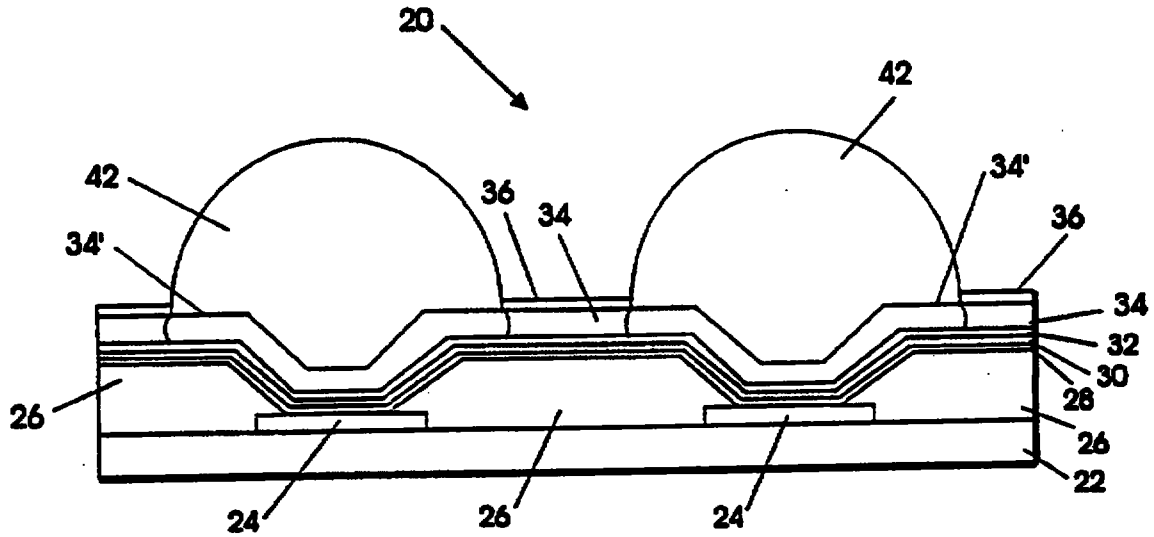

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FIG. 6

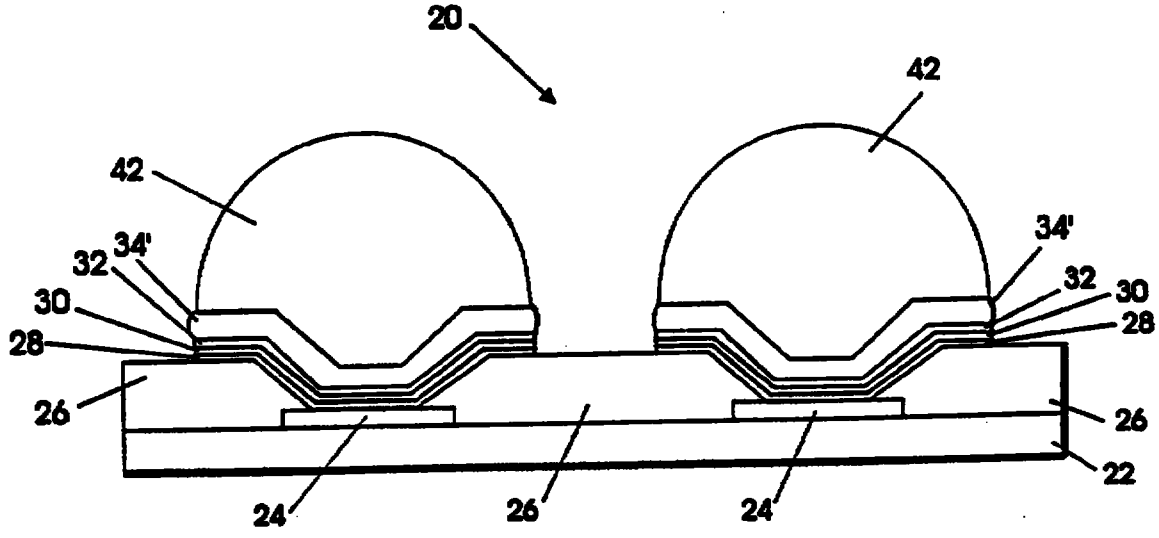

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FIG. 7

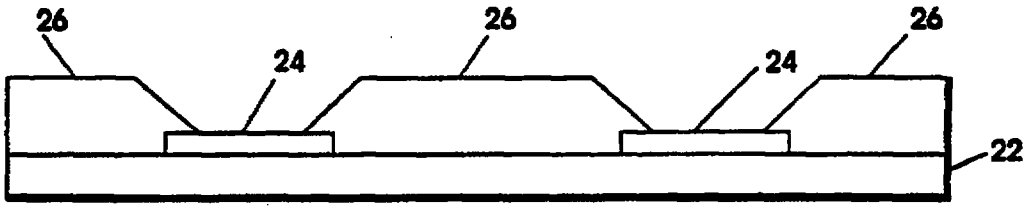


FIG. 8

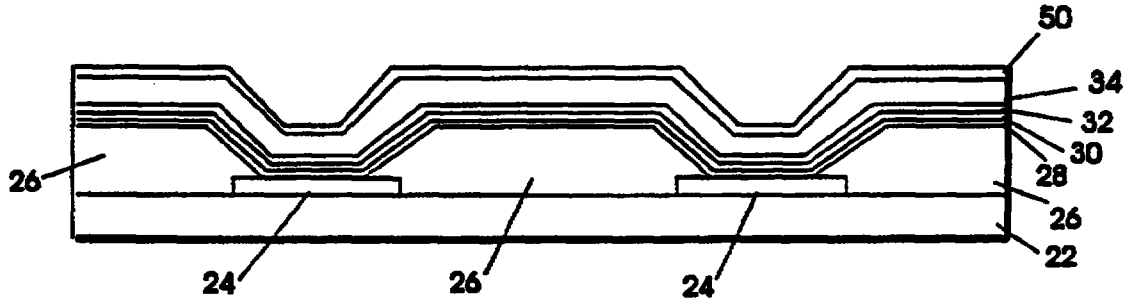


FIG. 9

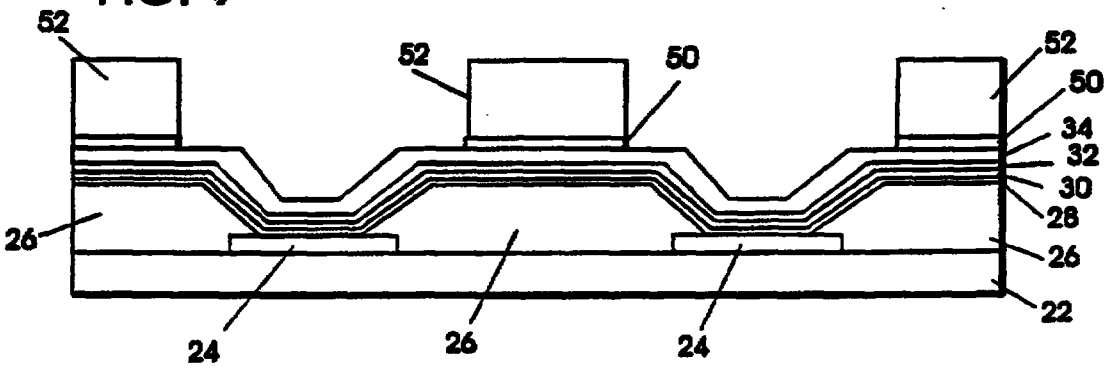


FIG. 10

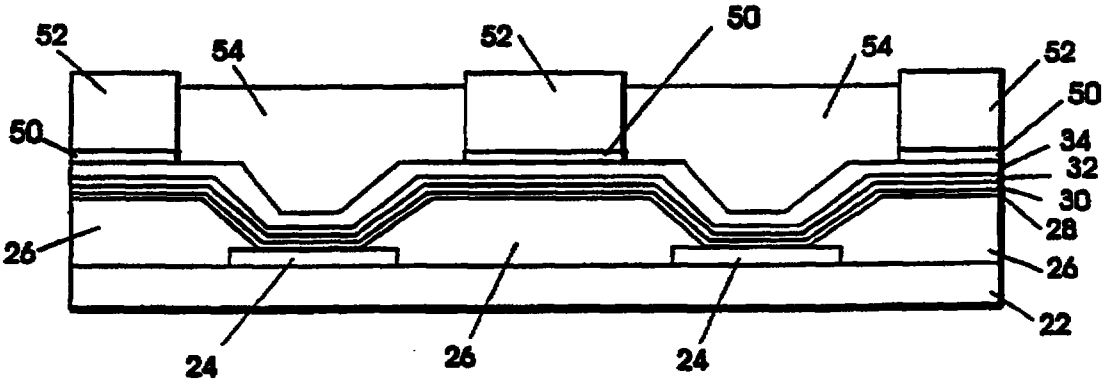


FIG. 11

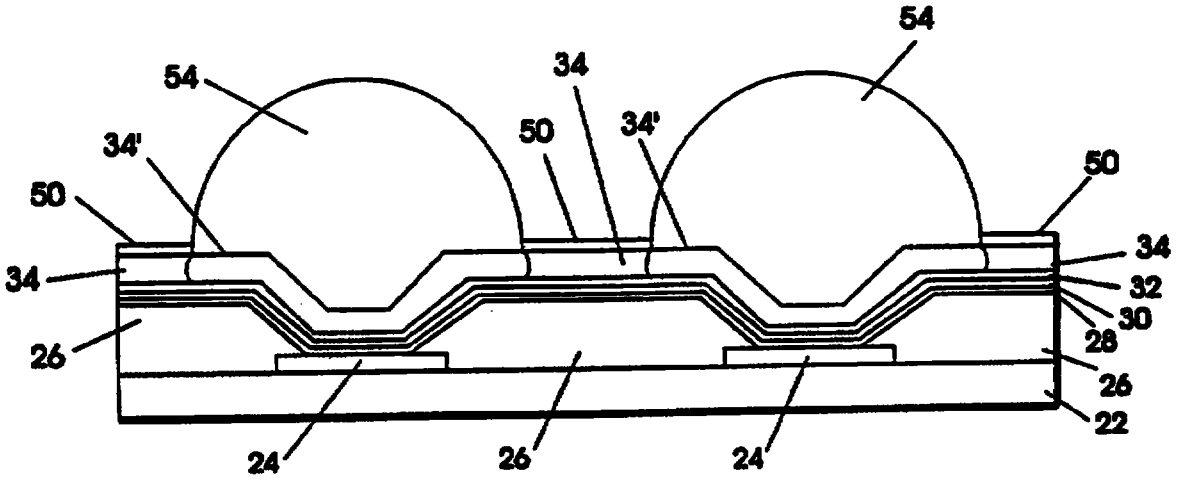
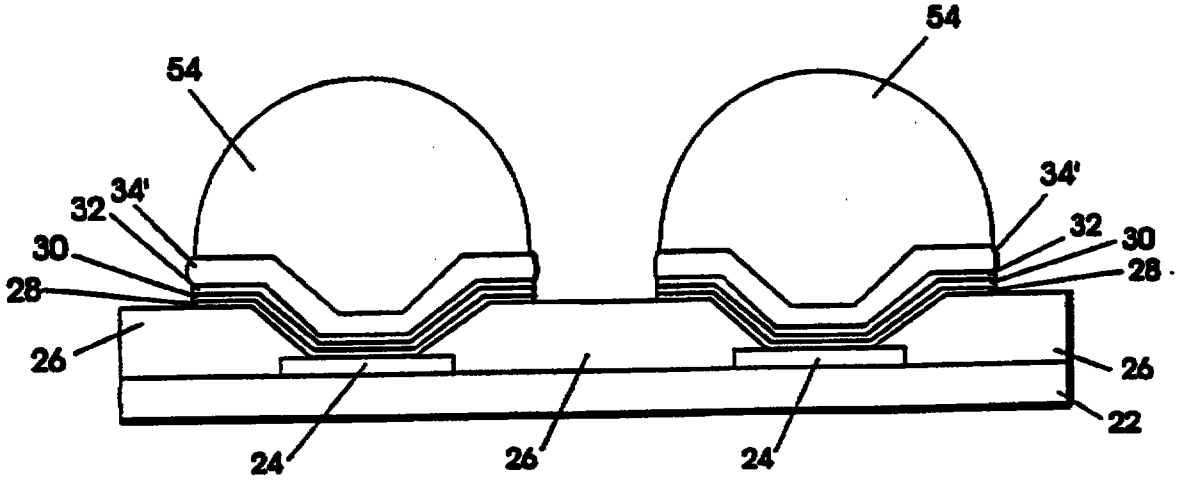

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FIG. 12


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* C L M S *

THAT WHICH IS CLAIMED:

1. A method for forming solder bumps (42) on a microelectronic device (20) having a substrate (22) and a plurality of contact pads (24) on said substrate (22), wherein each of said contact pads (24) has an exposed surface portion, said method characterized by the steps of:

forming a continuous titanium barrier layer (28) on said contact pads (24), wherein said barrier layer (28) covers said exposed surface portions of said contact pads (24) and extends over said substrate;

forming an under bump metallurgy layer (30, 32, 34) on said barrier layer (28) opposite said substrate;

forming a solder bump (42) on said under bump metallurgy layer (30, 32, 34) opposite said exposed surface portion of one of said contact pads (24) and said barrier layer thereby defining exposed and unexposed surface portions of said under bump metallurgy layer;

selectively removing said exposed portion of said under bump metallurgy layer (30, 32, 34) thereby defining an exposed portion of said barrier layer (28); and

selectively removing said exposed portion of said barrier layer (28).

2. A method according to Claim 1 wherein said contact pads (24) comprise titanium contact pads.

3. A method according to Claim 1 wherein said step of selectively removing said exposed portion of said under bump metallurgy layer (30, 32, 34) comprises the step of applying a chemical etchant to said under bump metallurgy layer (30, 32, 34) wherein said chemical etchant attacks said under bump metallurgy layer preferentially with respect to said barrier layer (28) and said solder bump (42).

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4. A method according to Claim 1 wherein said step of selectively removing said exposed portion of said titanium barrier layer (28) comprises the step of applying a titanium etchant to said barrier layer (30, 32, 34) wherein said titanium etchant attacks said barrier layer (30, 32, 34) preferentially with respect to said solder bump (42) and said under bump metallurgy layer.

5. A method according to Claim 1 wherein said step of forming an under bump metallurgy layer (30, 32, 34) comprises the steps of:

forming a chromium layer (30) on said barrier layer (28);

forming a phased layer (32) of chromium and copper on said chromium layer opposite said barrier layer (28); and

forming a copper layer (34) on said phased layer (32) opposite said chromium layer (30).

6. A method according to Claim 5 wherein said step of selectively removing said exposed portion of said under bump metallurgy layer (30, 32, 34) further comprises the steps of:

applying a copper etchant to said exposed portion of said copper layer (34) wherein said copper etchant selectively attacks said copper layer (34) and said copper portion of said phased layer (32) preferentially with respect to said solder bump (42), said chromium layer (30), and said titanium barrier layer (28); and

applying a chromium etchant to said chromium portion of said phased layer (32) and said chromium layer (30) wherein said chromium etchant selectively attacks said chromium portion of said phased layer (32) and said chromium layer (30) preferentially with respect to said solder bump (42), said copper layer (34), and said titanium barrier layer (28).

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7. A method according to Claim 1 wherein said step of forming a solder bump (42) is preceded by the step of forming a solder dam layer including a solder non-wettable layer (36) on said exposed portions of said under bump metallurgy layer, and wherein said step of selectively removing said exposed portion of said under bump metallurgy layer is preceded by the step of removing said solder dam layer.

8. A method according to Claim 7 wherein said step of forming a solder dam layer comprises the step of forming a solder non-wettable layer (36) selected from the group consisting of a titanium layer and a chromium layer.

9. A method according to Claim 7 wherein said step of forming a solder dam layer further comprises the step of forming a solder wettable layer (38) on said solder non-wettable layer (36) opposite said under bump metallurgy layer.

10. A method according to Claim 7 wherein said step of forming a solder bump (42) comprises the steps of:

forming a patterned mask layer (40) on said solder dam layer;

electroplating solder on said unexposed portion of said under bump metallurgy layer (30, 32, 34); and

selectively removing said patterned mask layer (40).

11. A method according to Claim 1 wherein said step of forming a solder bump (42) is followed by the step of reflowing said solder bump (42).

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12. A method according to Claim 11 wherein said step of reflowing said solder bump (42) results in a reaction between said solder bump (42) and said unexposed portion of said under bump metallurgy layer to form an intermetallic region (34').

13. A solder bump structure for a microelectronic device (20) comprising a substrate (22) and a plurality of contact pads (24) on said substrate, each of said contact pads (24) having an exposed surface portion opposite said substrate, said solder bump structure characterized by:

a continuous titanium barrier layer (28) extending across said substrate and contacting each of said exposed surface portions of each of said contact pads (24);

a continuous under bump metallurgy layer (30, 32, 34) on said barrier layer (28) opposite said substrate; and

a solder bump (42) on said under bump metallurgy layer (30, 32, 34) opposite one of said contact pads (24).

14. A solder bump structure according to Claim 13 wherein said continuous under bump metallurgy layer comprises:

a chromium layer (30) on said barrier layer (24);

a phased layer (32) of chromium and copper on said chromium layer (30) opposite said barrier layer (28); and

a copper layer (34) on said phased layer (32) opposite said chromium layer (30).

15. A solder bump structure according to Claim 13 wherein said plurality of contact pads (24) comprise a plurality of titanium contact pads.

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16. A solder bump structure according to Claim 13 wherein said solder bump (42) defines an exposed portion of said under bump metallurgy layer (30, 32, 34) and further comprising a solder dam layer (36) on said exposed portion of said under bump metallurgy layer (30, 32, 34) opposite said barrier layer (28).

17. A solder bump structure according to Claim 16 wherein said solder dam layer comprises a solder non-wettable layer (36).

18. A solder bump structure according to Claim 17 wherein said solder non-wettable layer (36) is selected from the group consisting of a titanium layer and a chromium layer.

19. A solder bump structure according to Claim 17 wherein said solder dam further comprises a solder wettable layer (38) on said solder non-wettable layer (36) opposite said under bump metallurgy layer.

20. A method according to Claim 1 wherein said step of forming an under bump metallurgy layer comprises the steps of:

forming a chromium layer (30) on said titanium barrier layer (28); and

forming a copper layer (34) on said chromium layer (30) opposite said barrier layer (28).

21. A solder bump structure according to Claim 13 wherein said continuous under bump metallurgy layer comprises:

a chromium layer (30) on said titanium barrier layer (28); and

a copper layer (34) on said chromium layer (30) opposite said barrier layer (28).

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REPLACEMENT SHEETS SG
Description : paged — to paged —
Claim(s) : paged 16 to paged 21
Drawing(s) : paged — to paged —
Abstract : paged — to paged —
DATE OF RECEIPT 21/9/98

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REPLACEMENT SHEET
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THAT WHICH IS CLAIMED:

* C L M S *

1. A method for forming solder bumps (42) on a microelectronic device (20) having a substrate (22) and a plurality of contact pads (24) on said substrate (22), wherein each of said contact pads (24) has an exposed surface portion, said method characterized by the steps of:

forming a continuous titanium barrier layer (28) on said contact pads (24), wherein said barrier layer (28) covers said exposed surface portions of said contact pads (24) and extends over said substrate;

forming an under bump metallurgy layer (30, 32, 34) on said barrier layer (28) opposite said substrate;

forming a solder bump (42) on said under bump metallurgy layer (30, 32, 34) opposite said exposed surface portion of one of said contact pads (24) and said barrier layer thereby defining exposed and unexposed surface portions of said under bump metallurgy layer;

selectively removing said exposed portion of said under bump metallurgy layer (30, 32, 34) thereby defining an exposed portion of said barrier layer (28);

selectively removing said exposed portion of said barrier layer (28); and

wherein said step of forming an under bump metallurgy layer (30, 32, 34) comprises the steps of:

forming a chromium layer (30) on said barrier layer (28),

forming a phased layer (32) of chromium and copper on said chromium layer opposite said barrier layer (28), and

forming a copper layer (34) on said phased layer (32) opposite said chromium layer (30).

2. A method according to Claim 1 wherein said step of selectively removing said exposed portion

REPLACEMENT SHEET
21 SEP 1998

of said under bump metallurgy layer (30, 32, 34) further comprises the steps of:

applying a copper etchant to said exposed portion of said copper layer (34) wherein said copper etchant selectively attacks said copper layer (34) and said copper portion of said phased layer (32) preferentially with respect to said solder bump (42), said chromium layer (30), and said titanium barrier layer (28); and

applying a chromium etchant to said chromium portion of said phased layer (32) and said chromium layer (30) wherein said chromium etchant selectively attacks said chromium portion of said phased layer (32) and said chromium layer (30) preferentially with respect to said solder bump (42), said copper layer (34), and said titanium barrier layer (28).

3. A method for forming solder bumps (42) on a microelectronic device (20) having a substrate (22) and a plurality of contact pads (24) on said substrate (22), wherein each of said contact pads (24) has an exposed surface portion, said method characterized by the steps of:

forming a continuous titanium barrier layer (28) on said contact pads (24), wherein said barrier layer (28) covers said exposed surface portions of said contact pads (24) and extends over said substrate;

forming an under bump metallurgy layer (30, 32, 34) on said barrier layer (28) opposite said substrate;

forming a solder bump (42) on said under bump metallurgy layer (30, 32, 34) opposite said exposed surface portion of one of said contact pads (24) and said barrier layer thereby defining exposed and unexposed surface portions of said under bump metallurgy layer;

selectively removing said exposed portion of said under bump metallurgy layer (30, 32, 34) thereby defining an exposed portion of said barrier layer (28);

REPLACEMENT SHEET

21 SEP 1998

selectively removing said exposed portion of said barrier layer (28);

wherein said step of forming a solder bump (42) is preceded by the step of forming a solder dam layer including a solder non-wettable layer (36) on said exposed portions of said under bump metallurgy layer, and wherein said step of selectively removing said exposed portion of said under bump metallurgy layer is preceded by the step of removing said solder dam layer; and

wherein said step of forming a solder dam layer further comprises the step of forming a solder wettable layer (38) on said solder non-wettable layer (36) opposite said under bump metallurgy layer.

4. A method for forming solder bumps (42) on a microelectronic device (20) having a substrate (22) and a plurality of contact pads (24) on said substrate (22), wherein each of said contact pads (24) has an exposed surface portion, said method characterized by the steps of:

forming a continuous titanium barrier layer (28) on said contact pads (24), wherein said barrier layer (28) covers said exposed surface portions of said contact pads (24) and extends over said substrate;

forming an under bump metallurgy layer (30, 32, 34) on said barrier layer (28) opposite said substrate;

forming a solder bump (42) on said under bump metallurgy layer (30, 32, 34) opposite said exposed surface portion of one of said contact pads (24) and said barrier layer thereby defining exposed and unexposed surface portions of said under bump metallurgy layer;

selectively removing said exposed portion of said under bump metallurgy layer (30, 32, 34) thereby defining an exposed portion of said barrier layer (28);

REPLACEMENT SHEET

21 SEP 1998

selectively removing said exposed portion of said barrier layer (28); and

wherein said step of forming an under bump metallurgy layer comprises the steps of:

forming a chromium layer (30) on said titanium barrier layer (28), and

forming a copper layer (34) on said chromium layer (30) opposite said barrier layer (28).

5. A solder bump structure for a microelectronic device (20) comprising a substrate (22) and a plurality of contact pads (24) on said substrate, each of said contact pads (24) having an exposed surface portion opposite said substrate, said solder bump structure characterized by:

a continuous titanium barrier layer (28) extending across said substrate and contacting each of said exposed surface portions of each of said contact pads (24);

a continuous under bump metallurgy layer (30, 32, 34) on said barrier layer (28) opposite said substrate;

a solder bump (42) on said under bump metallurgy layer (30, 32, 34) opposite one of said contact pads (24); and

wherein said continuous under bump metallurgy layer comprises:

a chromium layer (30) on said barrier layer (24),

a phased layer (32) of chromium and copper on said chromium layer (30) opposite said barrier layer (28), and

a copper layer (34) on said phased layer (32) opposite said chromium layer (30).

6. A solder bump structure for a microelectronic device (20) comprising a substrate (22) and a plurality of contact pads (24) on said substrate, each of said contact pads (24) having an exposed

REPLACEMENT SHEET

21 SEP 1998

surface portion opposite said substrate, said solder bump structure characterized by:

a continuous titanium barrier layer (28) extending across said substrate and contacting each of said exposed surface portions of each of said contact pads (24);

a continuous under bump metallurgy layer (30, 32, 34) on said barrier layer (28) opposite said substrate;

a solder bump (42) on said under bump metallurgy layer (30, 32, 34) opposite one of said contact pads (24);

wherein said solder bump (42) defines an exposed portion of said under bump metallurgy layer (30, 32, 34) and further comprising a solder dam layer (36) on said exposed portion of said under bump metallurgy layer (30, 32, 34) opposite said barrier layer (28);

wherein said solder dam layer comprises a solder non-wettable layer (36); and

REPLACEMENT SHEET
21 SEP 1998

wherein said solder dam further comprises a solder wettable layer (38) on said solder non-wettable layer (36) opposite said under bump metallurgy layer.

7. A solder bump structure according to Claim 6 wherein said solder non-wettable layer (36) is selected from the group consisting of a titanium layer and a chromium layer.

8. A solder bump structure for a microelectronic device (20) comprising a substrate (22) and a plurality of contact pads (24) on said substrate, each of said contact pads (24) having an exposed surface portion opposite said substrate, said solder bump structure characterized by:

a continuous titanium barrier layer (28) extending across said substrate and contacting each of

said exposed surface portions of each of said contact pads (24);

a continuous under bump metallurgy layer (30, 32, 34) on said barrier layer (28) opposite said substrate;

a solder bump (42) on said under bump metallurgy layer (30, 32, 34) opposite one of said contact pads (24); and

wherein said continuous under bump metallurgy layer comprises:

a chromium layer (30) on said titanium barrier layer (28), and

a copper layer (34) on said chromium layer (30) opposite said barrier layer (28).

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International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6: H01L — A2

(11) International Publication Number: WO 96/30933

(43) International Publication Date: 3 October 1996 (03.10.96)

(21) International Application Number: PCT/US96/03697

(22) International Filing Date: 18 March 1996 (18.03.96)

(30) Priority Data:
(1) 08/407,196 — 20 March 1995 (20.03.95) — US

(60) Parent Application or Grant
(63) Related by Continuation
US — 08/407,196 (CON)
Filed on — 20 March 1995 (20.03.95)

(71) Applicant (*for all designated States except US*): (1) MCNC [US/US]; 3021 Cornwallis Road, P.O. Box 12889, Research Triangle Park, NC 27709 (US).

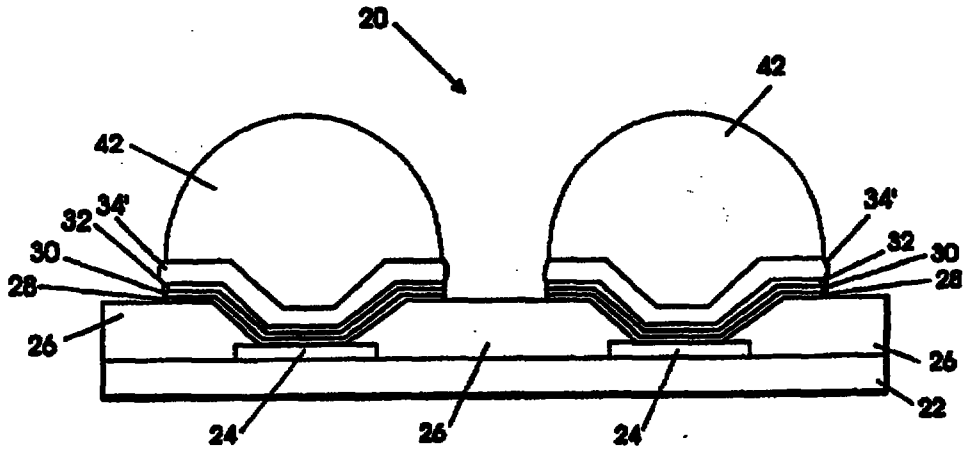
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(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: SOLDER BUMP FABRICATION METHODS AND STRUCTURE INCLUDING A TITANIUM BARRIER LAYER



(57) Abstract

A method for fabricating solder bumps on a microelectronic device having contact pads includes the steps of depositing a titanium barrier layer on the device, forming an under bump metallurgy layer on the titanium barrier layer, and forming one or more solder bumps on the under bump metallurgy layer. The solder bump or bumps define exposed portions of the under bump metallurgy layer which are removed, and then the exposed portion of the titanium barrier layer is removed. The titanium barrier layer protects the underlying microelectronic device from the etchants used to remove the under bump metallurgy layer. The titanium layer also prevents the under bump metallurgy layer from forming a residue on the underlying microelectronic device. Accordingly, the titanium barrier layer allows the under bump metallurgy layer to be quickly removed without leaving residual matter, thereby reducing the possibility of electrical shorts between solder bumps.