CLAIMS

1. An integrated circuit, comprising:

a photodetection region; and

a drain region electrically coupled to the photodetection region; and

an at least partially opaque and at least partially insulative material disposed above or below at least a portion of the photodetection region and having a triangular-shaped opening configured to receive dopants therethrough to induce an intrinsic electric field in a direction from the photodetection region to the drain region.

2. The integrated circuit of claim 1, wherein the photodetection region comprises a dopant configuration that induces the intrinsic electric field.

3. The integrated circuit of claim 2, wherein the dopant configuration generates a potential gradient from the photodetection region to the drain region.

4. The integrated circuit of claim 3, wherein the dopant configuration is triangular-shaped.

5. The integrated circuit of any one of claims 1 to 4, further comprising:

a first charge storage region electrically coupled to the photodetection region,

wherein the photodetection region is configured to receive incident light in a first direction and to transfer charge carriers, generated therein in response to the incident light, to the first charge storage region in a second direction perpendicular to the first direction.

6. The integrated circuit of claim 5, wherein the photodetection region is configured to induce the intrinsic electric field in the second direction.

7. The integrated circuit of claim 6, wherein the opening comprises a first end and a second end spaced from the first end in the second direction, and the opening is wider, in a third direction perpendicular to each of the first and second directions, at the first end than at the second end.

8. The integrated circuit of claim 7, wherein the opening is at least 75% wider, in the third direction, at the first end than at the second end.

9. The integrated circuit of claim 1, and/or wherein the mask has a thickness of approximately 0.6 microns in a direction parallel to the first optical axis.

10. The integrated circuit of any one of claims 1 to 9, wherein the drain region is coupled to the photodetection region by a charge transfer channel.

11. The integrated circuit of claim 10, further comprising:

a transfer gate electrically coupled to the charge transfer channel and configured to control a transfer of charge carriers from the photodetection region to the drain region.

12. The integrated circuit of claim 11, wherein the transfer gate is configured to receive a control signal and bias the charge transfer channel to transfer charge carriers using the control signal.

13. The integrated circuit of claim 5, further comprising a pixel comprising the photodetection region, the first charge storage region, and the drain region, wherein the pixel has an area smaller than or equal to 7.5 microns x 5 microns.

14. A method of manufacturing the integrated circuit of any one of claims 1 to 13, the method comprising:

depositing an at least partially opaque and at least partially insulative material on at least a portion of the photodetection region; and

removing at least a portion of the at least partially opaque and at least partially insulative material to create an opening having a triangular shape.

15. The method of claim 14, further comprising doping the photodetection region through the opening.

16. The integrated circuit of any one of claims 1 to 13, or the method of claim 14 or 15, further comprising a mask, wherein the mask includes the at least partially opaque and at least partially insulative layer.

17. An integrated circuit, comprising:

a first pixel comprising a first photodetection region configured to induce an electric field in a first direction; and

a second pixel comprising a second photodetection region configured to induce an electric field in a second direction substantially opposite the first direction,

wherein the first and second pixels are positioned one after another in one of the first and second directions.

18. The integrated circuit of claim 17, wherein:

the first pixel comprises a drain region and/or a charge storage region positioned after the first photodetection region in the first direction; and

the second pixel comprises a drain region and/or a charge storage region positioned after the second photodetection region in the second direction.

19. The integrated circuit of claim 18, further comprising:

a first row of pixels comprising the first pixel and each comprising a first photodetection region configured to induce an electric field in the first direction; and

a second row of pixels comprising the second pixel and each comprising a second photodetection region configured to induce an electric field in the second direction,

wherein the first row of pixels and the second row of pixels are positioned one after another in one of the first and second directions.

20. The integrated circuit of claim 18, wherein:

the first pixel comprises a first charge storage region positioned after the first photodetection region in the first direction; and

the second pixel comprises a second photodetection region positioned after the second photodetection region in the second direction.

21. A system, comprising:

the integrated circuit of any one of claims 5 to 13 and 16 to 20; and

a control circuit configured to provide control signals to transfer gates of the integrated circuit to accumulate charge carriers in the first charge storage region over a plurality of collection periods, each collection period corresponding to a pulse of excitation light.