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(71) Applicant: **MICRON TECHNOLOGY, INC.** [US/US];
8000 South Federal Way, Boise, ID 83716-9632 (US).

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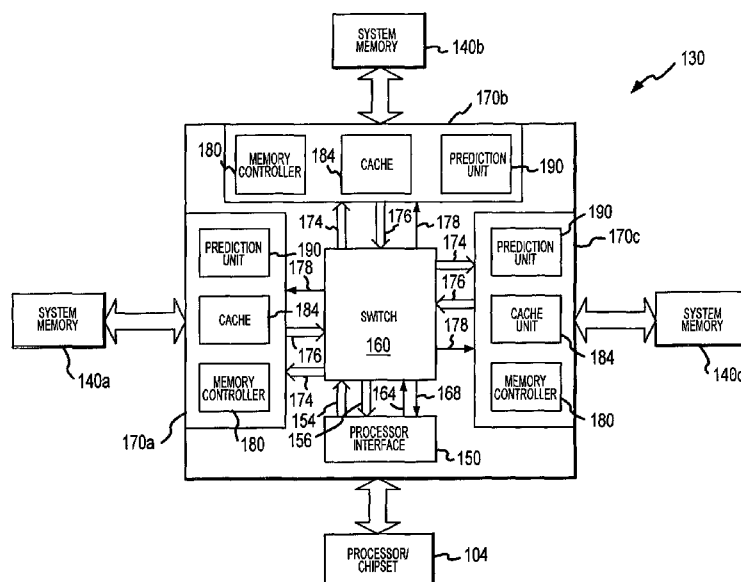
(72) Inventor: **JEDDELOH, Joseph**; 4302 Reiland Lane, Shoreview, MN 55126 (US).

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(74) Agents: **BULCHIS, Edward, W.** et al.; Dorsey & Whitney LLP, 1420 Fifth Avenue, Suite 3400, Seattle, WA 98101 (US).

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(54) Title: **MEMORY HUB WITH INTERNAL CACHE AND/OR MEMORY ACCESS PREDICTION**



(57) **Abstract:** A computer system includes a memory hub (130) for coupling a processor (104) to a plurality of synchronous dynamic random access memory ("SDRAM") devices (140a-c). The memory hub (130) includes a processor interface (150) coupled to the processor (104) and a plurality of memory interfaces (170a-c) coupled to respective SDRAM devices (140a-c). The processor interface (150) is coupled to the memory interfaces (170a-c) by a switch (160). Each of the memory interfaces (170a-c) includes a memory controller (180), a cache memory (184), and a prediction unit (190). The cache memory (184) stores data recently read from or written to the respective SDRAM device (140a-c) so that it can be subsequently read by processor (104) with relatively little latency. The prediction unit (190) prefetches data from an address from which a read access is likely based on a previously accessed address.