FIG. 1

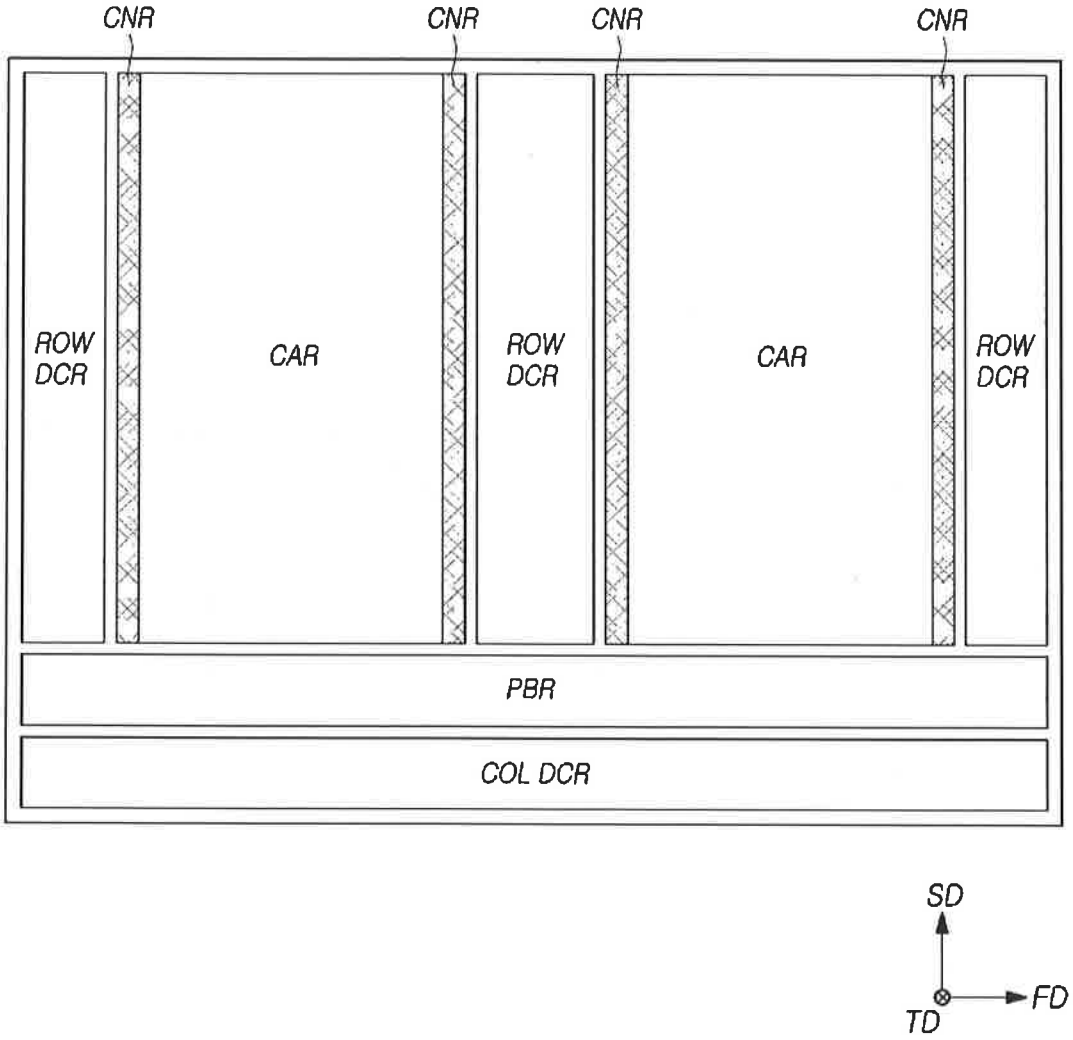

CNR
CNR
CNR
CNR
ROW DCR
CAR
ROW DCR
CAR
ROW DCR
PBR
COL DCR
SD
FD
TD

FIG.2

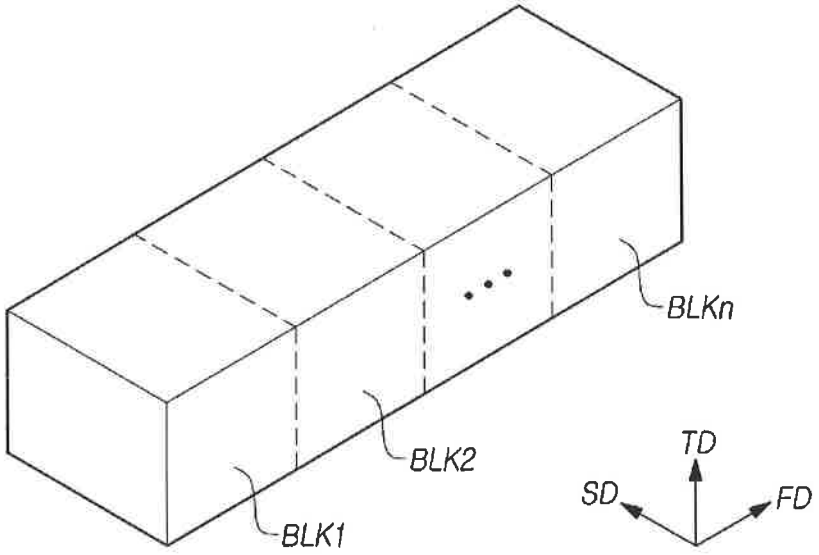


FIG.3

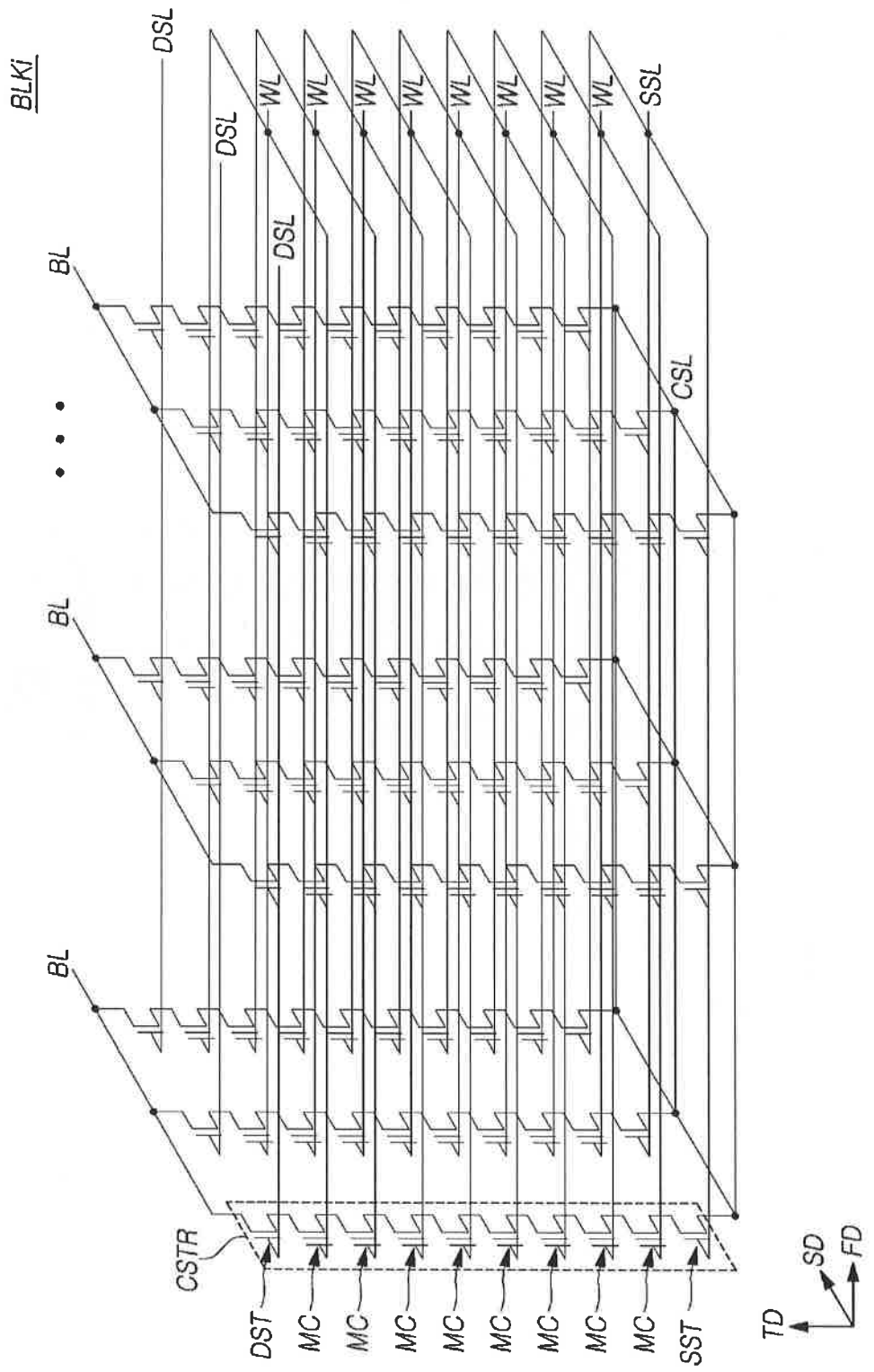

BLKi
BL
BL
BL
DSL
DSL
DSL
WL
WL
WL
WL
WL
WL
WL
WL
SSL
CSL
CSTR
DST
MC
MC
MC
MC
MC
MC
MC
MC
SST
TD
SD
FD

FIG.4

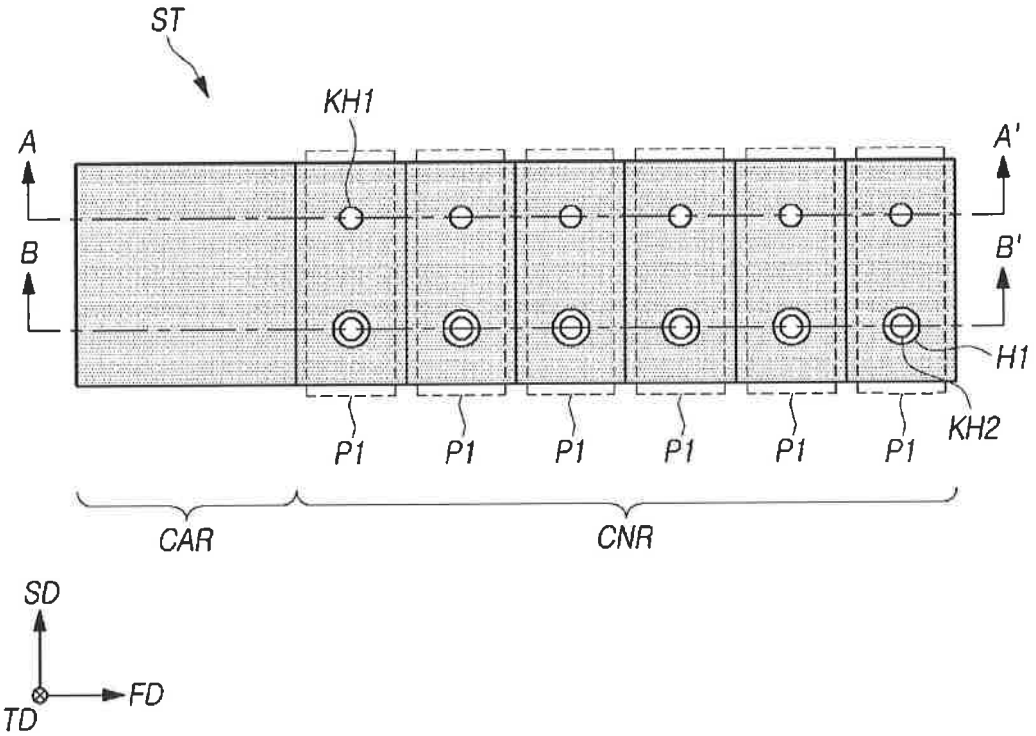


FIG. 5

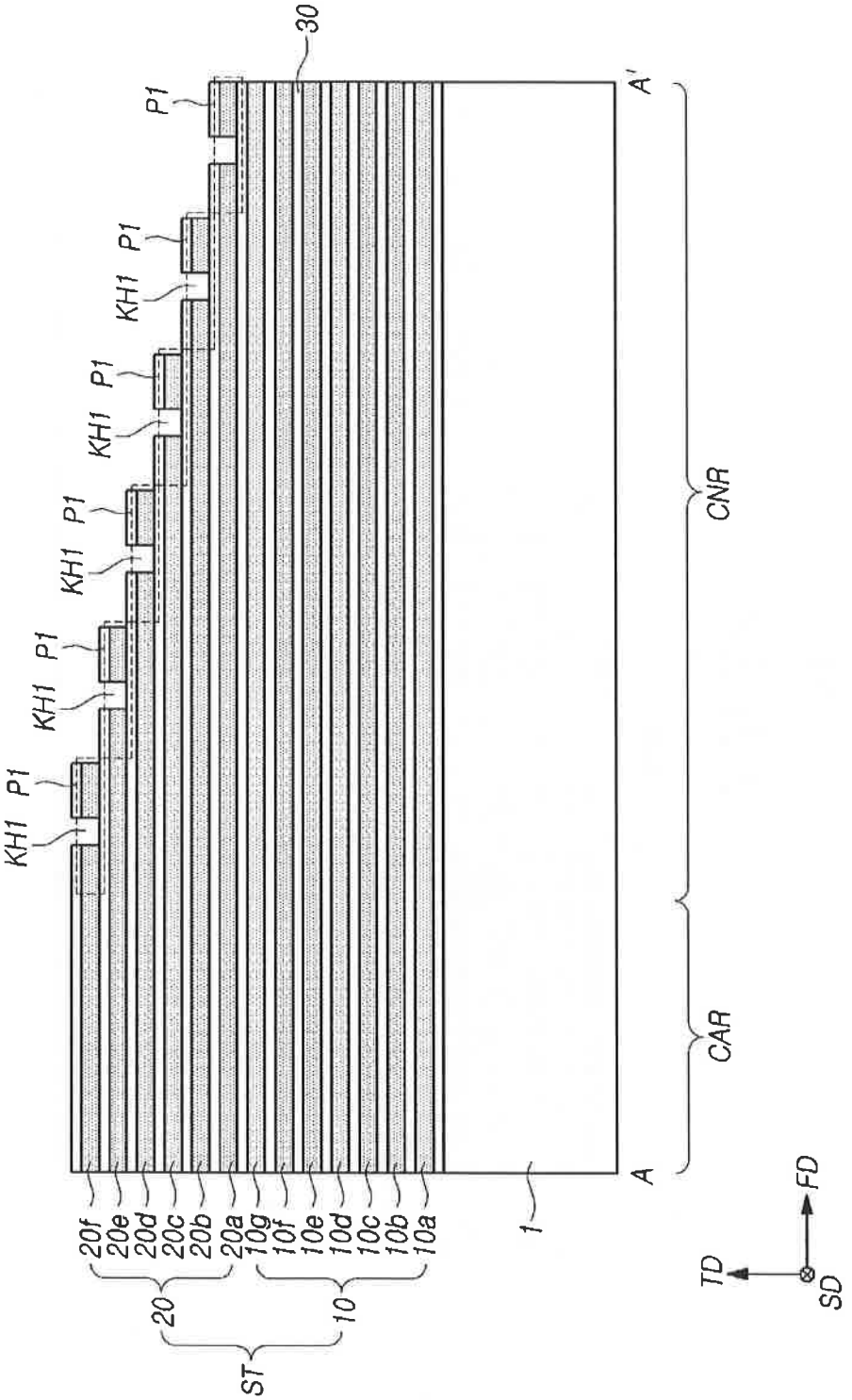

30
P1
KH1
A
A'
CNR
CAR
20f
20e
20d
20c
20b
20a
10g
10f
10e
10d
10c
10b
10a
1
20
10
ST
TD
FD
SD

FIG.6

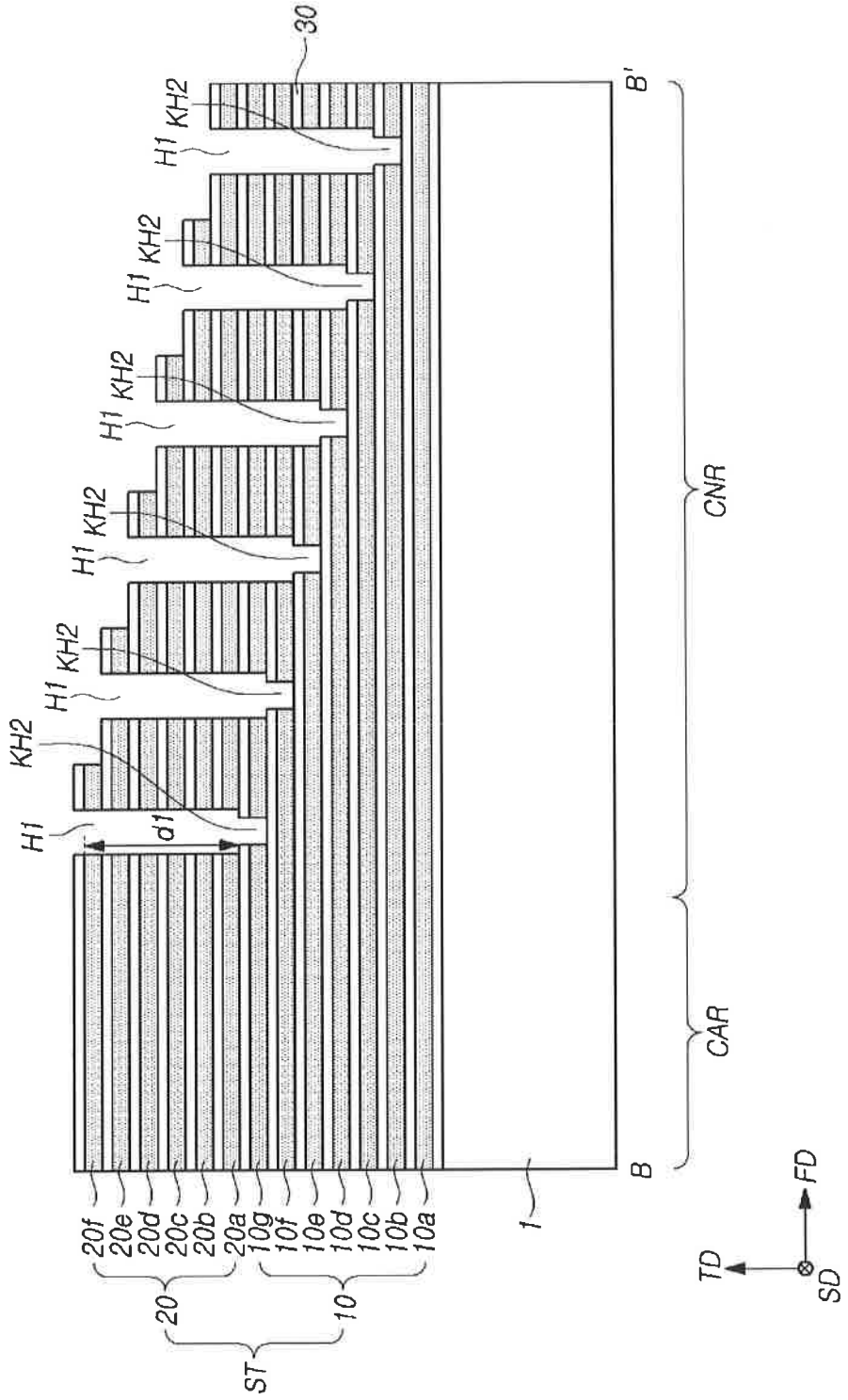

30
B'
H1
KH2
d1
CNR
CAR
B
1
20f
20e
20d
20c
20b
20a
10g
10f
10e
10d
10c
10b
10a
20
10
ST
TD
FD
SD

FIG. 7

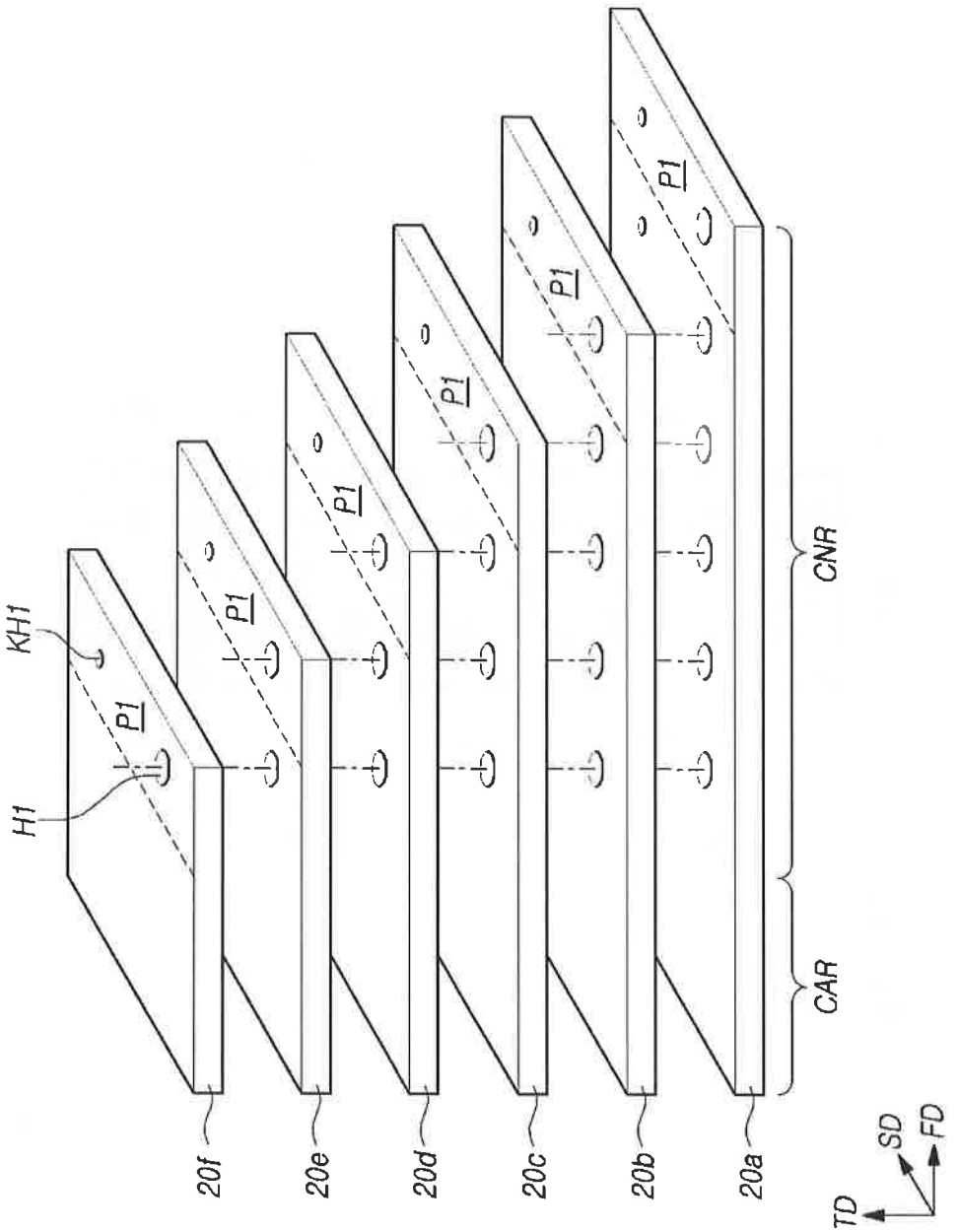


FIG. 8

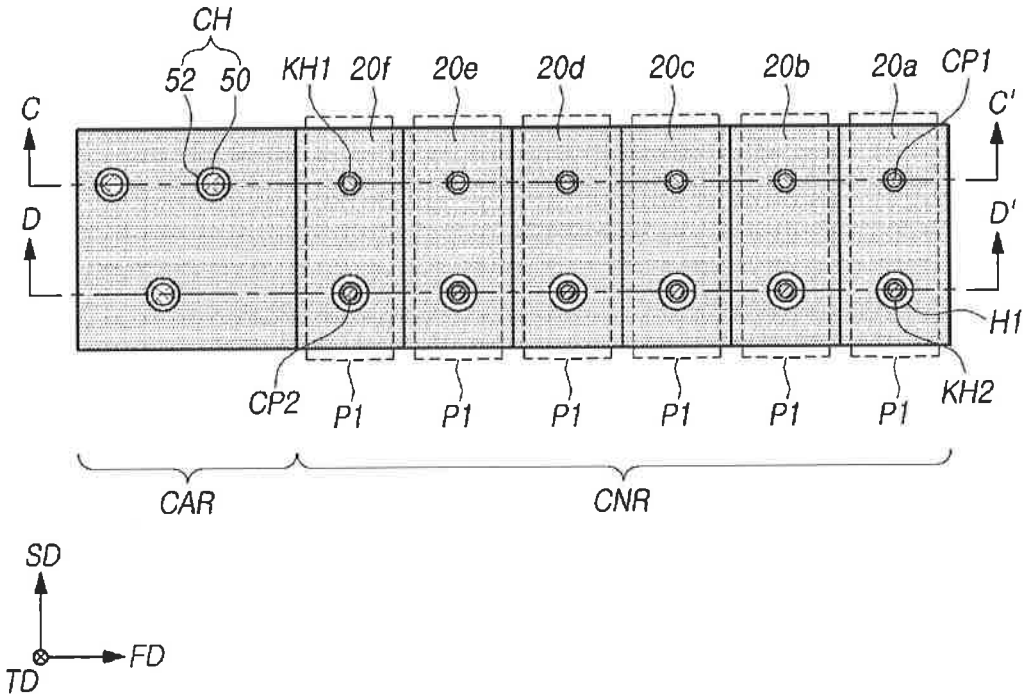

CH
52
50
KH1
20f
20e
20d
20c
20b
20a
CP1
C
C'
D
D'
H1
CP2
P1
P1
P1
P1
P1
P1
KH2
CAR
CNR
SD
FD
TD

FIG. 9

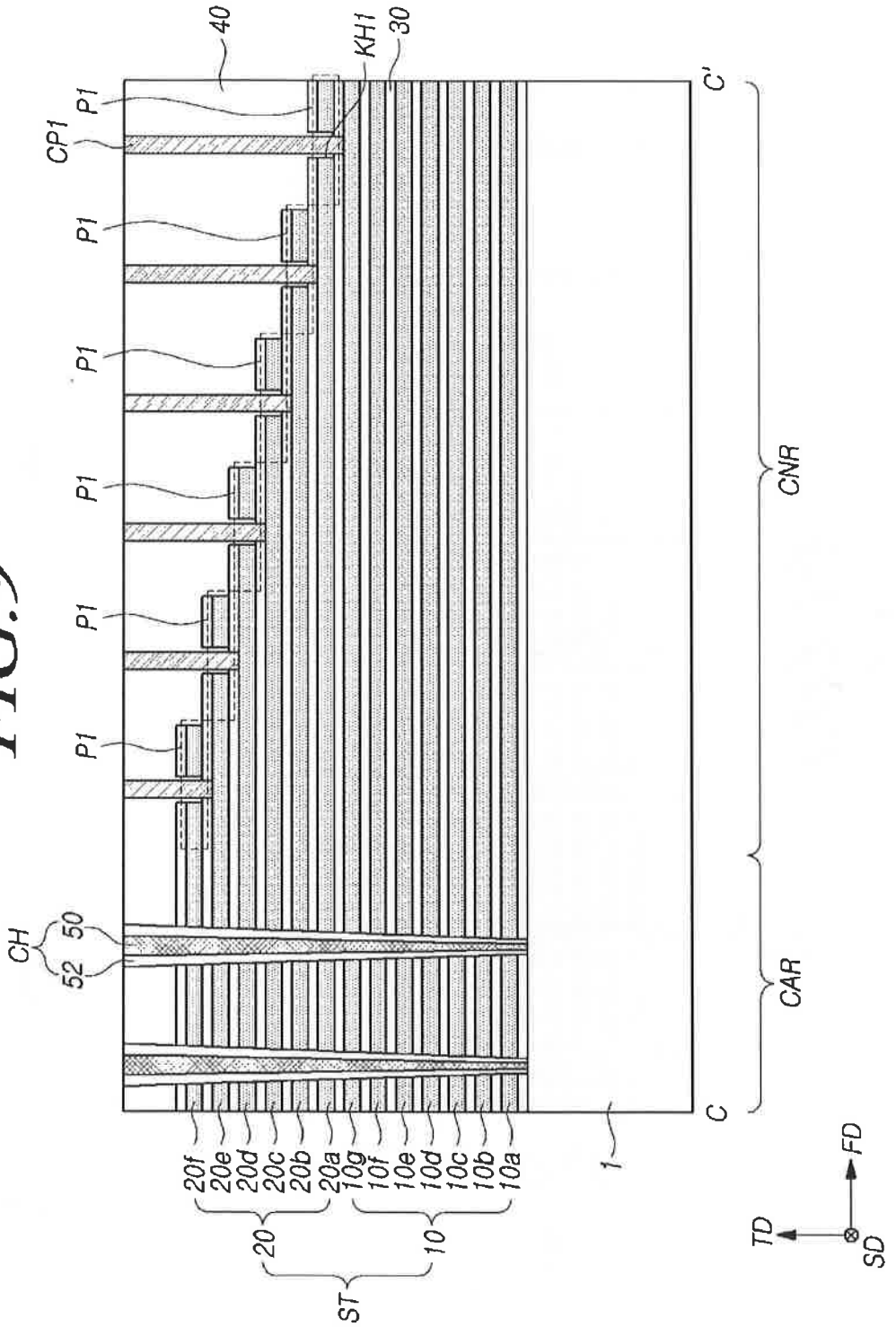

40
KH1
30
P1
CP1
C'
CH
50
52
CNR
CAR
C
20f
20e
20d
20c
20b
20a
10g
10f
10e
10d
10c
10b
10a
1
20
10
ST
TD
FD
SD

FIG. 10

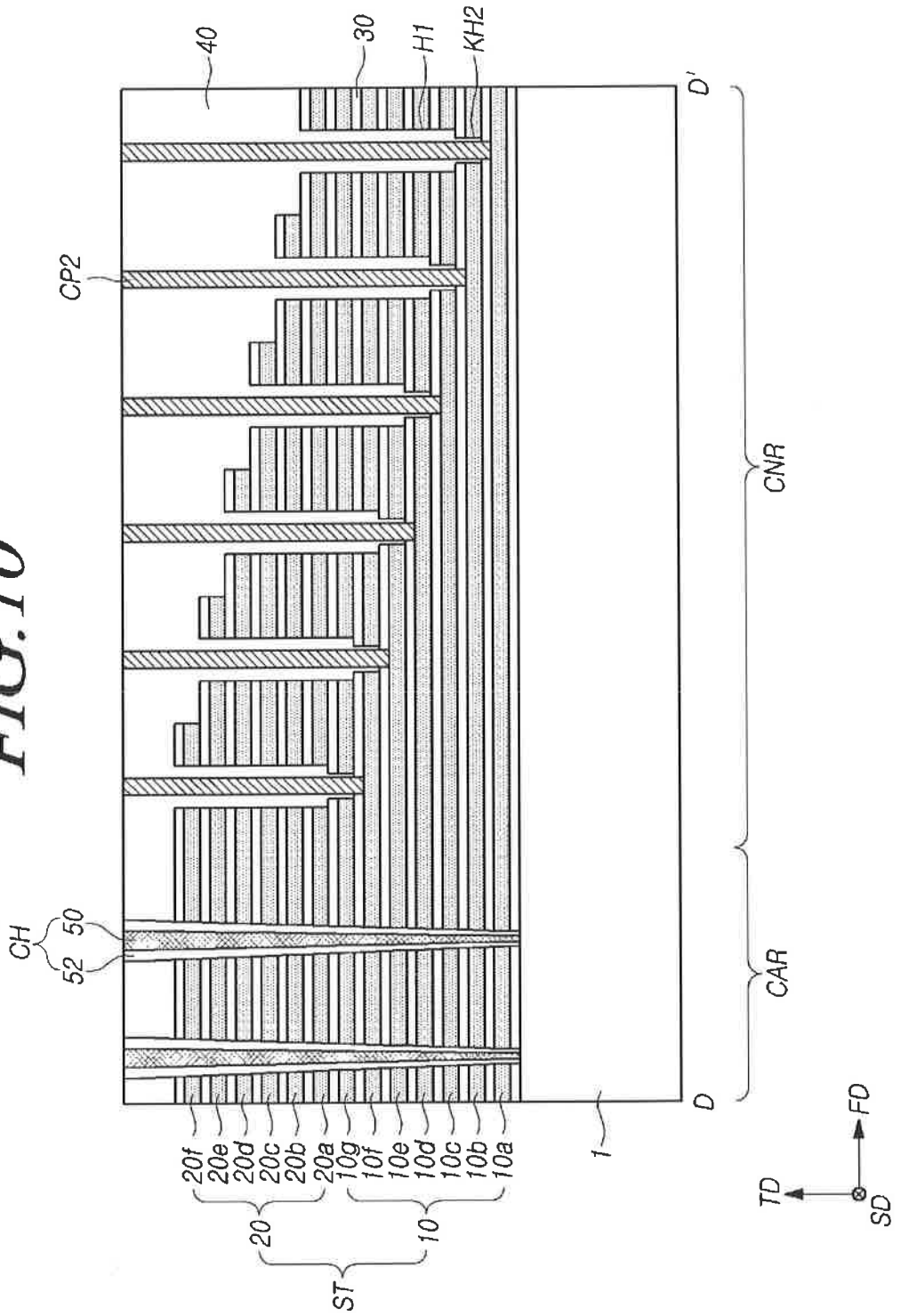

40
30
H1
KH2
D'
CP2
CNR
CH
50
52
CAR
D
20f
20e
20d
20c
20b
20a
10g
10f
10e
10d
10c
10b
10a
1
20
10
ST
TD
FD
SD

FIG. 11

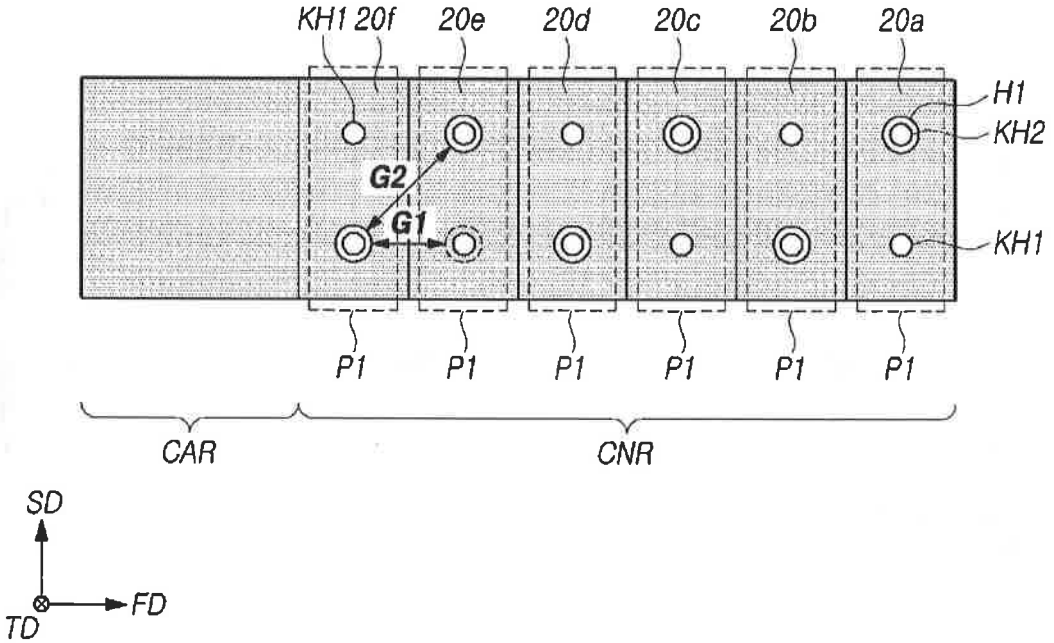

KH1
20f
20e
20d
20c
20b
20a
H1
KH2
KH1
G2
G1
P1
P1
P1
P1
P1
P1
CAR
CNR
SD
FD
TD

FIG. 12A

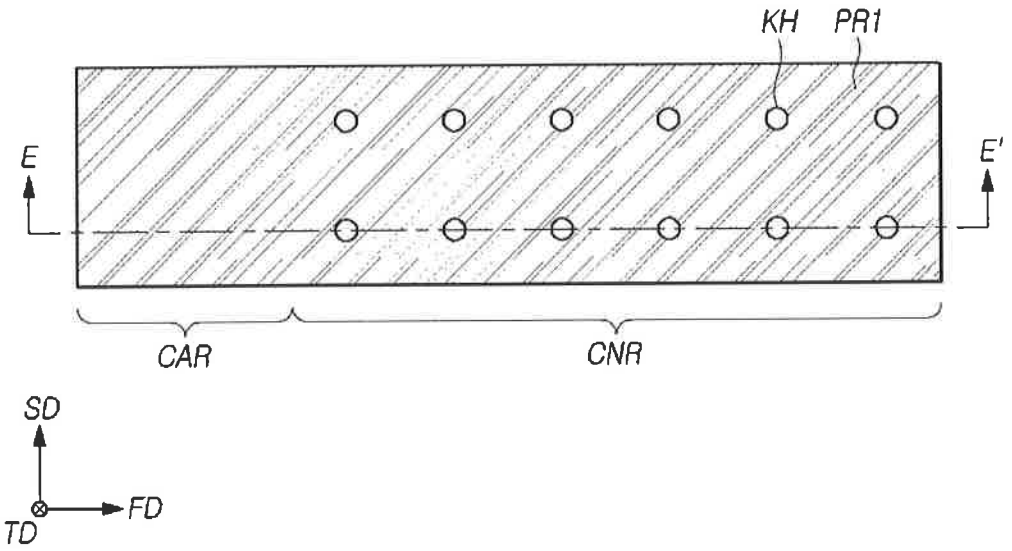


FIG. 12B

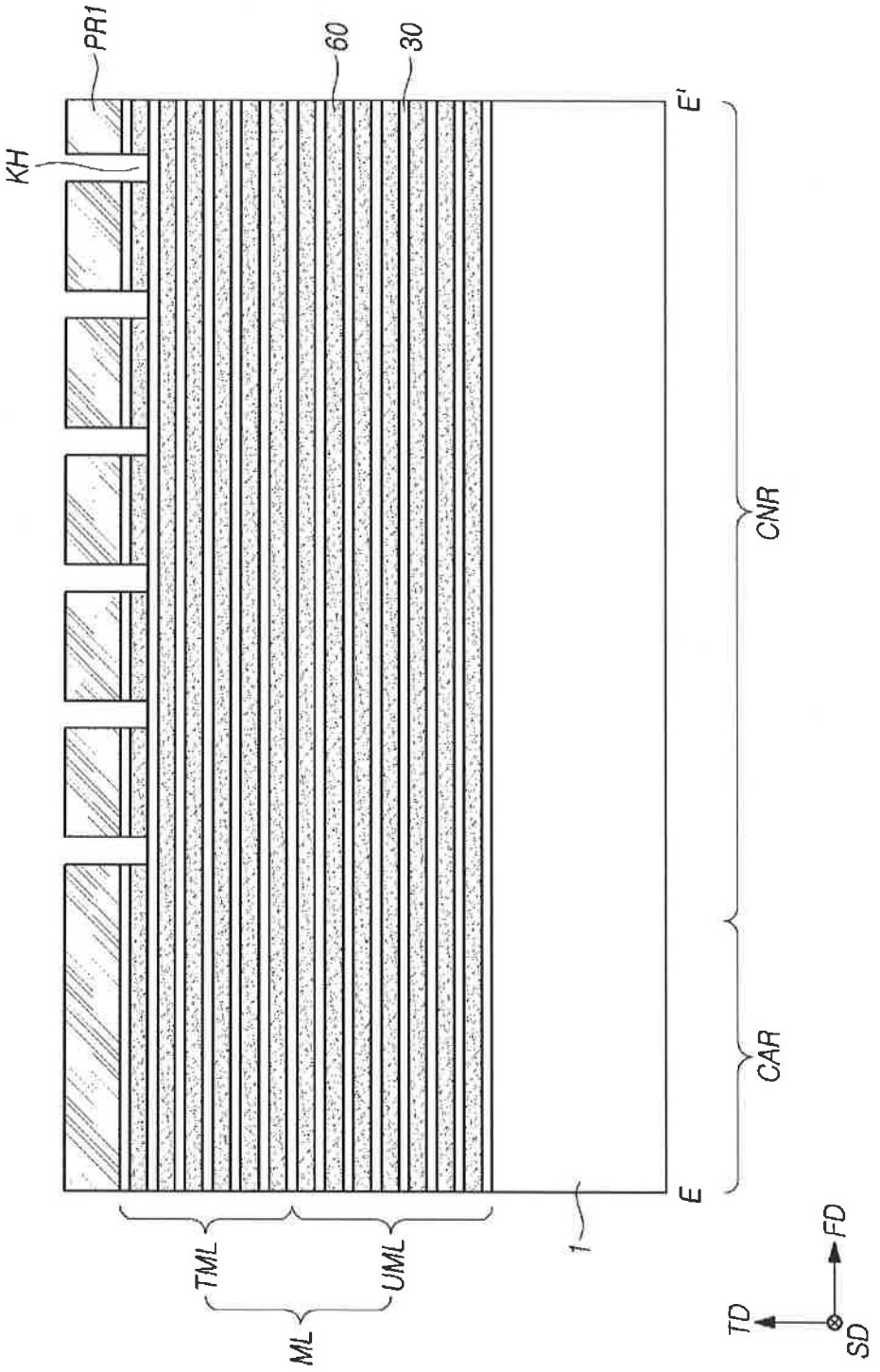


FIG. 13A

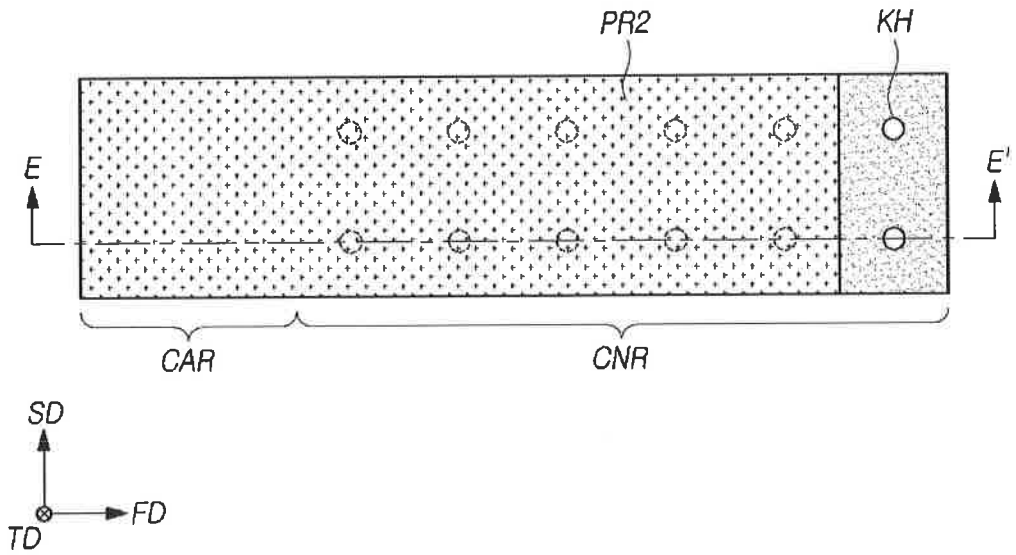


FIG. 13B

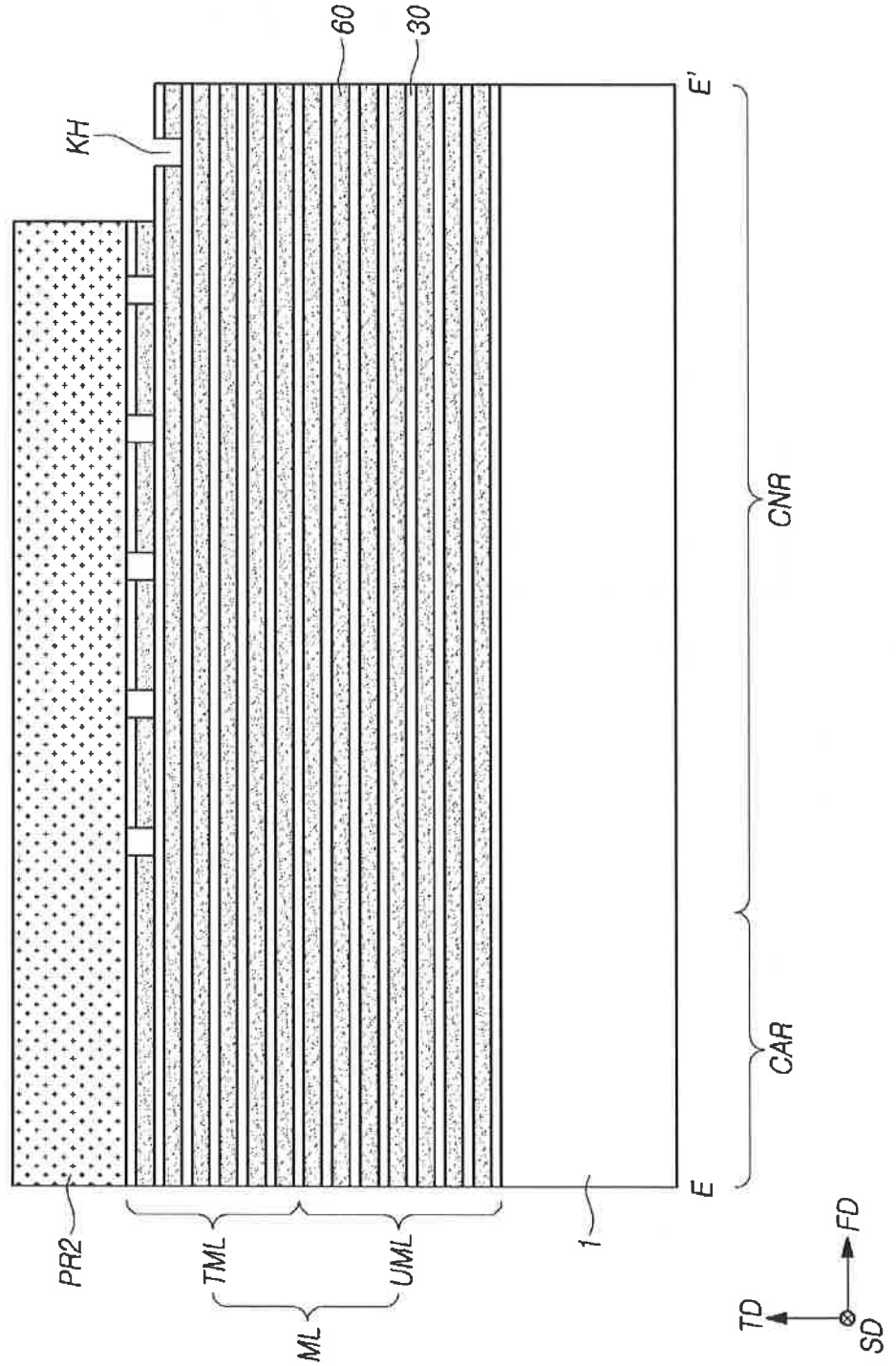


FIG. 14A

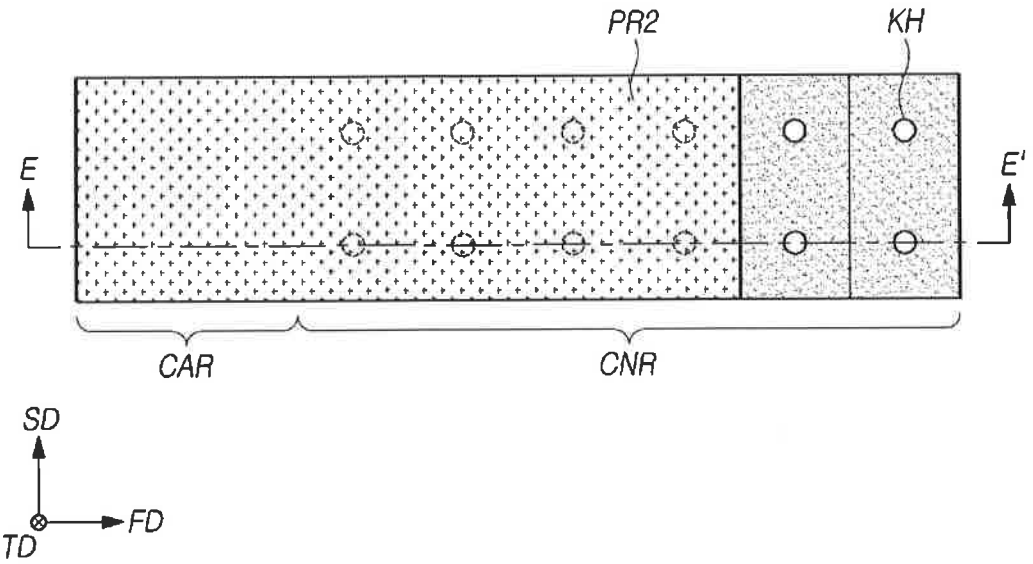


FIG. 14B

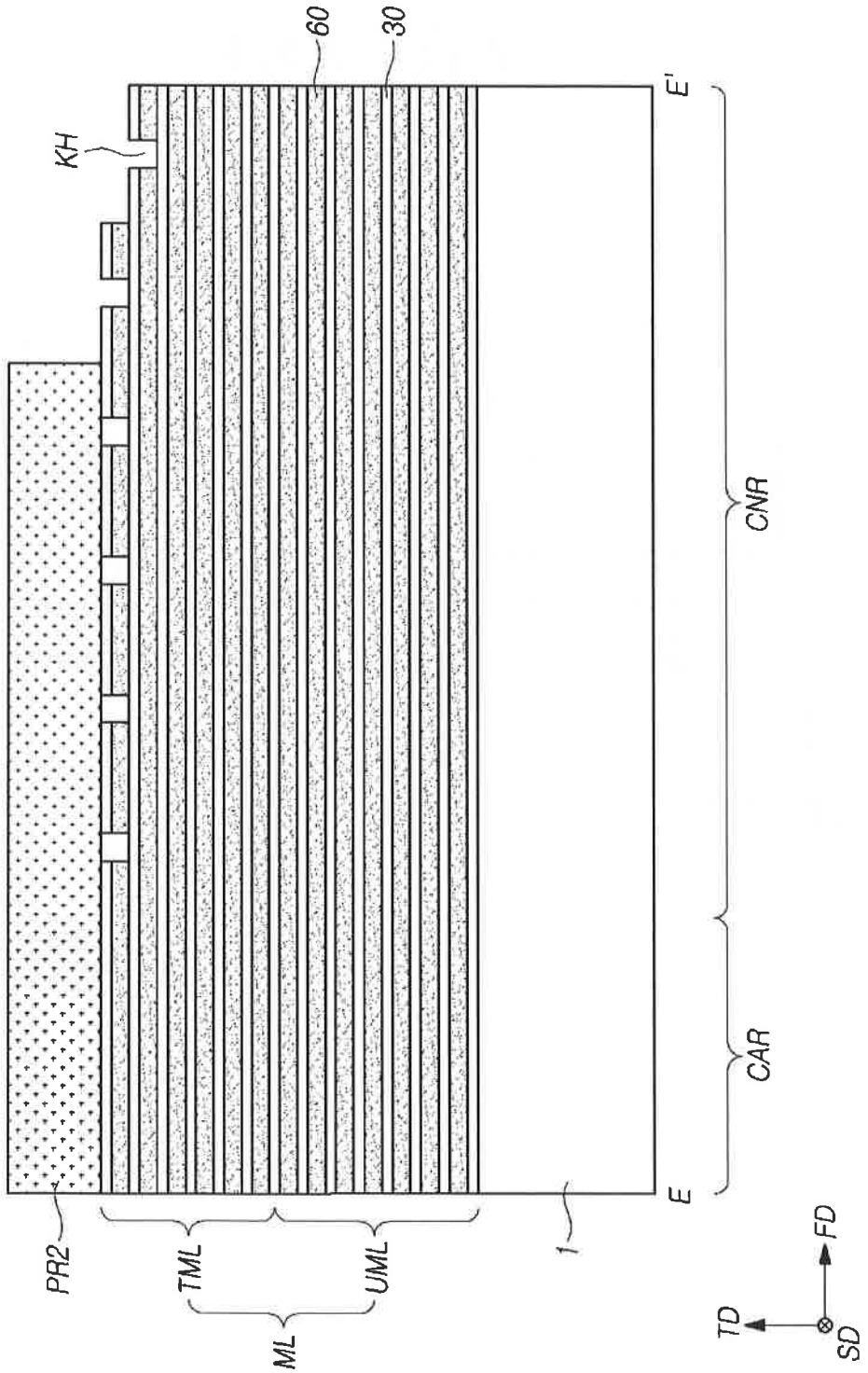


FIG. 15A

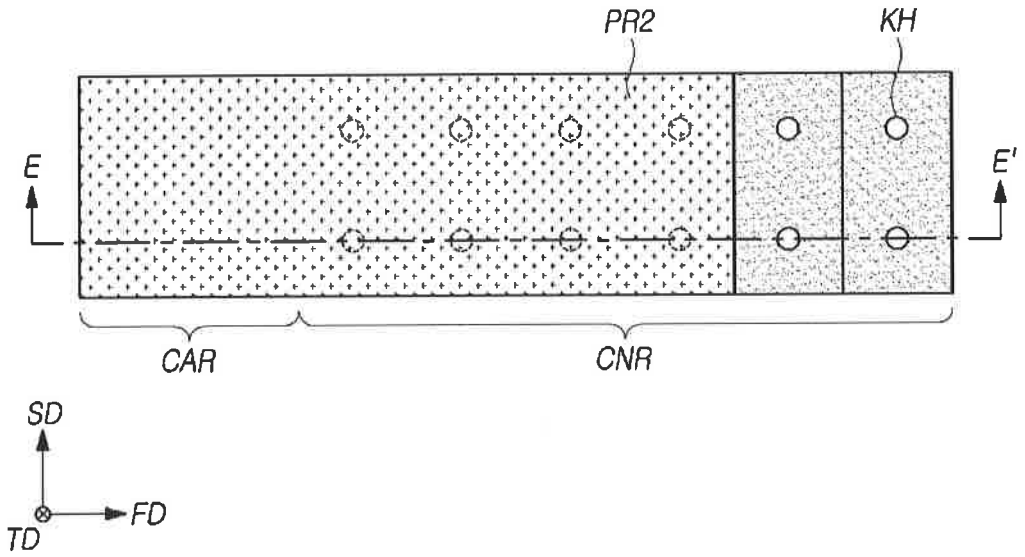


FIG. 15B

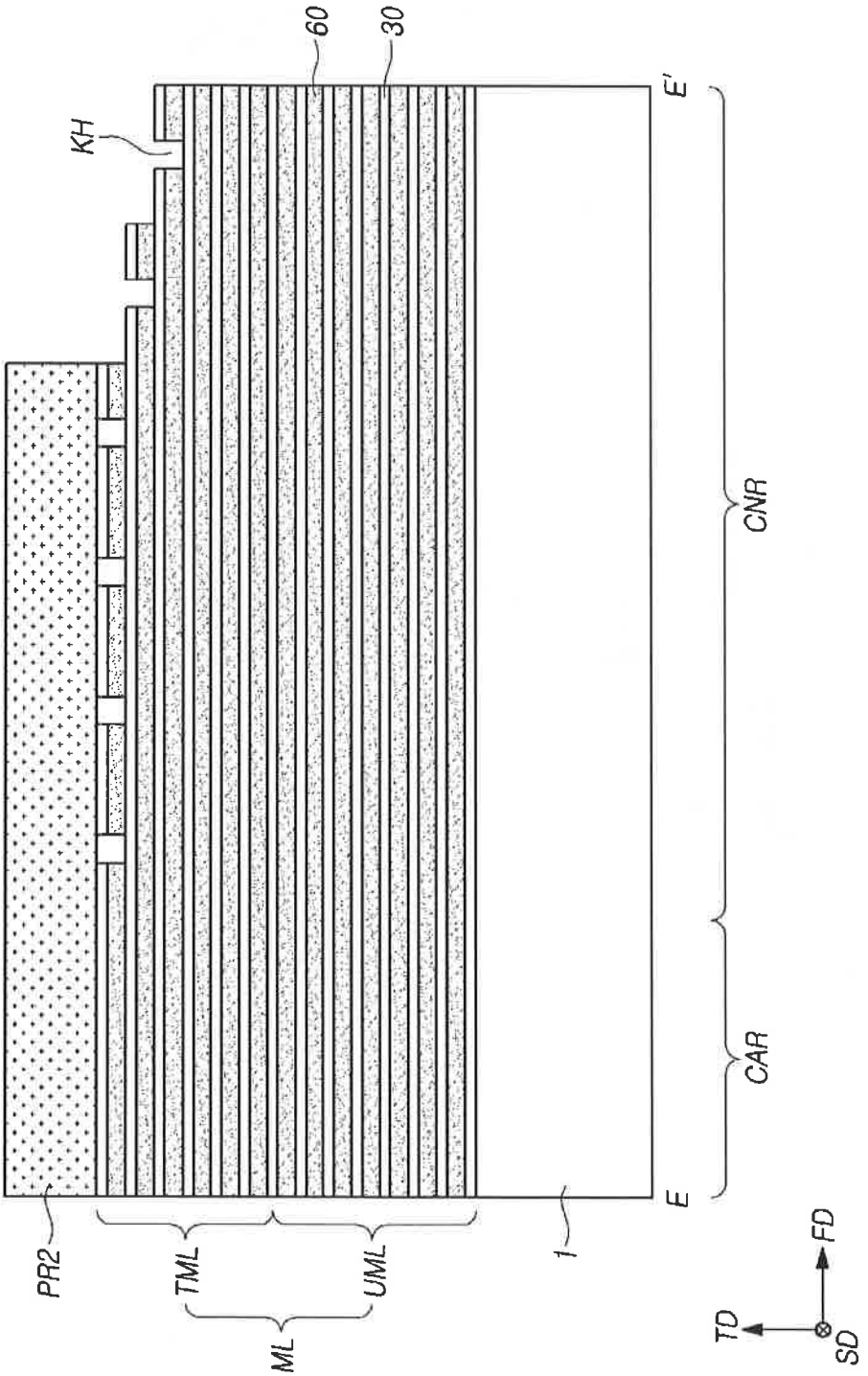


FIG. 16A

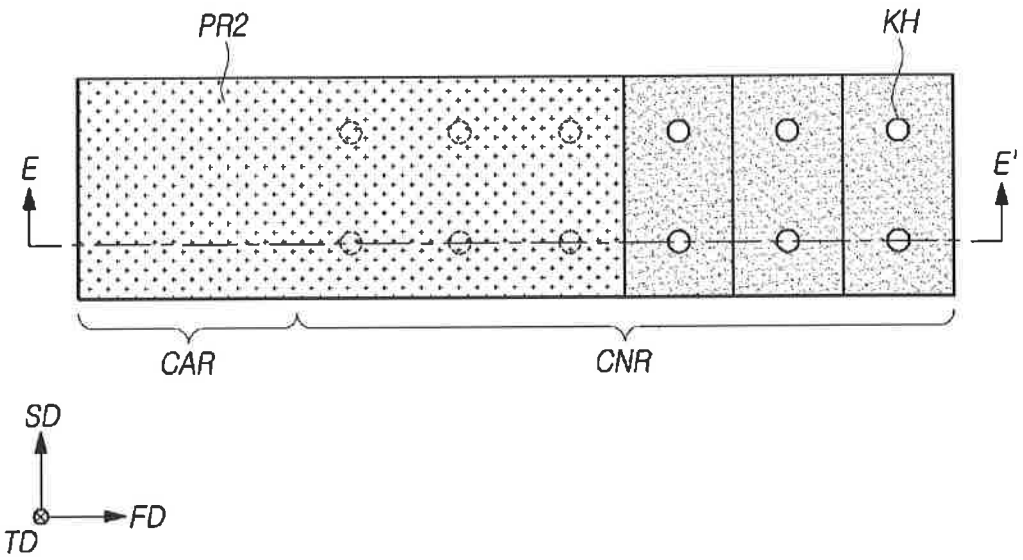


FIG. 16B

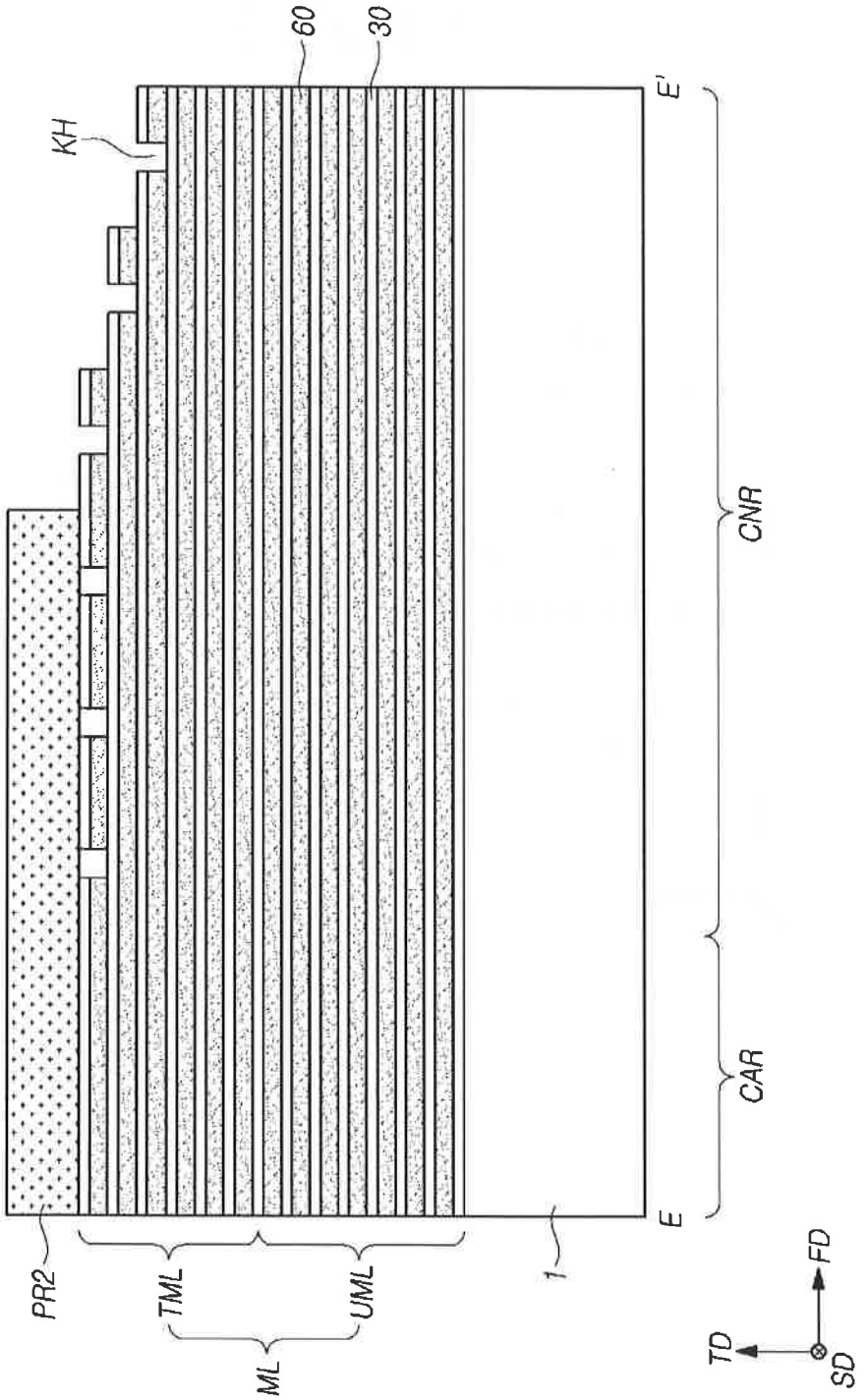


FIG. 17A

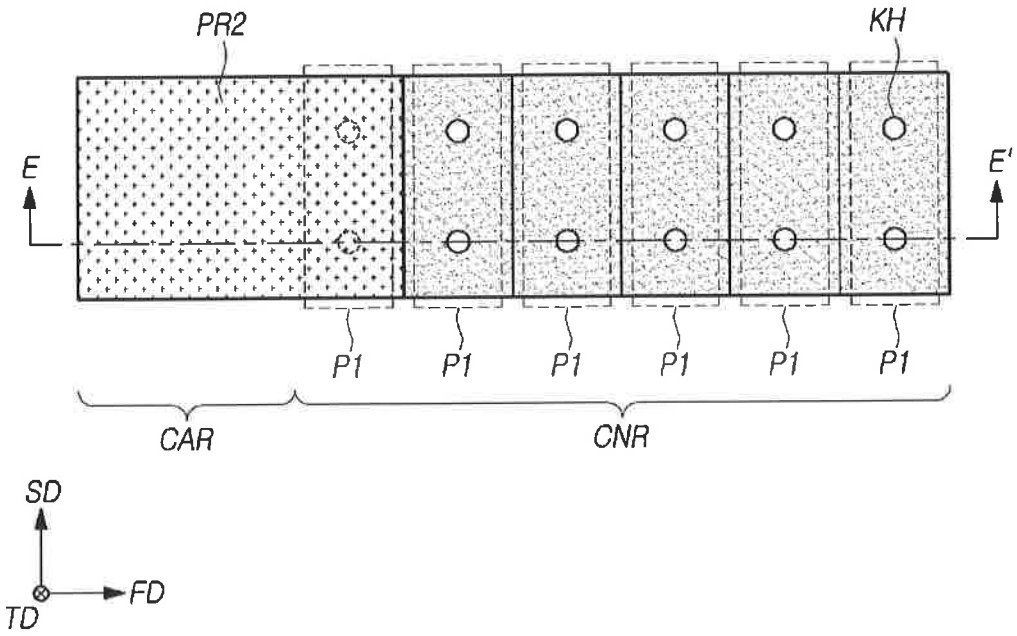


FIG. 17B

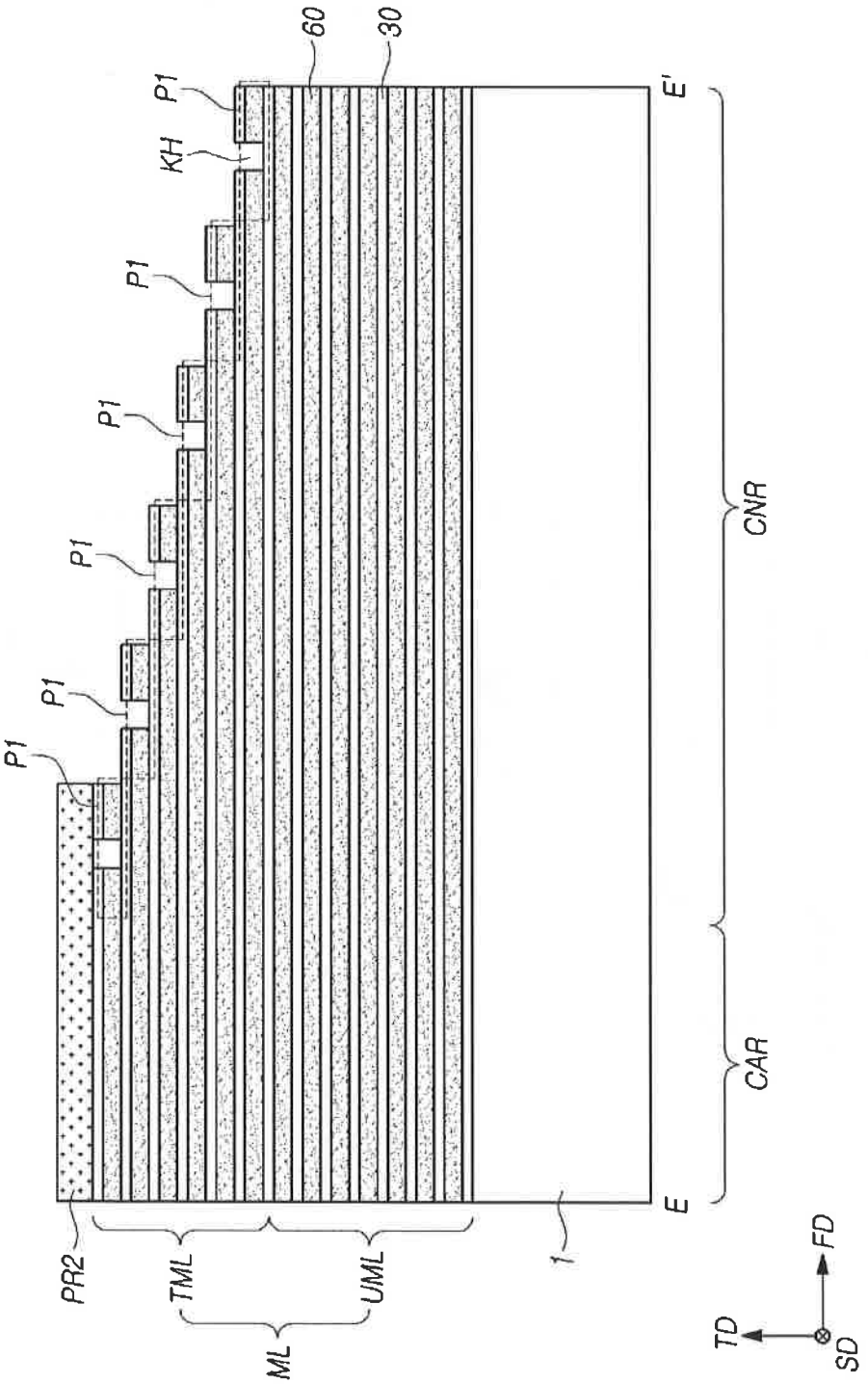


FIG. 18A

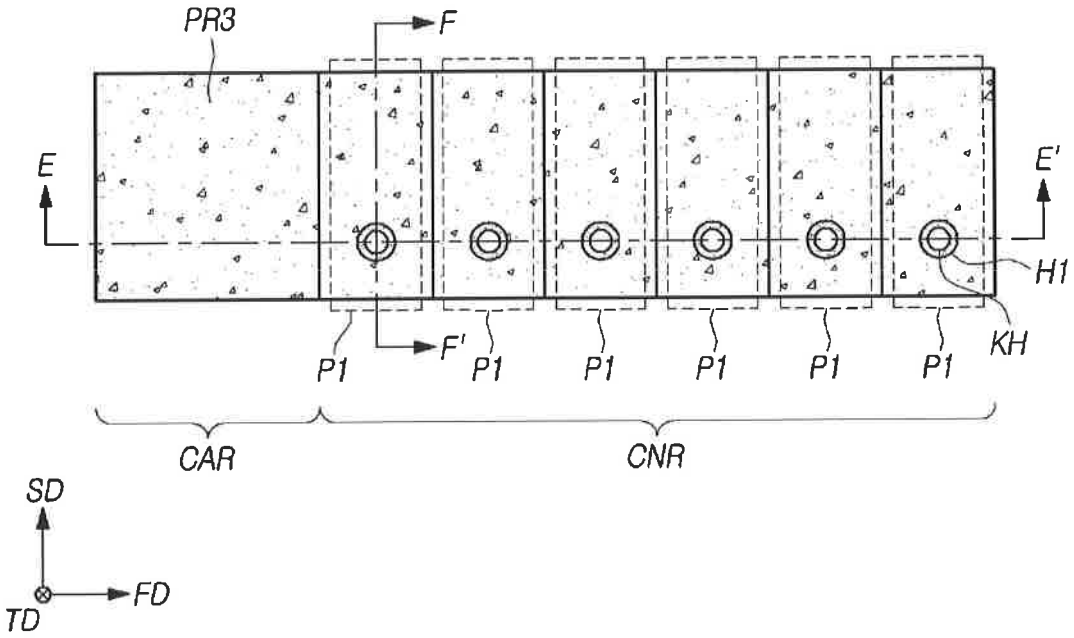


FIG. 18B

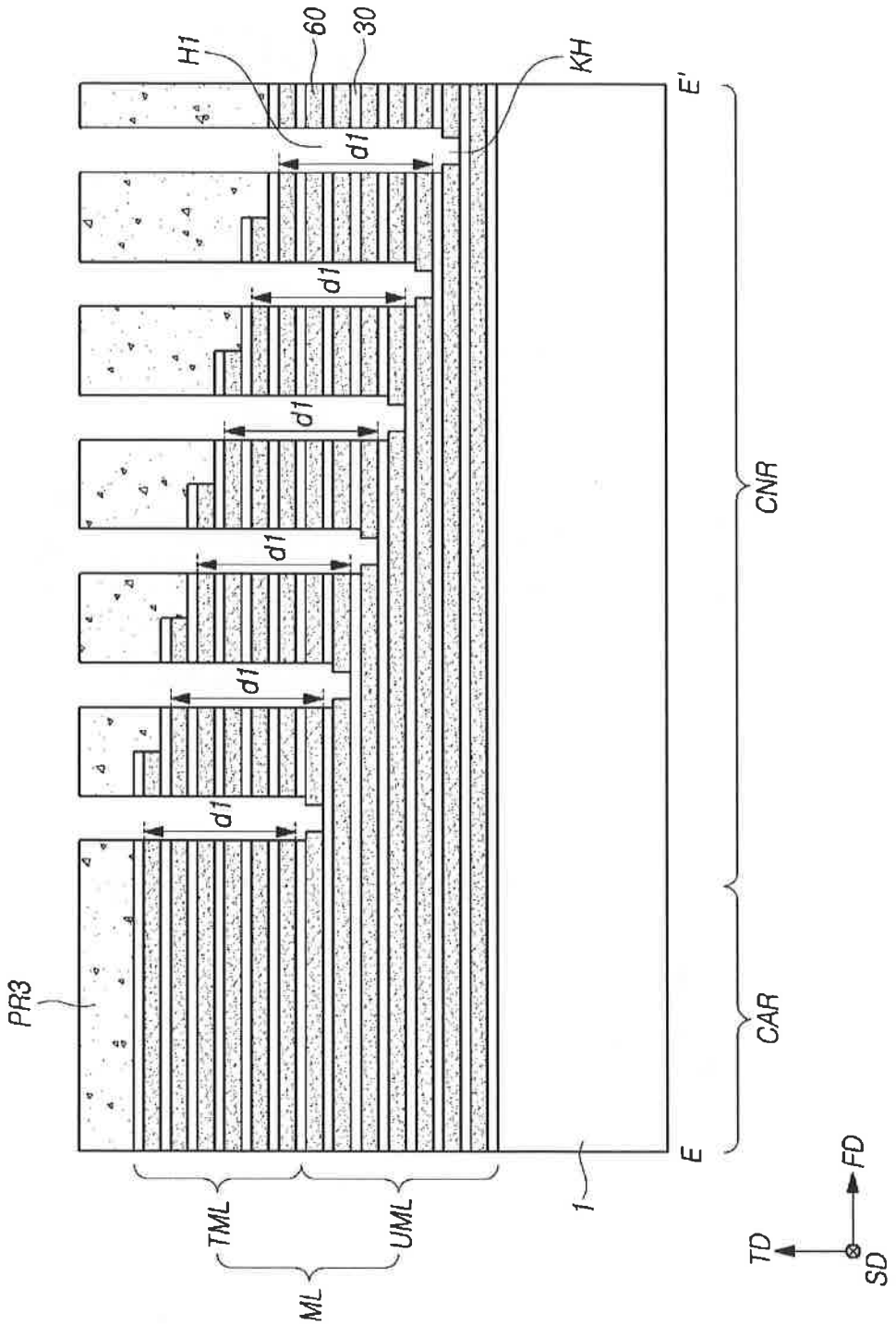


FIG. 18C

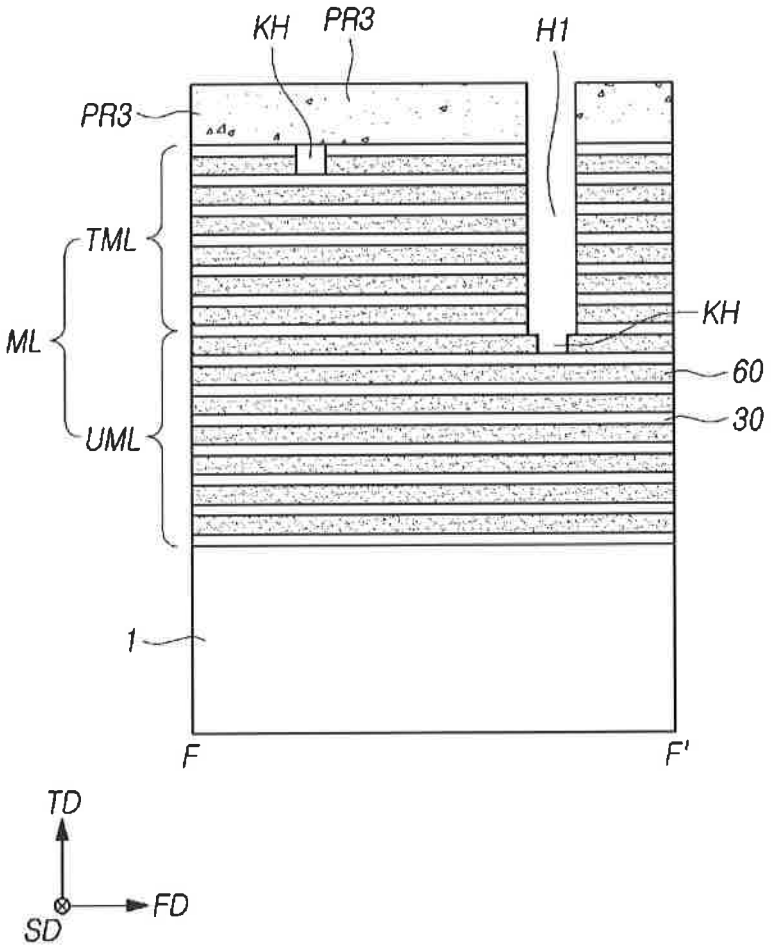


FIG. 19

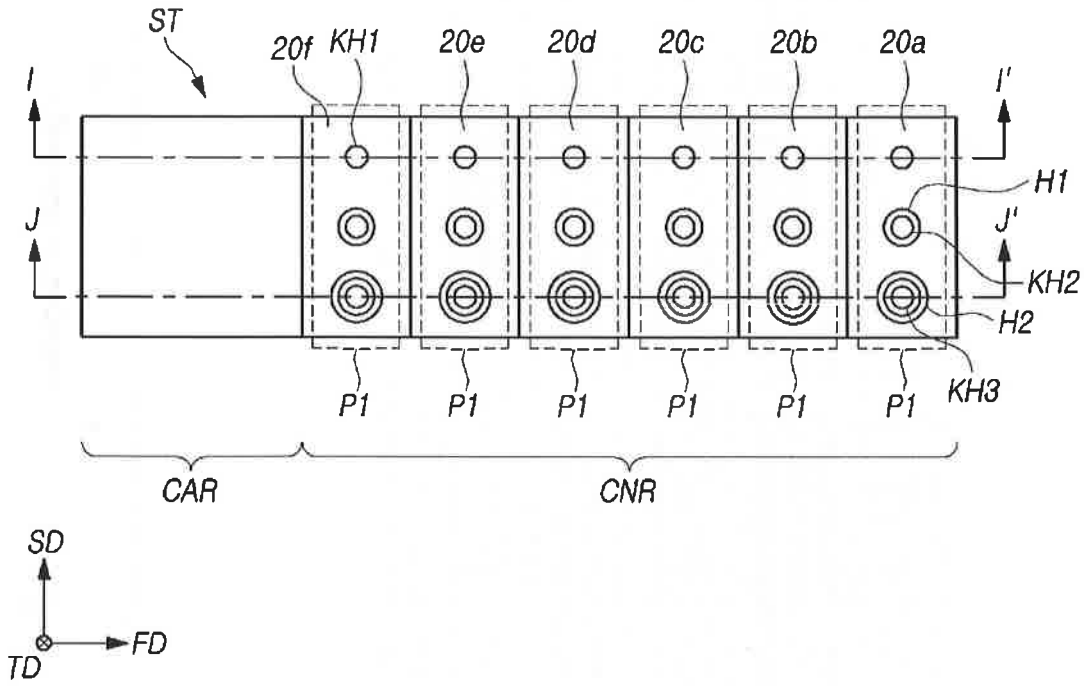

ST
20f
KH1
20e
20d
20c
20b
20a
I
I'
J
J'
H1
KH2
H2
KH3
P1
P1
P1
P1
P1
P1
CAR
CNR
SD
FD
TD

FIG.20

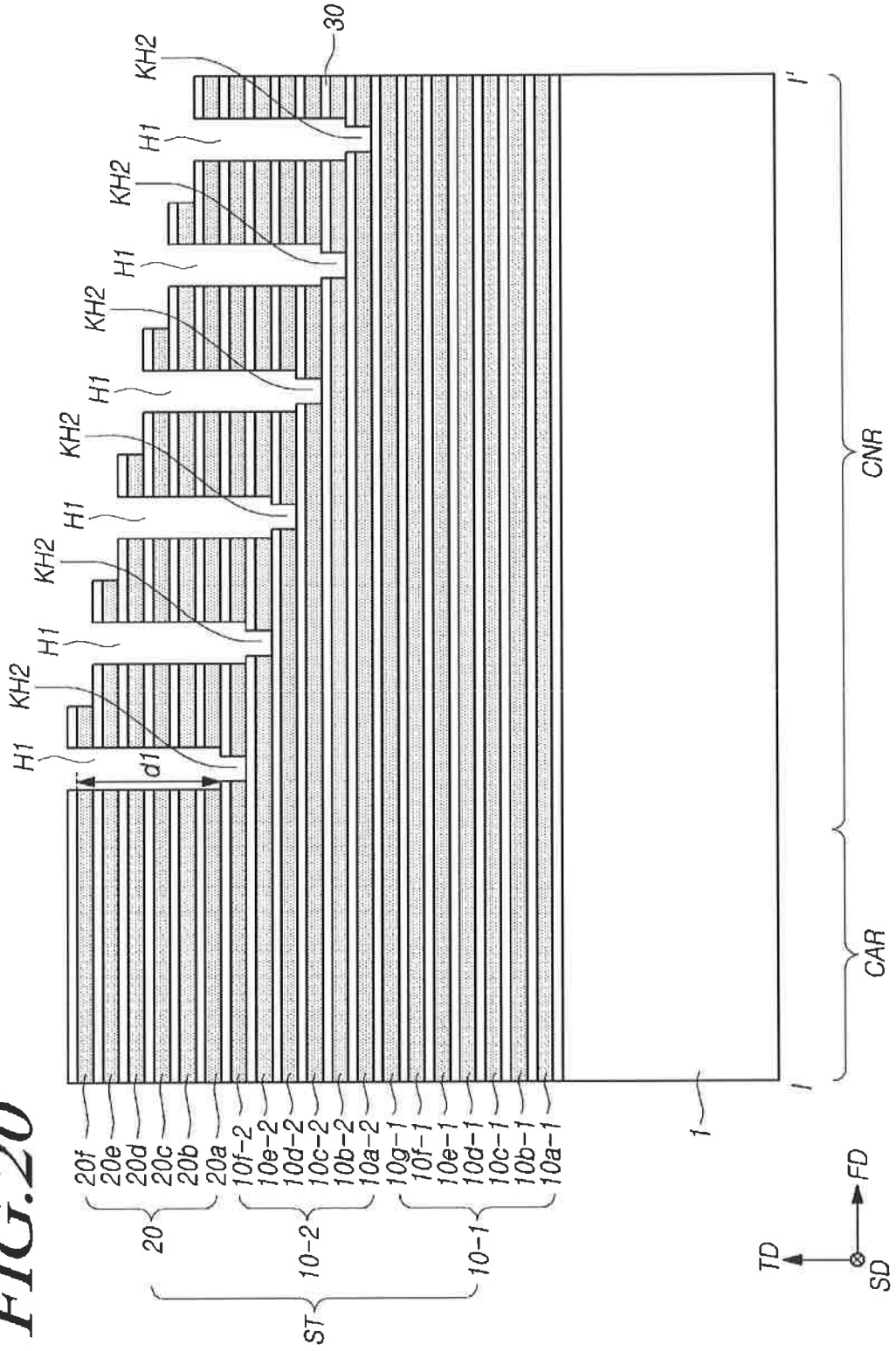

30
KH2
H1
KH2
H1
KH2
H1
KH2
H1
KH2
H1
KH2
H1
d1
20f
20e
20d
20c
20b
20a
10f-2
10e-2
10d-2
10c-2
10b-2
10a-2
10g-1
10f-1
10e-1
10d-1
10c-1
10b-1
10a-1
20
10-2
10-1
ST
1
1'
CAR
CNR
TD
FD
SD

FIG.21

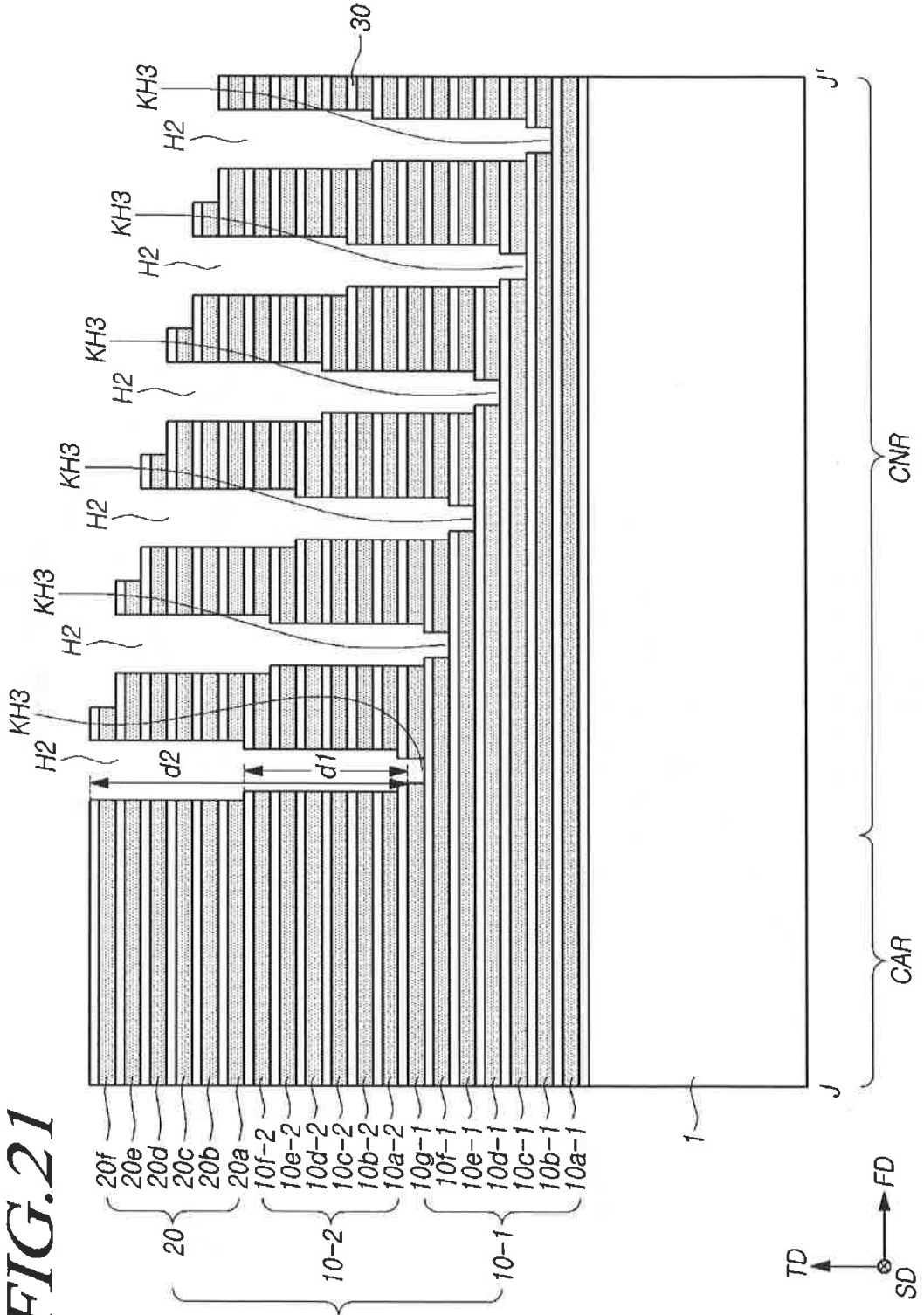

30
KH3
H2
J'
CNR
CAR
J
d2
d1
20f
20e
20d
20c
20b
20a
10f-2
10e-2
10d-2
10c-2
10b-2
10a-2
10g-1
10f-1
10e-1
10d-1
10c-1
10b-1
10a-1
1
20
10-2
10-1
ST
TD
FD
SD

FIG.22

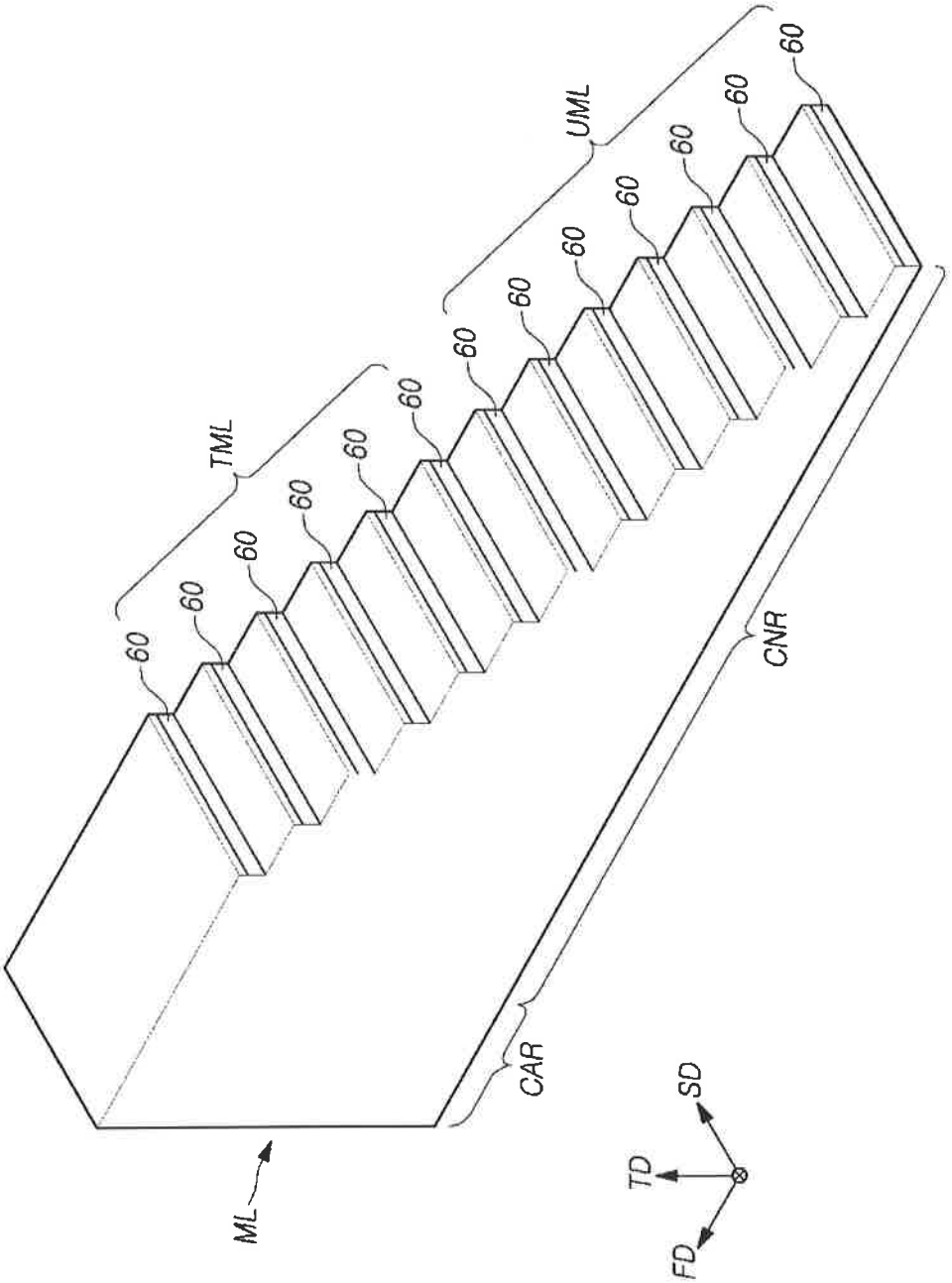


FIG.23

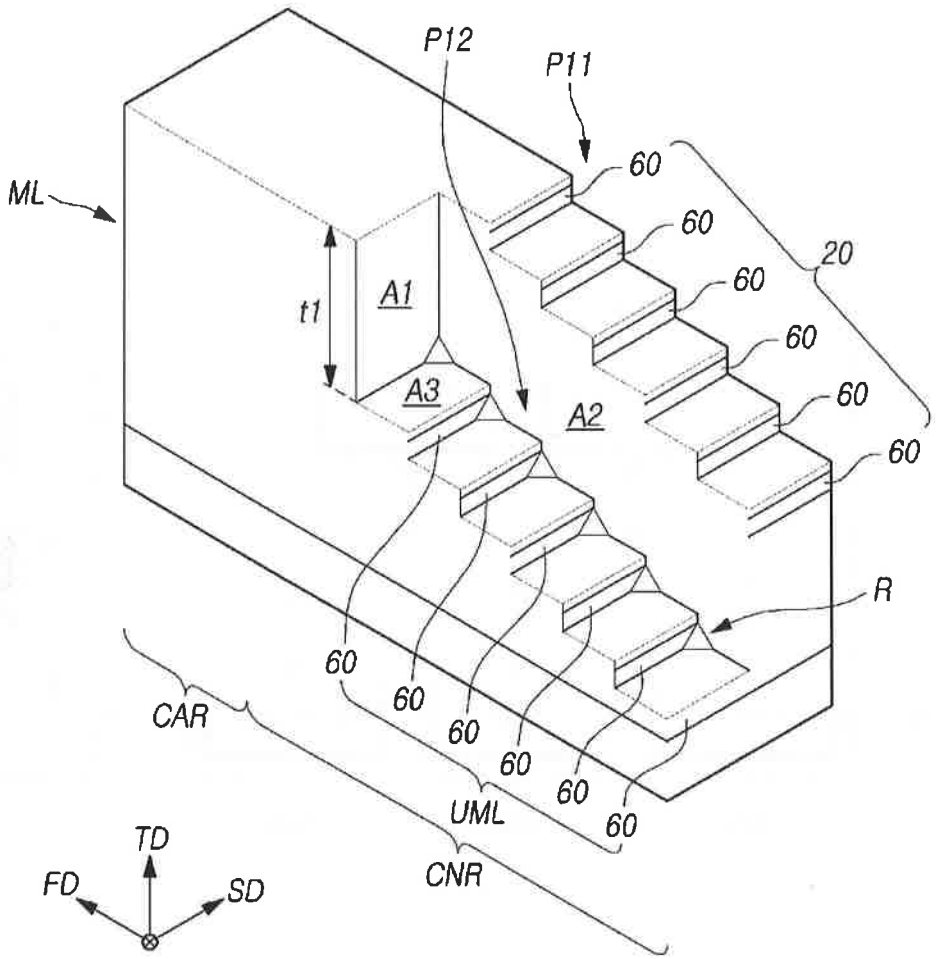

P12
P11
ML
60
60
60
60
60
60
20
t1
A1
A3
A2
R
60
60
60
60
60
60
CAR
UML
CNR
TD
FD
SD

FIG.24

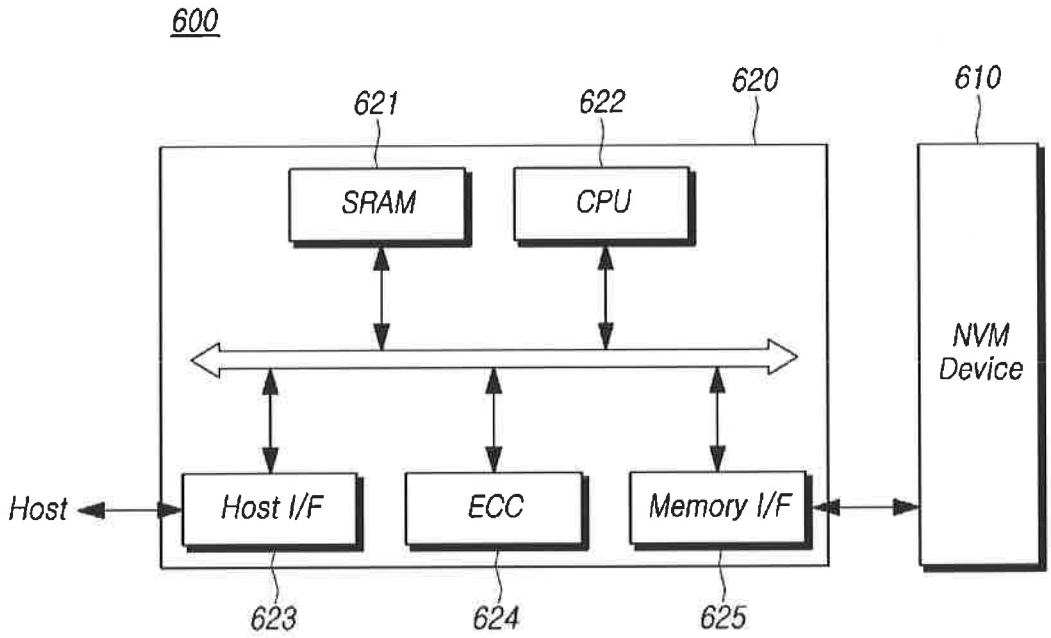
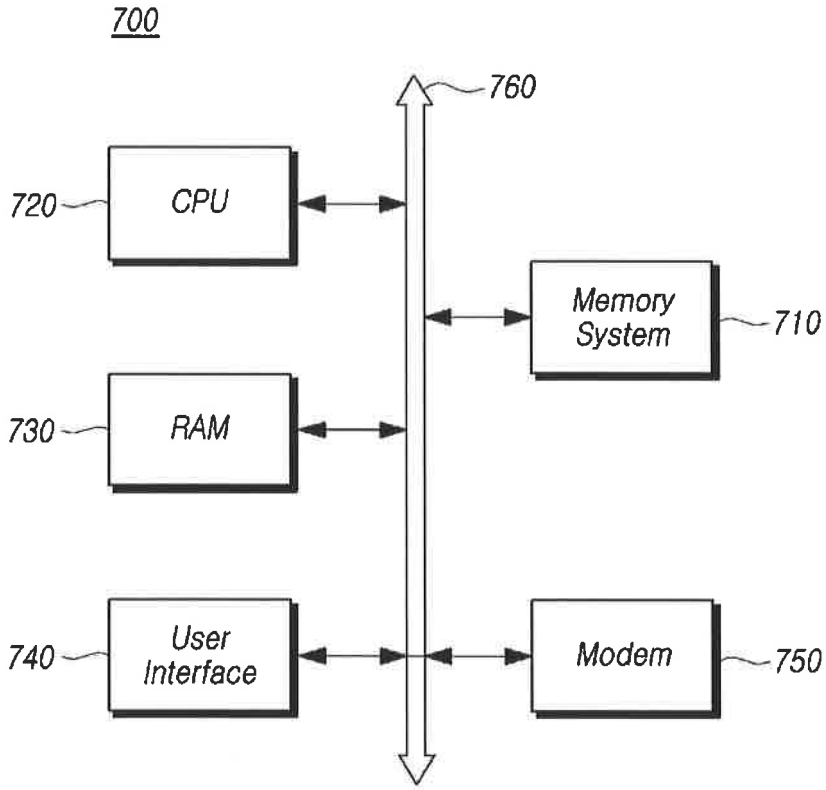

600
621
622
620
610
SRAM
CPU
NVM
Device
Host
Host I/F
ECC
Memory I/F
623
624
625

FIG.25


700
760
720
CPU
Memory System
710
730
RAM
740
User Interface
Modem
750