

An object of the present invention is a device for fusing a fusible element in an integrated circuit of the CMOS type. It can be used in numerous integrated circuits, in particular for defining read only memories or for replacing, by functional redundant circuits, functional circuits which have been put out of action. In memory card applications the fusible elements may also serve to protect, during access, certain memory zones. Before they are fused, the connection which they establish make it possible to program the integrated circuit of the memory card in order to introduce into it secret codes or recognition algorithms. After they are fused this programming and also reading of the said secret codes or the said algorithms become impossible.

In an integrated circuit the fusible elements are mainly formed by connections made of polysilicon or of metal. The sizes of the cross-sections of these connections and the useful fusible length of the fuse are determined in dependence on a nominal fusion current. The principle involved in fusing a fuse is simple. It suffices to pass through the fuse a current sufficiently large to make it blow. In practice this current, in modern integrated circuits, is of the order of several tens of milliamperes. After the fuse has blown, one of the terminals of the fuse, the one which it is desired to make inaccessible, is electrically floating. To avoid such a situation this terminal of the fuse is connected to a level detector. The said level detector is able on the one hand to indicate the fusing of the fuse and, on the other hand, to maintain the floating end of the connection at a constant potential.

However there are problems associated with the fusing of the fuse. First of all, the fusing current must be sufficiently large which necessitates, for routing the current, a very large control transistor. This control transistor serves to facilitate the programming of the fusion of various fuses in a circuit. The size of the transistor is dependent on the current which the said transistor must allow to pass. On the other hand, the rising edge of the current pulse must be very steep. In fact if the rise in current occurs slowly, all things considered, the fuse melts little by little. As it melts its electrical resistance

increases proportionately. In practice, for example, the dimensions of its cross-section may decrease during this fusing. As this resistance increases, the energy which the fuse is able to dissipate decreases. As this energy decreases the fuse heats up less and less and there is a risk that it can no longer fuse. If this situation occurs it is subsequently impossible to make the fuse melt. Lastly, the control of the transistor for routing the current makes it necessary to provide, in the procedure for fusing a fuse, the application of an end of fusing command and this complicates this procedure. In practice, it is necessary to provide a fusion duration. This fusion duration must be relatively long in order to ensure correct fusing in every case.

Fuses are also very susceptible to rupture caused by electrostatic discharges. This fragility is essentially due to the presence of the large transistor for controlling the fusing of the fuse. In practice, because of its size, the said transistor does not provide good protection with respect to high voltage electrostatic discharges, even if its control input is deactivated. It is in fact possible for the large transistor to allow the energy of the electrostatic discharges to pass when the integrated circuit is manipulated, in particular at the end of manufacturing and at the time of installation of the said integrated circuit in an electronic system. These repeated electrostatic discharges may have the same effect as an edge of the fusing current which rises too slowly. At the time when it is desired to melt the fuse the resistance of the latter may be large because of the initiations of fusing to which it has been subjected. The energy which it is then able to dissipate is too small: it no longer fuses.

An aim of the present invention is to overcome these disadvantages whilst, however, only applying to integrated circuits of the CMOS type. This restriction is not a nuisance since at present CMOS technology is increasingly used and in particular it is often preferred to NMOS technology. CMOS technology is characterized by a semiconductor substrate of a given conductivity type (usually of type P) in which insulation islands are formed by implantation of impurities corresponding to an

opposite conductivity type (usually type N). Various transistors and junctions may be formed by the implantation of regions doped with one or other type of impurities either in the substrate or in the said islands.

CMOS technology is however known to suffer from the occurrence of switching over of conduction, known as "latch up" in English publications. This switching over corresponds to a triggering of parasitic thyristors which are created naturally in a CMOS circuit comprising islands. These parasitic thyristors are formed by a succession of regions having alternate types of conductivity. A first region, of a given conductivity type (usually P) is contained in an island of a second given conductivity type (usually N), this island is itself located in a substrate of the first given conductivity type (usually P) and comprises one or more regions of the second given conductivity type (usually N). The succession of these four regions having alternating conductivities constitutes a thyristor the triggering of which in certain cases is very sensitive.

In the invention use has been made of the existence of this parasitic thyristor to melt the fuse by connecting a terminal of the fuse to the thyristor and triggering it. At the time of fusing, the current is supplied by a generator of a fusion potential. The current passes through the fuse and the thyristor, one of the terminals of which is connected to the other terminal of the generator of the fusing potential. Use of a parasitic thyristor for fusing a fuse is described in Patent Abstracts of Japan, Vol.8, No 221 (E-271)[1658], 9.10.1984, page 148. This document describes a device in accordance with the precharacterizing part of claim 1.

On the one hand the thyristor, whilst being of smaller size, withstands a very high current. On the other hand the thyristor conducts as long as the fuse is not completely fused - so long as the fuse allows current to pass. As soon as the fuse is blown the thyristor cuts off, and it is not necessary to provide in the procedure a command for end of fusing.

In the invention a triggering device having a circular structure is proposed. Thus, when the parasitic thyristor is not triggered it provides a much greater protection of the fuse from electrostatic discharges than is obtained in the quoted state of the art.

An object of the invention, therefore, is a device for fusing a fuse in an integrated circuit of the CMOS type of the kind characterized in claim 1. Claims 2 and 3 relate to advantageous embodiments.

The invention will be better understood on reading the following description with reference to the Figures which accompany it. They are given solely by way of non-limiting illustration of the invention. The Figures show:

- Figure 1: a cross-section of an integrated circuit of the CMOS type provided with a parasitic thyristor;
- Figure 2: a diagram equivalent to the circuit represented by this parasitic thyristor;
- Figure 3: a device for triggering a parasitic thyristor having a circular structure in accordance with the invention;
- Figure 4: an alternative embodiment of a triggering circuit not in accordance with the invention;
- Figure 5: a schematic representation of a level detector for checking the fusing state of the fuse;
- Figure 6 : a technological improvement of a pull down transistor in this level detector.

Figure 1 shows a parasitic thyristor of an integrated circuit of the CMOS type. The integrated circuit, not shown, is integrated in a substrate 1, in this case of type P⁻, comprising islands, in particular an island 2 of opposite conductivity: N⁻. Conventionally the substrate 1 includes regions 3 and 4 doped with the same impurities as those which were used to dope the island 2 but in a higher concentration: N⁺. They serve to perform various electronic functions, in particular acting as transistors. The substrate also includes a substrate terminal 5 comprising a region doped with the same impurities but in a higher

concentration, P^+ , than the substrate itself. This substrate terminal serves to bias the substrate to a fixed potential. When the substrate is of type P, this fixed potential V_{ss} is usually zero volts. One of the N^+ doped regions in the substrate, for example in this case the region 3 near the island 2, is also biased to the potential V_{ss} .

The island 2 comprises in a similar manner P^+ regions 6 and 7 doped with different impurities to those which were used to dope the island 2. It also comprises an N^+ region 8 doped with the same impurities as itself which acts as a terminal for the island. Usually an island terminal is biased to an opposite potential to the bias potential of the substrate. In the case of a P type substrate and N type islands, the island is positively biased to V_{cc} . One of the P^+ doped regions in the island, for example in this case the region 6 near the region 3 is also biased to the potential V_{cc} . It can be established that the highly doped regions 3 and 6 on either side of the boundary 9 of the island in the substrate 1, in combination with the island 2 and the substrate 1 constitute a parasitic thyristor of the $P^+ N^- P^- N^+$ type. Access can be obtained to the intermediate regions of the said thyristor through the terminals 8 and 5 of the island and the substrate respectively.

The equivalent circuit to the said thyristor is shown in Figure 2. In the island, the region 6, the island 2 and the substrate 1 form a bipolar transistor T1. In the substrate, the region 3, the substrate 1 and the island 2 form a bipolar transistor T2. Everything happens as if the transistor T1, in this example of PNP type, was connected by its emitter to V_{cc} (in the region 6, Figure 1), and connected by its collector, through the intermediary of the resistors R2 and R3 connected in series, to the substrate terminal 5, and was connected by its base, through the intermediary of a resistor R1, to the island terminal 8. The NPN type transistor T2 may be considered to be connected by its emitter to the region 3, by its collector, through the intermediary of the resistors R1 and R4 connected in series, to the region 8, and by its base, through the intermediary of the resistor R3, to the substrate terminal 5. The bases of these transistors, the points A and B

respectively, are thus connected to the mid-points of resistance bridges R1-R4 and R2-R3 respectively.

At rest the thyristor is not conductive. The potential at the point A is equal to the voltage V_{cc} and the potential at the point B is equal to V_{ss} . The two transistors T1 and T2 are blocked. To trigger the thyristor it suffices to lower the voltage at the point A until the transistor T1 begins to conduct. For example it suffices to lower this voltage by 0.6 volts. This drop in voltage equals the emitter-base of the transistor T1 voltage. As soon as the transistor T1 begins to conduct the voltage at the point B rises because current passes through the resistor R3. As a result, the transistor T2 which was blocked becomes conductive. Because the transistor T2 becomes conductive, current now passes through the resistors R1 and R4. This continues to cause the voltage at the point A to fall and results in a positive reaction. The phenomenon of switching then occurs. The two transistors become saturated causing a very large current (several hundreds of milliamperes) to pass between the supply V_{cc} and the ground potential V_{ss} . Only a switching off or a breakdown of the supply V_{cc} can stop this occurrence.

The idea of the invention is to use a control means to cause a drop in the potential at the point A or, conversely, to cause an increase in the potential at the point B when the thyristor is blocked. The following description corresponds, without it being possible to infer any restriction therefrom, to the said first solution: to lower the voltage at the point A.

Figure 3 shows a cross-section of an embodiment of a circuit for triggering a thyristor in accordance with the invention. In this Figure the fuse 10 has been shown as well as its supply with a fusing potential V_{FUS} which may be specific. Nevertheless, in the invention, because of the greater effectiveness of the thyristor, it is possible to cause the fuses to melt with a smaller voltage than V_{cc} . The device for fusing a fuse is formed with a circular structure centered around an axis 11 situated substantially in line with the the terminal 12 of the fuse

closest to the thyristor. The parasitic triggering thyristor thus comprises a central N^+ doped region 8 surrounded by a P^+ doped circular region 6. The said regions 8 and 6 are contained in the island 2 which likewise is circular and is itself surrounded by a N^+ doped circular region 3 in the substrate. The region 3 is itself contained in another P^+ doped circular region 5. The regions 8, 6, 3 and 5 here have the same functions as those described hereinabove. The regions 3 and 5 are joined by connections 13 and 14 to the substrate polarisation voltage. The two regions 6 and 8 in the island are connected in common to the terminal 12 of the fuse 6 by connections 15 to 17.

An MOS transistor T3 for triggering the thyristor comprises a limitrophe zone 18 of the island 2 near the boundary 9, a zone 19 in the substrate facing the said zone 18 on the other side of the boundary 9, and the annular N^+ doped region 3. This hybrid transistor thus comprises regions of which the respective concentrations of impurities are N^- , P^- and N^+ . A gate 20 superposed above an oxide electrical insulation gate, not shown, is supplied with a command signal COM. The gate 20 bridges over the boundary 9. Effectively it controls the conduction by the transistor T3 in the zone 19. It is without effect on the zone 18 and thus it is not a disadvantage to allow it to extend above this zone 18. At the time of application of a positive pulse to the gate 20, current flows in the transistor T3 thus formed. This current can only come from the island 2. Because of the internal resistance of the semiconductive material of the island 2 (resistor R1), the potential falls in the said island 2. The fall in potential at the point A is thus caused. In order that the effect of triggering the thyristor occurs it is however necessary to arrange that the transistor T3 will ensure a fall in potential of at least 0.6 volts at the point A. For this purpose the resistance R1 must be relatively large and the resistance R4 relatively small. In addition the transistor T3 must itself not be too resistive. Figure 2 shows by dashed lines the method of connection of the transistor T3 in the equivalent circuit to the thyristor.

The arrangement shown in Figure 3 has other great advantages. In particular it means it can protect itself very effectively against electrostatic discharges. Let it be assumed for example that a device for protection against electrostatic discharges greater than 20 volts is connected in parallel to the terminal 21 of the fuse. In the aforementioned state of the art the transistor for fusing the fuse was usually triggered at the same voltage as the protection device (for example by junction avalanche or BVdSS) or even possibly at a lower voltage. This led to deterioration of the fuse or possibly to its unexpected destruction. In the device shown, conduction of the N⁻ P- type junction between the island and the substrate, because of the low concentrations of impurities near this junction, typically occurs at 100 to 150 volts. Under these conditions the device for protecting the fuse is always affected first. It plays its usual role: the fuse cannot be caused to deteriorate.

The device shown in Figure 4, not in accordance with the invention, provides an inferior protection against electrostatic discharges. The transistor for triggering the thyristor is a conventional MOS transistor. It includes a region 22 near the boundary 9 as well as the region 3 situated near the region 22 and having the same concentration of impurities as it has (N⁺). The region 22 is separated from the region 3 by a distance corresponding to the conduction channel of this transistor. This channel is controlled by a gate 23 receiving the command signal COM. The island 2 also includes another, N⁺ doped, region 24 acting as a terminal for the secondary island 2 and connected electrically by a connection 25 to the region 22 of the control transistor. In this alternative embodiment the region 22 is no longer directly connected to the voltage Vss. It is only connected to it under certain conditions: when the COM signal is applied to the gate 23 and when it makes the transistor 3-22 conductive. The control transistor therefore is in this case a conventional MOS transistor.

Before causing the fuse to melt, the voltage present on the connection 25 is substantially the voltage VFUS. When the command for

fusing is applied to the gate 23, the transistor 22-23-3 begins to conduct in such a manner that the voltage at a mid-point C of a voltage divider formed by the resistors R5, R1 falls. At this time no current passes through the resistor R1. However because of the location of the region 24 between the region 8 and the region 6, the fall of the voltage at the point C causes a substantially equal fall of the voltage at the point A in the transistor T1. Under these conditions, the expected effect, the triggering of the thyristor, occurs.

The interesting feature of this device resides in the formation of a transistor 22-23-3 of conventional type in contrast to the hybrid transistor 18-19-3 in Figure 3. However, in this alternative embodiment the protection against electrostatic discharges is less reliable. In fact an electrostatic discharge may make use of a pathway passing successively through the connection 16, the region 8, the island 2, the region 24, the connection 25 and the region 22 before passing to ground by avalanche of the junction 22-1 and BVdSS of the control transistor. Under these conditions it is the junction 22-1 and the length of the channel of the transistor T3 which ensures the maintenance of the voltage against this discharge. Because the region 22 is highly doped, the potential barrier of this junction is smaller. There is therefore a disadvantage of the same type, from this point of view, as in the aforementioned state of the art.

There can be a very large number of circuits for detecting the state of the fuse. Figure 5 shows one example. This circuit substantially comprises a pull down transistor T4 and a detection inverter including two transistors 26, 27. The transistors 26 and 27 are connected in series between the supply Vcc of the integrated circuit and ground. When the detection inverter detects the change in state of the fuse it switches over. The output 28 of the level detector is connected to the middle point of the two transistors 26 and 27. These two transistors are controlled in common, through the intermediary of a resistor R6, by a voltage available at the terminals of a transistor T4. The transistor T4 is connected in parallel to the terminals of the transistor T3 and it

receives the potential V_{cc} on its gate. When the fuse has melted, when the command COM has stopped, the transistor T4 causes the input to the transistors 26 and 27 to be connected to ground. The transistor 27 is then blocked, whereas the transistor 26 is conductive. The output 28 is brought to the potential V_{cc} . The presence of the resistor R6 serves to protect the fuse 10 against electrostatic discharges which could pass through the transistors 26 or 27. At the time of such a discharge a large potential difference is developed in the resistor R6 so that the potential barrier of the transistor 27 is sufficient to resist the remainder of this electrostatic discharge. On the other hand this cannot be envisaged with the transistor T4 which is almost always conductive nor with the transistor T3 in the alternative embodiment in Figure 4.

In order nevertheless to achieve this objective, these two transistors may be formed in the manner shown in Figure 6. Preferably the transistors T3 and T4 comprise a gate 29 which controls a conduction channel between two N^+ doped regions 30 and 31. One of their regions, the region 31 which is spatially nearest the thyristor in the substrate 1, is implanted in an N^- doped island 32. Because of the low concentration of impurities in the island 32 the $N^- P^-$ junction between this island and the substrate resists electrostatic discharges. A potential difference of 150 volts may for example be withstood (in practice however it may be limited by the breakdown of the oxide of the gate between the region 32 and the gate 29 to about 50 volts). The length of the channel must however be sufficient to avoid passage by premature breakdown of the transistor T4.

CLAIMS

1. A device for fusing a fuse in an integrated circuit of the CMOS type comprising a thyristor in series with the fuse and means for controlling the switching on of the thyristor comprising an MOS transistor the control gate of which is connected to a thyristor control signal, characterized in that this device has a circular structure, the thyristor comprising:

- an integrated circuit substrate (1) of a first conductivity type,
- an island (2) of a second conductivity type formed in the substrate,

- a first region (8), in the centre of the island, having the same conductivity type as but being more highly doped than the island,

- a second region (6) in the island having the same conductivity type as but being more highly doped than the substrate, this second region (6) surrounding the central region (8),

- a third region (3) in the substrate, having the same type of conductivity as but being more highly doped than the island, this third region (3) surrounding the island,

- a fourth region (5) in the substrate having the same type of conductivity as but being more highly doped than the substrate, this fourth region (5) surrounding the region (3), the first region (8) and the second region (6) being connected to a terminal (12) of the fuse, the third region (3) and the fourth region (5) being connected in common to a polarisation voltage (14) of the substrate,

the MOS transistor (T3) being formed by the alignment of a zone (18) of the island adjacent to the boundary (9) between the island and the substrate, of a zone (19) in the substrate adjacent to the said boundary (9) and of the third region (3) of the thyristor, the control gate (20) being located above, bridging the boundary (9).

2. A device as claimed in claim 1, characterized in that the thyristor is of the parasitic type in the integrated circuit.

3. A device as claimed in claim 1 or claim 2, having a detection circuit connected to the terminal (12) of the fuse connected to the thyristor, for detecting fusing of the fuse and for forcing the potential at the terminal (12) of the fuse, and comprising a pull-down transistor (T4) connected in series between this terminal (12) of the fuse and ground, this pull-down transistor (T4) being characterized in that it is connected in parallel to the terminals of the MOS transistor (T3) and in that it comprises two regions having the second conductivity type formed in the substrate (1) having the first conductivity type, that one of the two regions which is spatially closer to the thyristor being formed in a region which is larger than it is and which has the same conductivity type as it has but is less highly doped.

