

**IMPLEMENTATION ARCHITECTURE FOR
PERFORMING HIERARCHICAL MOTION
ANALYSIS OF IMAGES IN REAL TIME**

ABSTRACT

First hardware means, comprising a given number of prior-art image-pyramid stages (406-1, 406-n), together with second hardware means, comprising the same given number of novel motion-vector stages (416-1, 416-n), perform cost-effective hierarchical motion analysis (HMA) in real time, with minimum system processing delay and/or employing minimum hardware structure. Specifically, the first and second hardware means, in response to relatively high-resolution image data from an ongoing input series of successive given pixel-density image-data frames that occur at a relatively high frame rate (e.g., 30 frames per second), derives, after a certain processing-system delay, an ongoing output series of successive given pixel-density vector-data frames that occur at the same given frame rate. Each vector-data frame is indicative of image motion occurring between each pair of successive image frames.

FIGURE 4

