substrate. In some embodiments, the die element is ready for bonding to said further substrate without a requirement for further cutting of the die element to decrease the size of its footprint.

The term also includes reference to an integrated circuit formed directly on a substrate that is ready to be bonded to a further integrated circuit on a wafer without cutting of said substrate.

In a second aspect of the invention there is provided a structure comprising: an integrated circuit wafer having a plurality of integrated circuits formed thereon, each of said wafer integrated circuits being provided with a plurality of wafer contact elements; a plurality of die elements on said wafer, each die element having a plurality of die contact elements at locations corresponding to locations of said wafer contact elements; and a positioning member, the positioning member being provided in juxtaposition with said wafer and having a plurality of formations at locations of the positioning member corresponding to locations of said plurality of wafer integrated circuits, said formations defining respective sets of lateral boundaries arranged to constrain movement of a die element provided on said wafer within a set of said boundaries, respective corresponding contact elements of the wafer and die element being bonded to one another by means of a diffusion bond.

In a third aspect of the invention there is provided a positioning member for use in positioning a plurality of die elements on a wafer, the wafer having a plurality of wafer integrated circuits provided thereon, said integrated circuits each having a plurality of contact elements, said die elements each having a plurality of die contact elements provided thereon, with the positioning member provided in predetermined juxtaposition with said wafer, the positioning member having a plurality of formations at locations of the positioning member corresponding to locations of said plurality of wafer integrated circuits, said formations defining respective sets of lateral boundaries arranged to constrain movement of respective die elements provided on the wafer surface such that respective corresponding contact elements of the wafer integrated circuits and die elements are aligned with one another.

In an embodiment~~a fourth aspect~~ of the invention there is provided a 3D integrated circuit structure comprising a wafer integrated circuit cut from a wafer and a die element, the wafer integrated circuit having a set of wafer integrated circuit contact elements formed