

Abstract of the Disclosure

TITLE: SEMICONDUCTOR MEMORY

A plurality of information memory cells and a single reference memory cell are coupled to a single word line. The reference memory cell stores reference information equivalent to a reference potential to information readout. Pieces of information, stored in the information memory cells, are fed, over respective bit lines, to first input terminals of sense amplifiers. The reference information, stored in the reference memory cell, is fed, over a bit line, to second input terminals of the sense amplifiers. When the potential of signal charges stored in the information memory cells falls due to leakage current, the potential of a signal charge stored in the reference memory cell correspondingly falls due to leakage current. This prolongs a length of time taken for a difference between these potentials to reach a sense limit, thereby achieving a longer data retention time. As a result of such arrangement, even when there occurs a small current leakage from memory cells, it is possible to secure a long data retention time thereby making it possible to obtain a long refresh cycle period.

Figure 1.



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