ABSTRACT

A METHOD TO FORM A HIGH K DIELECTRIC GATE INSULATOR LAYER, A METAL GATE STRUCTURE, AND SELF-ALIGNED CHANNEL REGIONS, POST SOURCE/DRAIN FORMATION

A process of fabricating a sub-micron MOSFET device, featuring a high dielectric constant gate insulator layer, and a metal gate structure, has been developed. Processes performed at temperatures detrimental to the high dielectric, gate insulator layer, such as formation of spacers on the sides of subsequent gate structures, as well as formation of source/drain regions, are introduced prior to the formation of the high dielectric, gate insulator layer. This is accomplished via use of a dummy gate structure, comprised of silicon nitride, used as a mask to define the source/drain regions, and used as the structure in which sidewall spacers are formed on. After selective removal of the dummy gate structure, creating an opening in an interlevel dielectric layer exposing the MOSFET channel region, deposition of the high dielectric, gate insulator layer, on the surface of the MOSFET channel region, is performed.

FIGURE 1 IS SUGGESTED FOR PUBLICATION