CLAIMS

The invention claimed is:

1. A floating body transistor construction comprising a U-shaped semiconductor material; the U-shape having a pair of limbs joined to a central portion; each of the limbs containing a source/drain region of a pair of gatedly-coupled source/drain regions; and the floating body of the transistor extending across the central portion between the source/drain regions.

2. The construction of claim 1 further comprising electrically insulative material filling the U of the U-shaped semiconductor material.

3. The construction of claim 2 wherein the electrically insulative material comprises silicon dioxide.

4. The construction of claim 2 wherein the electrically insulative material consists of silicon dioxide.

5. The construction of claim 1 wherein the semiconductor material comprises monocrystalline silicon.

6. The construction of claim 1 wherein the semiconductor material consists of monocrystalline silicon.

7. The construction of claim 1 wherein the semiconductor material is a planar expanse; and further comprising a planar gate on one side of the semiconductor material expanse.

8. The construction of claim 7 further comprising gate oxide between the planar gate and the semiconductor material expanse.

9. The construction of claim 7 wherein the planar gate comprises one or more metals.

10. The construction of claim 7 wherein the planar gate comprises one or more of titanium, ruthenium and titanium nitride.

11. The construction of claim 1 wherein the semiconductor material is a planar expanse; and further comprising a planar front gate on one side of the semiconductor material expanse, and a planar back gate on an opposing side of the semiconductor material expanse.

12. The construction of claim 11 wherein the front gate and the back gate are identical in composition to one another.

13. The construction of claim 12 wherein the composition includes one or more metals.

14. The construction of claim 12 wherein the composition includes one or more of titanium, ruthenium and titanium nitride.

15. The construction of claim 11 further comprising:

first gate oxide between the front gate and the semiconductor material expanse; and

second gate oxide between the back gate and the semiconductor material expanse.

16. A semiconductor construction comprising:

an electrically conductive plate;

an expanse of semiconductor material adjacent the plate, and spaced from the plate by one or more dielectric materials; the expanse having a pair of prongs extending from a base portion; the prongs comprising conductively-doped regions;

an insulative material between the prongs; and

a floating body transistor comprising at least a portion of the semiconductor material and at least a portion of the plate, the conductively-doped regions of the prongs being source/drain regions of the transistor, the plate comprising a gate of the transistor, and the base portion of the expanse comprising the floating body of the transistor.

17. The construction of claim 16 wherein the insulative material comprises silicon dioxide.

18. The construction of claim 16 wherein the insulative material consists of silicon dioxide.

19. The construction of claim 16 wherein the semiconductor material comprises monocrystalline silicon.

20. The construction of claim 16 wherein the semiconductor material consists of monocrystalline silicon.

21. The construction of claim 16 wherein the one or more dielectric materials include silicon dioxide.

22. The construction of claim 16 wherein the one or more dielectric materials consist of silicon dioxide.

23. The construction of claim 16 wherein the plate comprises one or more metals.

24. The construction of claim 16 wherein the plate comprises one or more of titanium, ruthenium and titanium nitride.

25. A semiconductor construction comprising:

a series of electrically conductive plates; the plates alternating between front gate plates and back gate plates; and

a plurality of expanses of trough-shaped semiconductor material; individual expanses being between front gate plates and back gate plates; the individual expanses comprising a pair of upwardly-projecting sidewalls joining to a central valley portion; the sidewalls comprising transistor source/drain regions and the central portions comprising floating body regions of floating body transistors.

26. The construction of claim 25 wherein:

the floating body transistors are within a memory array;

at least some of the individual front gates are shared between pairs of floating body transistors on opposing sides of the individual front gate plates; and

at least some of the individual back gates are shared between pairs of floating body transistors on opposing sides of the individual back gate plates.

27. The construction of claim 25 further comprising electrically insulative material filling the troughs of the trough-shaped expanses.

28. The construction of claim 27 wherein the insulative material comprises silicon dioxide.

29. The construction of claim 27 wherein the insulative material consists of silicon dioxide.

30. The construction of claim 25 wherein the semiconductor material comprises monocrystalline silicon.

31. The construction of claim 25 wherein the front gate plates are separated from the semiconductor material by first gate dielectric; wherein the back gate plates are separated from the semiconductor material be second gate dielectric; and wherein the first and second gate dielectrics are the same composition as one another.

32. The construction of claim 31 wherein the first and second gate dielectrics include silicon dioxide.

33. The construction of claim 31 wherein the first and second gate dielectrics consist of silicon dioxide.

34. The construction of claim 25 wherein the back gate plates are the same composition as the front gate plates.

35. The construction of claim 25 wherein the back gate plates are the same composition as the front gate plates; and wherein the plates comprise one or more metals.

36. The construction of claim 25 wherein the back gate plates are the same composition as the front gate plates; and wherein the plates comprise one or more of titanium, ruthenium and titanium nitride.

37. A semiconductor construction comprising:

a series of electrically conductive plates; the plates alternating between front gate plates and back gate plates;

an array of floating body transistors, with columns of the transistor array being between front gate plates and back gate plates; each of the individual transistors along the columns having a source region and a drain region; the source and drain regions of the transistors alternating with one another along the columns of the array; and

the source regions being tied to one another along diagonals extending about 45 degrees to the columns of the array.

38. The construction of claim 37 wherein the transistors comprise expanses of trough-shaped semiconductor material; individual expanses being between front gate plates and back gate plates; the individual expanses comprising a pair of upwardly-projecting sidewalls joining to a central valley portion; the sidewalls comprising the transistor source and drain regions, and the central portions comprising floating body regions of the floating body transistors.

39. A method of forming a semiconductor construction, comprising:

providing a substrate;

forming a plurality of separate trough-shaped structures of semiconductor material over the substrate; the individual trough-shaped structures comprising a pair of upwardly-projecting sidewalls joined to a valley;

filling the valleys of the trough-shaped structures with insulative material;

forming a plurality of electrically conductive gatelines extending through the trough-shaped structures to subdivide the trough-shaped structures into a plurality of trough-shaped slices sandwiched between pairs of the conductive gatelines; and

incorporating paired conductive gatelines and the trough-shaped slices therebetween into floating body transistors.

40. The method of claim 39 wherein the upwardly-projecting sidewalls of the trough-shaped structures are capped with one or more sacrificial materials, and further comprising, after forming the electrically conductive gatelines:

removing the one or more sacrificial materials; and

growing additional semiconductor material over the upwardly projecting sidewalls to extend the upwardly-projecting sidewalls of the trough-shaped slices.

41. The method of claim 40 wherein the one or more sacrificial materials comprise a silicon nitride-containing layer over a silicon dioxide-containing layer.

42. The method of claim 40 wherein the one or more sacrificial materials consist of a layer of silicon nitride over a layer of silicon dioxide.

43. The method of claim 39 further comprising forming source regions and drain regions within the upwardly-projecting sidewalls of the trough-shaped slices; each slice comprising a source region within one sidewall, and a drain region within the other sidewall.

44. The method of claim 43 wherein the upwardly-projecting sidewalls of the trough-shaped structures are capped with one or more sacrificial materials, and further comprising, after forming the electrically conductive gatelines:

removing the one or more sacrificial materials;

growing additional semiconductor material over the upwardly projecting sidewalls to extend the upwardly-projecting sidewalls of the trough-shaped slices; and

forming the source and drain regions within the extended upwardly-projecting sidewalls.

45. The method of claim 39 wherein the conductive gatelines are alternating front gatelines and back gatelines; and further comprising electrically connecting all of the back gatelines to one another.

46. The method of claim 39 wherein the semiconductor material comprises monocrystalline silicon.

47. The method of claim 39 wherein the insulative material comprises silicon dioxide.

48. The method of claim 39 wherein the insulative material consists of silicon dioxide.

49. The method of claim 39 wherein the substrate comprises an insulator over a semiconductor base; and wherein the trough-shaped structures are formed to be directly against the insulator.

50. The method of claim 49 wherein the insulator consists of silicon dioxide; and wherein the semiconductor base comprises of monocrystalline silicon.

51. The method of claim 39 wherein the conductive gatelines comprise one or more metals.

52. The method of claim 39 wherein the conductive gatelines comprise one or more of titanium, ruthenium and titanium nitride.

53. A method of forming a semiconductor construction, comprising:

providing a substrate comprising semiconductor material over an electrically insulative mass, the semiconductor material having a thickness;

forming a plurality of first trenches extending into the semiconductor material, but not entirely through the thickness of the semiconductor material; the first trenches extending primarily linearly along defined latitudinal directions;

forming one or more second trenches which extend entirely through the semiconductor material and into the insulative mass; the forming of the second trenches leaving a plurality of spaced regions of the semiconductor material extending along and under the first trenches; the individual spaced regions of semiconductor material being trough-shaped with sidewalls of the troughs being along opposing sides of the first trenches, and bottoms of the troughs being under the first trenches;

filling the second trenches with electrically insulative material;

forming a plurality of third trenches extending primarily linearly along longitudinal directions substantially orthogonal to the latitudinal directions, the third trenches extending across the trough-shaped regions of the semiconductor material and across the electrically insulative material, and thus having peripheries comprising insulative material regions and semiconductor material regions; the third trenches dividing the trough-shaped semiconductor material into trough-shaped slices;

lining the semiconductor material regions of the third trench peripheries with dielectric material;

after the lining, forming conductive material within the third trenches;

conductively doping at least portions of the sidewalls of the trough-shaped regions of the semiconductor material; and

wherein the conductive material within the third trenches forms a plurality of front-gate/back-gate pairs, with each pair sandwiching a single of the trough-shaped slices therebetween; each sandwich of a front-gate/trough-shaped semiconductor material slice/back-gate being a floating body transistor unit cell.

54. The method of claim 53 wherein the conductively-doped portions of the sidewalls are source and drain regions; and wherein each trough-shaped semiconductor material slice has a source region in one sidewall of the slice and a drain region in the other sidewall of the slice.

55. The method of claim 54 further comprising electrically interconnecting pluralities of the source regions along directions extending diagonally to the longitudinal and latitudinal directions.

56. The method of claim 54 further comprising electrically interconnecting pluralities of the drain regions along a common latitudinal direction.

57. The method of claim 54 further comprising:

electrically interconnecting pluralities of the source regions along directions extending diagonally to the longitudinal and latitudinal directions with source interconnect lines; and

electrically interconnecting pluralities of the drain regions along common latitudinal directions with bitlines.

58. The method of claim 57 wherein the bitlines are over the source interconnect lines.

59. The method of claim 53 wherein the third trenches extend into but not through the insulative mass.

60. The method of claim 53 wherein forming the conductive material within the third trenches only partially fills the third trenches to leave upper portions of the third trenches which are not filled; and further comprising forming electrically insulative caps within the upper portions of the third trenches.

61. The method of claim 60 wherein the electrically insulative caps comprise silicon nitride.

62. The method of claim 60 wherein the forming the conductive material to only partially fill the third trenches comprises:

forming the conductive material to completely fill the third trenches; and

recessing the conductive material within the third trenches to form the unfilled upper portions of the third trenches.

63. The method of claim 53 wherein the first trenches are formed before the second trenches.

64. The method of claim 53 wherein the first trenches are filled with the insulative material during the filling of the second trenches with the insulative material.

65. The method of claim 64 wherein the insulative material comprises silicon dioxide.

66. The method of claim 64 wherein the insulative material consists of silicon dioxide.

67. The method of claim 53 further comprising electrically connecting all of the back-gates to one another.

68. The method of claim 53 wherein the semiconductor material comprises monocrystalline silicon.

69. The method of claim 53 wherein the insulative mass is over a semiconductor base; wherein the insulative mass consists of silicon dioxide; and wherein the semiconductor base comprises monocrystalline silicon.

70. The method of claim 53 wherein the conductive material comprises one or more metals.

71. The method of claim 53 wherein the conductive material comprises one or more of titanium, ruthenium and titanium nitride.

CLAIMS

1. A method of forming a semiconductor construction, comprising:

providing a substrate comprising first semiconductor material over an electrically insulative mass, the first semiconductor material having a thickness;

providing a patterned mask over the first semiconductor material, the mask comprising a layer of silicon nitride over a layer of silicon dioxide;

forming a plurality of first trenches extending into the first semiconductor material, but not entirely through the thickness of the first semiconductor material; the first trenches being U-shaped and extending primarily linearly along defined latitudinal directions;

forming one or more second trenches which extend entirely through the first semiconductor material and into the insulative mass; the forming of the second trenches leaving a plurality of spaced regions of the first semiconductor material extending along and under the first trenches; the individual spaced regions of first semiconductor material being trough-shaped with sidewalls of the troughs being along opposing sides of the first trenches, and bottoms of the troughs being under the first trenches;

overfilling the second trenches with electrically insulative material;

planarizing the electrically insulative material by polishing utilizing the layer of silicon nitride as a stop during the polishing;

after filling the second trenches, forming a plurality of third trenches entirely through the first semiconductor material and into the insulative mass extending primarily linearly along longitudinal directions substantially orthogonal to the latitudinal directions, the third trenches extending across the trough-shaped regions of the first semiconductor material and across the electrically insulative material, and thus having peripheries comprising insulative material regions and first semiconductor material regions; the third trenches dividing the trough-shaped first semiconductor material into trough-shaped slices;

lining the first semiconductor material regions of the third trench peripheries with dielectric material;

after the lining, forming conductive material within the third trenches;

removing the patterned mask and replacing the mask with a second semiconductor material, the second semiconductor material being the same composition as the first semiconductor material;

conductively doping the second semiconductor material to form source regions and drain regions;

conductively doping at least portions of the sidewalls of the trough-shaped regions of the first semiconductor material; and

wherein the conductive material within the third trenches forms a plurality of front-gate/back-gate pairs, with each pair sandwiching a single of the trough-shaped slices therebetween; each sandwich of a front-gate/trough-shaped first semiconductor material slice/back-gate being a floating body transistor unit cell.

2. A method of forming a semiconductor construction, comprising:

providing a substrate comprising first semiconductor material over an electrically insulative mass, the first semiconductor material having a thickness;

providing a patterned mask comprising silicon dioxide and silicon nitride over the first semiconductor material;

forming a plurality of first trenches extending into the first semiconductor material, but not entirely through the thickness of the first semiconductor material; the first trenches being U-shaped and extending primarily linearly along defined latitudinal directions;

forming one or more second trenches which extend entirely through the first semiconductor material and into and about half way through the insulative mass; the forming of the second trenches leaving a plurality of spaced regions of the first semiconductor material extending along and under the first trenches; the individual spaced regions of first semiconductor material being trough-shaped with sidewalls of the troughs being along opposing sides of the first trenches, and bottoms of the troughs being under the first trenches;

overfilling the second trenches with electrically insulative material;

planarizing the electrically insulative material utilizing the mask as a stop;

after filling the second trenches, forming a plurality of third trenches entirely through the first semiconductor material and about half way through the insulative mass extending primarily linearly along longitudinal directions substantially orthogonal to the latitudinal directions, the third trenches extending across the trough-shaped regions of the first semiconductor material and across the electrically insulative material, and thus having peripheries comprising insulative material regions and first semiconductor material regions; the third trenches dividing the trough-shaped first semiconductor material into trough-shaped slices;

lining the first semiconductor material regions of the third trench peripheries with dielectric material;

after the lining, forming conductive material within the third trenches;

removing the patterned mask and replacing the mask with a second semiconductor material, the second semiconductor material being the same composition as the first semiconductor material;

conductively doping the second semiconductor material to form source regions and drain regions;

conductively doping at least portions of the sidewalls of the trough-shaped regions of the semiconductor material;

wherein the conductive material within the third trenches forms a plurality of front-gate/back-gate pairs, with each pair sandwiching a single of the trough-shaped slices therebetween; each sandwich of a front-gate/trough-shaped first semiconductor material slice/back-gate being a floating body transistor unit cell;

wherein the conductively-doped portions of the sidewalls are part of source and drain regions; and

wherein each trough-shaped semiconductor material slice has a source region in one sidewall of the slice and a drain region in the other sidewall of the slice.

3. The method of claim 2 further comprising electrically interconnecting pluralities of the source regions along directions extending diagonally to the longitudinal and latitudinal directions.

4. The method of claim 2 further comprising electrically interconnecting pluralities of the drain regions along a common latitudinal direction.

5. The method of claim 2 further comprising:

electrically interconnecting pluralities of the source regions along directions extending diagonally to the longitudinal and latitudinal directions with source interconnect lines; and

electrically interconnecting pluralities of the drain regions along common latitudinal directions with bitlines.

6. The method of claim 5 wherein the bitlines are over the source interconnect lines.

7. The method of claim 1 wherein forming the conductive material within the third trenches only partially fills the third trenches to leave upper portions of the third trenches which are not filled; and further comprising forming electrically insulative caps within the upper portions of the third trenches.

8. The method of claim 1 wherein the first trenches are filled with the insulative material during the filling of the second trenches with the insulative material.

9. The method of claim 1 further comprising electrically connecting all of the back-gates to one another.

10. The method of claim 1 wherein the insulative mass is over a semiconductor base; wherein the insulative mass consists of silicon dioxide; and wherein the semiconductor base comprises monocrystalline silicon.