TITLE OF THE INVENTION

Lift Off Gate MOS Device

BACKGROUND OF THE INVENTION

The present invention relates generally to lift off gate metal oxide semiconductor (MOS) devices including lateral double diffused metal oxide semiconductor field effect transistors (LDMOSFETs) and vertical double diffused metal oxide semiconductor (VDMOS) devices and, more particularly, to an improved MOS device having a graded lift off gate structure which is fabricated using standard processes and which provides enhanced performance in high frequency, particularly radio frequency (RF) integrated circuit power applications.

The use of LDMOSFET's in intelligent power applications is well known. LDMOSFET's are becoming increasingly important in high frequency power devices, particularly in wireless personal communication service systems. Such applications require high trans-conductance and high blocking voltage with minimal parasitic capacitance.

Figs. 1 and 2 are diagrammatic representations of the structure of a conventional LDMOSFET 10. The LDMOSFET 10 is comprised of a standard P-type silicon substrate 12 with standard N-type source and drain silicon areas 14, 16 and with standard source metal 18, gate metal 20 and drain 22 electrodes. A layer of oxide 24 is imposed between the substrate 12 and the gate 20 in the channel region 26. The gate oxide layer 24 is of a generally uniform thickness typically about 600-1000 Angstroms. A thin gate oxide 24 is used to provide the desired high transconductance of the

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channel region 26. However, the use of a thin gate oxide layer 24 leads to increased gate-drain parasitic capacitance, shown schematically as capacitor Crss and increased gate-source parasitic capacitance Ciss (see Fig. 2). The thinness of the gate oxide layer 24 also results in the creation of a high electric field near the edge 28 of the gate 20 closest to the drain 22 due to electric field crowding. The high electric field results in a decrease in the breakdown voltage. An increase in the thickness of the gate oxide layer 24 would increase the breakdown voltage but would seriously deteriorate transconductance of the channel region 26.

Fig. 3 is a diagrammatic representation of a portion of an improved LDMOSFET 110 which was designed to provide high transconductive without significantly diminishing the breakdown voltage. The LDMOSFET 110 has a structure which in most respects is the same as the conventional LDMOSFET 10 described above in connection with Figs. 1 and 2. In particular, the LDMOSFET 110 is comprised of a standard P-type silicon substrate 112 with standard N-type source and drain silicon areas 114 and 116 and with standard source metal (not shown) gate metal 120 and drain (not shown) electrodes. However, unlike the gate 20 of LDMOSFET 10 which is generally rectangular in cross section with a generally uniform thickness, the gate 120 is generally step-shaped in cross section and includes a first generally rectangular area 120a which is of a first uniform thickness and a second generally rectangular shaped area 120b which is of a second general uniform thickness and is offset from the first area 120a in a step-like arrangement as shown in Fig. 3. The oxide layer between the step gate 120 and the substrate 112 is also generally step-shaped in cross section and includes a first relatively thin area 124a and a second, relatively thicker area 124b. The first, thin gate oxide layer 124a is located between the first generally rectangular gate area 120a and the substrate in the channel region 126. The second, thicker gate oxide layer 124b is located between the second rectangular gate area 124b and the substrate 112. As with the conventional LDMOSFET of Fig. 1, the first, thin gate oxide area 124a has a thickness of approximately 350 Angstroms whereas the second thicker gate oxide area 124b has a thickness of approximately 620

Angstroms. By keeping the first gate oxide area 124a thin, high transconductance of the channel region 126 is maintained. However, by making the second gate oxide area 124b substantially thicker, the gate oxide can distribute more potential drop and therefore significantly reduce the electric field crowding in the silicon beneath the second gate oxide layer 124b and increase the breakdown voltage. Further details concerning the structure and operation of the LDMOSFET 110 illustrated in Fig. 3 are available from an article entitled "A Novel LDMOS Structure With A Gate Step Oxide" by Der-Gao Lin, S. Larry Tu, Yee-Chaung See and Pak Tam, which can be found in the IEEE Tech. Dig. IEDM (1995) at pages 963-966, which is incorporated herein by reference.

While the LDMOSFET 110 as shown in Fig. 3 has been demonstrated to provide enhanced performance in some power applications, the fabrication of the LDMOSFET 110 involves substantial additional processing steps which significantly increase fabrication complexity and cost. In addition, the step gate 120 requires a pattern inside the gate which is very difficult for short gate devices. However, in many high frequency RF devices, a short gate length is required for compatibility. Thus, the LDMOSFET 110 is not suitable for many high frequency power applications.

The present invention comprises an improved LDMOSFET with a lift off gate which can be made without the increased fabrication complexity and cost of the step gate device of Fig. 3. In particular, an LDMOSFET in accordance with the present invention provides higher transconductance of the channel region while also keeping the high blocking voltage of a conventional LDMOSFET. An LDMOSFET in accordance with the present invention can be fabricated without the additional processing steps required for fabricating the step-type LDMOSFET 110 and no special gate area patterning is required. Moreover, with the LDMOSFET of the present invention, a very short gate length may be employed, making the LDMOSFET of the present invention capable of achieving the high frequency compatibility necessary in RF devices for high frequency power applications.

BRIEF SUMMARY OF THE INVENTION

Briefly stated, the present invention comprises an improved lift off gate metal oxide semiconductor device which includes a silicon substrate, a source, a drain and a gate, the gate being spaced from the peripheral surface of the substrate in a channel region by an oxide layer. The improvement comprises that the peripheral portions of the gate which are oriented toward the substrate are graded for lift off and the portions of the oxide layer proximate the graded gate portions are graded in a complimentary manner. In this manner, the thickness of the oxide layer proximate the graded gate portions is greater than the thickness of the oxide layer proximate the ungraded portion of the gate. The thinner portion of the oxide layer proximate the ungraded gate portion provides for high transconductance of the channel region. The graded peripheral portions of the gate and the thicker oxide layer proximate the graded portions of the gate provide for less electric field crowding and increased breakdown voltage. Moreover, the thicker oxide layer proximate the graded gate portions results in reduced Crss and Ciss which improves high frequency performance. The present invention further comprises a method of fabricating such a device employing standard lift oxidation technology and by forming the P-body by a high temperature drive-in step using oxygen as the ambient gas.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The foregoing summary, as well as the following detailed description of preferred embodiments of the invention, will be better understood when read in conjunction with the appended drawings. For the purpose of illustrating the invention, there is shown in the drawings embodiments which are presently preferred. It should be understood, however, that the invention is not limited to the precise arrangements and instrumentalities shown. In the drawings:

Fig. 1 is a cross-sectional view of a conventional LDMOSFET;

Fig. 2 is an enlarged cross-sectional view of a portion of the conventional LDMOSFET of Fig. 1;

Fig. 3 is an enlarged cross-sectional view of a portion of a step-gate LDMOSFET in accordance with the prior art;

Fig. 4 is an enlarged cross-sectional view of a portion of an LDMOSFET made in accordance with a preferred embodiment of the present invention; and

Fig. 5 is a greatly enlarged transmission electron microscope (TEM) image of the fabricated lift off gate portion of the LDMOSFET of Fig. 4.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 4 is an enlarged cross-sectional view of a portion of an LDMOSFET 210 in accordance with a preferred embodiment of the present invention. It should be understood that while a description of an improved LDMOSFET is set forth below the present invention is not limited to an LDMOSFET but is also applicable to a VDMOSFET. Fig. 4 illustrates only the portion of the LDMOSFET 210 proximate to the gate 220. However, it will be appreciated by those of ordinary skill in the art that the LDMOSFET 210 has an overall structure which, except for the differences as described below, is substantially the same as the conventional LDMOSFET 10 as shown in Fig. 1. In particular, the LDMOSFET 210 is comprised of a standard P-type silicon substrate 212 with standard N-type source and drain silicon areas and with standard source metal (not shown), gate 220 and drain (not shown) electrodes which are positioned in substantially the same manner as in the conventional LDMOSFET 10. However, unlike the gate 20 of the conventional LDMOSFET 10 which is generally rectangularly shaped in cross section with a corner or sharp edge 28 facing the drain, the gate 220 of the LDMOSFET 210 in accordance with the present invention, although generally rectangular includes lowermost edges 220a and 220b which are generally graded, beveled or smoothly curved to provide a bird-beak shape as shown in Fig. 4. In this manner the edges 220a, 220b of the gate 220 avoid a small sharp, prominent area for the concentration of electric fields. The graded edges 220a and 220b extend upwardly along the thickness of the gate 220 to a boundary 220d. The

gate oxide layer 224, in general, is substantially thicker than the gate oxide layer 24 of the conventional LDMOSFET 10. However, a portion 224a of the gate oxide layer 224 between the ungraded portion of the gate 220c and the substrate 212 includes a substantially reduced thickness and is shaped in a manner which is complementary to the shape of the gate 220. Preferably the reduced thickness portion 224a of the gate oxide layer 224 is about 300 Angstroms thick but could be ⅛ to ½ of the thickness of the gate oxide layer 224 and, as shown, is preferably above the channel region 226 of the substrate 212. Preferably, the thickness of the remainder of the gate oxide layer 224, particularly in the area around the graded edges 220a, 220b of the gate 220, is about 1,000 Angstroms but could be in the range of 100 to 1,110 Angstroms. The thinner portion 224a of the gate oxide layer 224 provides high transconductance of the channel region 226. Correspondingly, the thicker portion of the gate oxide layer 224 proximate the edges 220a, 220b of the gate 220 distributes the potential drop over a larger area than if the edges were as sharp as the edges of a conventional LDMOSFET as shown in Fig. 1. The resulting reduction in the electric field concentration or crowding in the silicon beneath the gate oxide layer 224 substantially increases the breakdown voltage and reduces the gate-drain parasitic feedback capacitance (Crss). No special gate area patterning is required for the LDMOSFET 210 and, therefore, it is suitable for any gate length, making the LDMOSFET 210 particularly useful for high frequency RF devices.

The graded gate structure of the improved LDMOSFET 210 can be fabricated using standard lift oxidation techniques after polysilicon patterning. In forming a conventional LDMOSFET, the P-type body is formed by a high temperature drive-in step with nitrogen as the ambient gas. To fabricate the graded lift off gate LDMOSFET, oxygen is used or partially used instead of nitrogen as the ambient gas for the high temperature drive-in step. The oxygen oxidizes the exposed surface of the polysilicon gate. At the gate edges, near the drain and source regions, the graded or curved gate portion is formed due to the gradual encroachment of the oxidation. This effect increases the gate oxide thickness toward the edges of the gate, producing the

bird-beak shaped gate and complimentary graded oxide structure as shown in Figs. 4 and 5. Thus, unlike the step-type gate of the conventional LDMOSFET 110 of the Fig. 3, no special gate area patterning or additional processing steps are required for fabricating the LDMOSFET 210 in accordance with the present invention.

Fig. 5 shows a transmission electron microscope (TEM) image of the cross-sectional structure of a fabricated graded lift off gate LDMOSFET in which the upgraded gate oxide layer 224 is about 300 Angstroms while the oxide layer 224a of the lift off gate area is about 1000 Angstroms at the edges. The structure brings the breakdown voltage from 24V to 70V.

From the foregoing, it can be seen that the present invention comprises an improved MOS device such as an LDMOSFET, which includes a graded lift off gate structure that provides enhanced performance particularly in high frequency power applications. Since there is a common feature of DMOS for both LDMOS and VDMOS the uniqueness of the graded lift off gate is applicable to VDMOS. It will be appreciated by those skilled in the art that changes or modifications could be made to the above-described embodiment without departing from the broad inventive concept thereof. For example, the shape of the graded gate structure could be altered to provide for a lesser or greater degree of grading or curvature. It should be understood, therefore, that this invention is not limited to the particular embodiment disclosed, but is intended to cover all modifications within the spirit and scope of the present invention as defined by the appended claims.



CLAIMS

1. An improved lift off gate metal oxide semiconductor device including a silicon substrate, a source, a drain and a gate, the gate being spaced from the peripheral surface of the substrate in a channel region by an oxide layer, the improvement comprising:

the peripheral portions of the gate which are oriented toward the substrate are graded for lift off; and

the portions of the oxide layer proximate the graded gate portions are graded in a manner complementary to the graded gate portions so that the thickness of the oxide layer proximate the graded gate portions is greater than the thickness of the oxide layer proximate the ungraded portion of the gate to provide high transconductance in the channel region and increased breakdown voltage.

2. The improved device of claim 1, wherein the graded gate portions extend in a direction along the thickness of the gate to a predetermined boundary and wherein the thickness of the oxide layer proximate the graded portions of the gate corresponds to the distance between the periphery of the substrate and the predetermined boundary on the gate.

3. The improved device as recited in claim 1, wherein the oxide layer proximate the graded gate portions has a thickness in the range of 100 to 1,100 Angstroms.

4. The improved device as recited in claim 1, wherein the oxide layer proximate the ungraded portion of the gate has a thickness in the range of ⅓ to ½ of the thickness of the gate oxide layer.

5. The improved device as recited in claim 1, wherein the gate has a length which may vary depending upon the particular application.

6. A method of fabricating a lift off gate metal oxide semiconductor device having a silicon substrate, a source, a drain and a gate, the gate being spaced from the peripheral surface of the substrate in a channel region by an oxide layer, the peripheral portions of the gate oriented toward the substrate being

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graded and the portions of the oxide layer proximate the graded portions of the gate being graded in a complementary manner so that the thickness of the oxide layer proximate the graded gate portions is greater than the thickness of the oxide layer proximate the ungraded portion of the gate, the method comprising the steps of:

employing standard lift oxidation technology after polysilicon patterning to fabricate the device; and

forming the P-type body by a high temperature drive-in step using oxygen as ambient gas.