CLAIMS

What is claimed is:

1. An apparatus, comprising:
a first die;
a second die including one or more through-silicon vias disposed therein (TSV die), the first die electrically coupled to the TSV die through the one or more through-silicon vias; and
a coreless substrate, wherein both the first die and the TSV die are embedded in the coreless substrate.

2. The apparatus of claim 1, wherein the coreless substrate comprises an encapsulation layer, and wherein both the first die and the TSV die are embedded in the encapsulation layer.

3. The apparatus of claim 1, wherein the first die is electrically coupled to the TSV die through the one or more through-silicon vias by one or more corresponding conductive bumps disposed on the first die and by one or more bond pads disposed on the TSV die.

4. The apparatus of claim 1, further comprising:
a layer of epoxy flux material disposed between the first die and the TSV die.

5. The apparatus of claim 1, wherein the coreless substrate is free from routing layers between the first die and the TSV die.

6. The apparatus of claim 1, further comprising:
a die-bonding film disposed on the first die.

7. The apparatus of claim 1, wherein a surface of the first die protrudes from a surface of the coreless substrate.

8. The apparatus of claim 1, wherein no surface of the first die protrudes from a surface of the coreless substrate.

9. The apparatus of claim 1, wherein the first die is fully embedded by the coreless substrate, and wherein the TSV die is fully embedded and surrounded in the coreless substrate.

10. A process, comprising,
bonding a backside of a first die to a panel with a die-bonding film;
coupling a backside of a second die including one or more through-silicon vias disposed therein (TSV die) above and to a device side of the first die, through the one or more through-silicon vias;
forming an encapsulation layer above a device side of the TSV die, the encapsulation layer surrounding the first die and the TSV die; and, subsequently,
removing the panel from the die-bonding film.

11. The process of claim 10, wherein bonding the backside of the first die to the panel comprises bonding the backside of the first die to a surface of a cavity disposed in the panel.

12. The process of claim 10, wherein bonding the backside of the first die to the panel with the die-bonding film comprises bonding with an epoxy-based material.

13. The process of claim 10, wherein coupling the backside of the TSV die to the device side of the first die comprises coupling through one or more conductive bumps disposed on the device side of the first die and by one or more corresponding bond pads disposed on the backside of the TSV die.

14. The process of claim 13, wherein coupling the backside of the TSV die to the device side of the first die comprises bonding the backside of the TSV die to the device side of the first die with an epoxy flux material.

15. The process of claim 14, wherein the epoxy flux material cleans the one or more corresponding bond pads disposed on the backside of the TSV die and encapsulates joints formed between the one or more conductive bumps disposed on the device side of the first die and the one or more corresponding bond pads disposed on the backside of the TSV die.

16. The process of claim 13, wherein coupling through the one or more conductive bumps disposed on the device side of the first die and the one or more corresponding bond pads disposed on the backside of the TSV die comprises using a thermal compression bonding technique.

17. The process of claim 16, wherein the backside of the TSV die is heated to a temperature approximately in the range of 220 – 240 degrees Celsius during the thermal compression bonding.

18. The process of claim 10, further comprising:
prior to removing the panel, forming one or more routing layers above, and electrically coupled with, the device side of the TSV die.

19. The process of claim 18, further comprising:
prior to removing the panel, forming an array of external conductive contacts above, and electrically coupled with, the one or more routing layers.

20. The process of claim 19, wherein forming the array of external conductive contacts comprises forming a ball grid array (BGA).

What is claimed is:

1. An apparatus, comprising:

a first die comprising a device side and a back side;

a second die including one or more through-silicon vias disposed therein, the first die electrically coupled to the second die through the one or more through-silicon vias; and

a coreless substrate, wherein both the first die and the second die are embedded in the coreless substrate, the coreless substrate comprising a land side and a die side, wherein the first die protrudes from a global planarity surface of the die side of the coreless substrate wherein the global planarity surface is substantially planar with the device side.

2. The apparatus of claim 1, wherein the coreless substrate comprises an encapsulation layer, and wherein both the first die and the second die are embedded in the encapsulation layer.

3. The apparatus of claim 1, wherein the first die is electrically coupled to the second die through the one or more through-silicon vias by one or more corresponding conductive bumps disposed on the first die and by one or more bond pads disposed on the second die.

4. The apparatus of claim 1, further comprising:

a layer of epoxy flux material disposed between the first die and the second die.

5. The apparatus of claim 1, wherein the coreless substrate is free from routing layers between the first die and the second die.

6. The apparatus of claim 1, further comprising:

a die-bonding film disposed on the first die.

7. The apparatus of claim 1, wherein the first die is fully embedded by the coreless substrate, and wherein the second die is fully embedded and surrounded in the coreless substrate.

8. An apparatus, comprising:

a memory die comprising a device side and a backside;

a logic die including one or more through-silicon vias disposed therein, the logic die comprising a device side and a backside, the logic die is disposed above and in alignment with the memory die, the backside of the logic die facing the device side of the memory die, wherein the memory die is electrically coupled to the logic die through the one or more through-silcone vias; and

a coreless substrate comprising a land side and a die side, wherein both the memory die and the logic die are embedded in the coreless substrate, the backside of the memory die facing the die side of the coreless substrate, and the device side of the logic die facing the land side of the coreless substrate, wherein the memory die protrudes from a global planarity surface of the die side of the coreless substrate; and

an array of external conductive contacts disposed on the land side of the coreless substrate wherein the global planarity surface is substantially planar with the device side.

9. The apparatus of claim 8, wherein the coreless substrate comprises an encapsulation layer, and wherein both the memory die and the logic die are embedded in the encapsulation layer.

10. The apparatus of claim 8, wherein the memory die is electrically coupled to the logic die through the one or more through-silicon vias by one or more corresponding conductive bumps disposed on the device side of the memory die and by one or more bond pads disposed on the backside of the logic die.

11. The apparatus of claim 8, further comprising:

a layer of epoxy flux material disposed between and in contact with the device side of the memory die and the backside of the logic die.

12. The apparatus of claim 8, wherein the coreless substrate is free from routing layers between the device side of the memory die and the backside of the logic die.

13. The apparatus of claim 8, further comprising:

a die-bonding film disposed on the backside of the memory die.

14. The apparatus of claim 8, wherein the array of external conductive contacts is a ball grid array (BGA).

15. The apparatus of claim 8, wherein the device side of the memory die is larger in area than the backside of the logic die.