# Heating Plate with Planar Heater Zones for Semiconductor Processing

## Background

[0001] With each successive semiconductor technology generation, substrate diameters tend to increase and transistor sizes decrease, resulting in the need for an ever higher degree of accuracy and repeatability in substrate processing. Semiconductor substrate materials, such as silicon substrates, are processed by techniques which include the use of vacuum chambers. These techniques include non plasma applications such as electron beam deposition, as well as plasma applications, such as sputter deposition, plasma-enhanced chemical vapor deposition (PECVD), resist strip, and plasma etch.

[0002] Plasma processing systems available today are among those semiconductor fabrication tools which are subject to an increasing need for improved accuracy and repeatability. One metric for plasma processing systems is increased uniformity, which includes uniformity of process results on a semiconductor substrate surface as well as uniformity of process results of a succession of substrates processed with nominally the same input parameters. Continuous improvement of on-substrate uniformity is desirable. Among other things, this calls for plasma chambers with improved uniformity, consistency and self diagnostics.

## Summary

[0003] Described herein is a heating plate for a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, the heating plate comprising: an electrically insulating layer; planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater elements made of an insulator-conductor composite, the planar heater zones laterally distributed across the electrically insulating layer and operable to tune a spatial temperature profile on the semiconductor substrate; power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second

electrically conductive power supply line electrically connected to the third and fourth planar heater zones; power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones.

## Brief Description Of Figures

**[0004]** Fig. 1 is a schematic cross-sectional view of a substrate support assembly in which a heating plate with an array of planar heater zones is incorporated, the substrate support assembly also comprising an electrostatic chuck (ESC).

**[0005]** Fig. 2 illustrates the electrical connection of power supply lines and power return lines to an array of planar heater zones in a heating plate which can be incorporated in a substrate support assembly.

**[0006]** Fig. 3 is a schematic cross-sectional view of a substrate support assembly in which a heating plate is incorporated, the substrate support assembly further including a primary heater layer.

**[0007]** Fig. 4 is a schematic of an exemplary plasma processing chamber, which can include a substrate support assembly with the heating plate described herein.

## Detailed Description

**[0008]** Radial and azimuthal substrate temperature control in a semiconductor processing apparatus to achieve desired critical dimension (CD) uniformity on the substrate is becoming more demanding. Even a small variation of temperature may affect CD to an unacceptable degree, especially as CD approaches sub-100nm in semiconductor fabrication processes.

**[0009]** A substrate support assembly may be configured for a variety of functions during processing, such as supporting the substrate, tuning the substrate temperature, and supplying radio frequency power. The substrate support assembly can comprise an electrostatic chuck (ESC) useful for electrostatically clamping a substrate onto the substrate support assembly during processing. The ESC may be a tunable ESC (T-ESC). A T-ESC is described in commonly assigned U.S. Patent Nos. 6,847,014 and 6,921,724, which are hereby incorporated by reference. The substrate support

assembly may comprise a ceramic substrate holder, a fluid-cooled heat sink (hereafter referred to as cooling plate) and a plurality of concentric planar heater zones to realize step by step and radial temperature control. Typically, the cooling plate is maintained between -20 °C and 80 °C. The heaters are located on the cooling plate with a layer of thermal insulator in between. The heaters can maintain the support surface of the substrate support assembly at temperatures about 0 °C to 90 °C above the cooling plate temperature. By changing the heater power within the plurality of planar heater zones, the substrate support temperature profile can be changed. Further, the mean substrate support temperature can be changed step by step within the operating range of 0 to 90 °C above the cooling plate temperature. A small azimuthal temperature variation poses increasingly greater challenges as CD decreases with the advance of semiconductor technology.

**[0010]** Controlling temperature is not an easy task for several reasons. First, many factors can affect heat transfer, such as the locations of heat sources and heat sinks, the movement, materials and shapes of the media. Second, heat transfer is a dynamic process. Unless the system in question is in heat equilibrium, heat transfer will occur and the temperature profile and heat transfer will change with time. Third, non-equilibrium phenomena, such as plasma, which of course is always present in plasma processing, make theoretical prediction of the heat transfer behavior of any practical plasma processing apparatus very difficult if not impossible.

**[0011]** The substrate temperature profile in a plasma processing apparatus is affected by many factors, such as the plasma density profile, the RF power profile and the detailed structure of the various heating the cooling elements in the chuck, hence the substrate temperature profile is often not uniform and difficult to control with a small number of heating or cooling elements. This deficiency translates to non-uniformity in the processing rate across the whole substrate and non-uniformity in the critical dimension of the device dies on the substrate.

**[0012]** In light of the complex nature of temperature control, it would be advantageous to incorporate multiple independently controllable planar heater zones in the substrate support assembly to enable the apparatus to actively create and

maintain the desired spatial and temporal temperature profile, and to compensate for other adverse factors that affect CD uniformity.

**[0013]** Described herein is a heating plate for a substrate support assembly in a semiconductor processing apparatus, wherein the heating plate has multiple independently controllable planar heater zones that include heater elements made from a conductor-insulator composite. This heating plate comprises a scalable multiplexing layout scheme of the planar heater zones, power supply lines and power return lines (collectively, power lines). By tuning the power of the planar heater zones, the temperature profile during processing can be shaped both radially and azimuthally. More details are disclosed in commonly-owned U.S. Published Patent Application No. 2011/092072, the disclosure of which is hereby incorporated by reference. Although this heating plate is primarily described for a plasma processing apparatus, this heating plate can also be used in other semiconductor processing apparatuses that do not use plasma.

**[0014]** The planar heater zones in this heating plate are preferably arranged in a defined pattern, for example, a rectangular grid, a hexagonal grid, a polar array, concentric rings or any desired pattern. Each planar heater zone may be of any suitable size and may have one or more heater elements. When a planar heater zone is powered, all heater elements therein are powered; when a planar heater zone is not powered, all heater elements therein are not powered. To minimize the number of electrical connections, power supply lines and power return lines are arranged such that each power supply line is connected to a different group of planar heater zones and each power return line is connected to a different group of planar heater zones, each planar heater zone being in one of the groups connected to a particular power supply line and one of the groups connected to a particular power return line. No two planar heater zones are connected to the same pair of power supply and power return lines. A planar heater zone can be activated by directing electrical current through a pair of power supply line and power return line to which this particular planar heater zone is connected. The power density of the heater elements is preferably less than 10 $W/cm^2$, more preferably less than 5 $W/cm^2$. In one embodiment, each planar heater zone is not larger than four device dies being manufactured on a semiconductor substrate, or not larger than two device dies being

manufactured on a semiconductor substrate, or not larger than one device die being manufactured on a semiconductor substrate, or 16 to 100 $cm^2$, or 1 to 15 $cm^2$, or 2 to 3 $cm^2$, or 0.1 to 1 $cm^2$ in area to correspond to the device dies on the substrate. The heating plate can include any suitable number of planar heater zones, such as 100 to 1000 planar heater zones. The thickness of the heater elements may range from 2 micrometers to 1 millimeter, preferably 5-80 micrometers. To allow space between planar heater zones and/or power supply and power return lines, the total area of the planar heater zones may be up to 99% of the area of the upper surface of the substrate support assembly, e.g. 50-99% of the area. The power supply lines or the power return lines may be arranged in gaps ranging from 1 to 10 mm between the planar heater zones, or in separate planes separated from the planar heater zones plane by electrically insulating layers. The power supply lines and the power return lines are preferably made as wide as the space allows, in order to carry large current and reduce Joule heating. In one embodiment, in which the power lines are in the same plane as the planar heater zones, the width of the power lines is preferably between 0.3 mm and 2 mm. In another embodiment, in which the power lines are on different planes than the planar heater zones, the width of the power lines can be as large as the planar heater zones, e.g. for a 300 mm chuck, the width can be 1 to 2 inches. Preferably, the materials of the power supply lines and power return lines are materials with low resistivity, such as Cu, Al, W, Inconel® or Mo.

**[0015]** A conventional resistive heater element typically comprises a serpentine trace made of electrical conductors with low resistivity, such as Al, Cu, W, Inconel® and Mo. Under a fixed input voltage $V$, the heating power P of the resistive heater element is $V^2/R$, wherein $R$ is the electrical resistance thereof. $R$ can be expressed as $(\rho \cdot L)/(W \cdot T)$, wherein $\rho$ is the electrical resistivity of the material the serpentine trace is made of; $L$, $W$ and $T$ are the total trace length (i.e. the length measured by following the serpentine trace), width and thickness of the serpentine trace, respectively. Geometrical factors $L$, $W$ and $T$ of the serpentine trace are constrained by the physical size of the planar heater zone in which the resistive heater element is enclosed. $L$ has an upper limit due to available area in the planar heater zone; $W$ and $T$ have a lower limit due to fabrication techniques. Thus, $R$ has an upper limit and $P$ has a lower limit. It is increasingly difficult to meet the power density requirement

(preferably less than 10 W/cm$^2$, more preferably less than 5 W/cm$^2$. Increasing the electrical resistivity $\rho$, as described hereinbelow, can alleviate this problem.

**[0016]** Fig. 1 shows a substrate support assembly comprising one embodiment of the heating plate having an electrically insulating layer 103. The layer 103 may have one or more layers made of a polymer material, an inorganic material, a ceramic such as silicon oxide, alumina, yttria, aluminum nitride or other suitable material. The substrate support assembly further comprises (a) at least one ESC (electrostatic clamping) electrode 102 (e.g. monopolar or bipolar) embedded in the layer 103 to electrostatically clamp a substrate to the surface of the layer 103 with a DC voltage, (b) a thermal barrier layer 107, (c) a cooling plate 105 containing channels 106 for coolant flow. The power supply lines and power return lines are not shown for clarity.

**[0017]** As shown in Fig. 2, each of the planar heater zones 101 is connected to one of the power supply lines 201 and one of the power return lines 202. No two planar heater zones 101 share the same pair of power supply 201 and power return 202 lines. By suitable electrical switching arrangements, it is possible to connect a pair of power supply line 201 and power return line 202 to a power supply (not shown), whereby only the planar heater zone connected to this pair of power lines is powered. The time-averaged heating power of each planar heater zone can be individually tuned by time-domain multiplexing. In order to prevent crosstalk between different heater zones, a rectifier 250 (e.g. a diode) may be serially connected between each heater zone and the power supply lines connected thereto (as shown in Fig. 2), or between each heater zone and the power return lines connected thereto (not shown). The rectifier can be physically located in the heating plate or any suitable location. Alternatively, any current blocking arrangement such as solid state switches can be used to prevent crosstalk.

**[0018]** Each planar heater zone 101 comprises at least one heater element made of an insulator-conductor composite. In one embodiment, the insulator-conductor composite comprises one or more insulator materials selected from the group consisting of $Al_2O_3$, $SiO_2$, $Y_2O_3$, $Si_3N_4$, AlN, and one or more conductor materials selected from the group consisting of Al, Cu, Mo, W, Au, Ag, Pt, Pd, C, $MoSi_2$, WC, SiC. The insulator-conductor composite can be made by mixing powders

(preferably having particle sizes from 0.2 to 20 microns) of an insulator and a conductor with a suitable liquid (e.g. methanol, ethanol, acetone, isopropyl alcohol, water, mineral oil, or a mixture thereof) into a slurry, screen printing the slurry and sintering the slurry. In a preferred embodiment, the insulator-conductor composite comprises up to 30 wt% of $Al_2O_3$ and balance of W.

**[0019]** The layer 103 of the heating plate is preferably made of ceramic. The heating plate can be made by an exemplary method comprising: pressing a mixture of ceramic powder, binder and liquid into sheets; drying the sheets; forming vias in the sheets by punching holes in the sheets; forming power supply lines and power return lines on the sheets by screen printing a slurry of conducting powder (e.g. W, WC, doped SiC or $MoSi_2$), pressing a precut metal foil, spraying a slurry of conducting powder, or any other suitable technique; forming heater elements by screen printing or spraying a slurry of insulator and conductor powders; aligning the sheets; bonding the sheets together by sintering to form the layer 103; filling the vias with a slurry of conducting powder. The sheets can be about 0.3 mm in thickness.

**[0020]** Fig. 3 shows the substrate support assembly of Fig. 1, further comprising the primary heater layer 601. Preferably, the primary heater layer 601 includes at least two individually controlled high-power heaters. The power of the primary heaters is between 100 and 10000W, preferably, between 1000 and 5000W. The primary heaters may be arranged as a rectangular grid, concentric annular zones, radial zone or combination of annular zones and radial zones. The primary heaters may be used for changing the mean temperature, tuning the radial temperature profile, or step-by-step temperature control on the substrate. The primary heaters are above thermal barrier layer 107 and may be located above or below the heater zones 101.

**[0021]** As an overview of how a plasma processing chamber operates, Fig. 4 shows a schematic of a plasma processing chamber comprising a chamber 713 in which an upper showerhead electrode 703 and a substrate support assembly 704 are disposed. A substrate 712 is loaded through a loading port 711 onto the substrate support assembly 704. A gas line 709 supplies process gas to the upper showerhead electrode 703 which delivers the process gas into the chamber. A gas source 708 (e.g. a mass flow controller supplying a suitable gas mixture) is connected to the gas

line 709. A RF power source 702 is connected to the upper showerhead electrode 703. In operation, the chamber is evacuated by a vacuum pump 710 and the RF power is capacitively coupled between the upper showerhead electrode 703 and a lower electrode in the substrate support assembly 704 to energize the process gas into a plasma in the space between the substrate 712 and the upper showerhead electrode 703. The plasma can be used to etch device die features into layers on the substrate 712. The substrate support assembly 704 includes a heating plate as described herein. As described above, it should be appreciated that while the detailed design of the plasma processing chamber may vary, RF power is coupled to the plasma through the substrate support assembly 704.

**[0022]** Examples of suitable insulating and conductive material for use in manufacture of the substrate support assembly are disclosed in commonly assigned U.S. Patent No. 6,483,690, the disclosure of which is hereby incorporated by reference.

**[0023]** While a heating plate, methods of manufacturing the heating plate, and a substrate support assembly comprising the heating plate have been described in detail with reference to specific embodiments thereof, it will be apparent to those skilled in the art that various changes and modifications can be made, and equivalents employed, without departing from the scope of the appended claims.

Claims:

1. A substrate support configured to support a semiconductor substrate in a semiconductor processing apparatus, the substrate support comprising:

an electrically insulating layer;

a plurality of planar thermal zones each comprising one or more thermal elements made of an insulator-conductor composite, the planar thermal zones laterally distributed across the electrically insulating layer;

power supply lines comprising at least a first electrically conductive power supply line electrically connected to at least two of the planar thermal zones and a second electrically conductive power supply line electrically connected to at least two of the planar thermal zones;

power return lines comprising at least a first electrically conductive power return line electrically connected to at least two of the planar thermal zones and a second electrically conductive power return line electrically connected to at least two of the planar thermal zones;

wherein each planar thermal zone is connected to a different pair of power supply and return lines, wherein the power supply lines and the power return lines are on a different plane than the plurality of planar thermal zones, and wherein respective widths of the power supply lines and the power return lines are as large as a width of the plurality of planer thermal zones.

2. The substrate support of claim 1, wherein the insulator-conductor composite comprises one or more insulator materials selected from the group consisting of $Al_2O_3$, $SiO_2$, $Si_3N_4$ and AlN, and one or more conductor materials selected from the group consisting of Al, Cu, Mo, W, Au, Ag, Pt, Pd, C, $MoSi_2$, WC and SiC.

3. The substrate support of claim 2, wherein the insulator-conductor composite comprises up to 30 wt % of $Al_2O_3$ and balance of W.

4. The substrate support of claim 1, wherein the planar thermal zones are sized such that:

(a) each planar thermal zone has a cross-sectional area of 0.1 to 1 $cm^2$,

(b) each planar thermal zone has a cross-sectional area of 1 to 3 $cm^2$,

(c) each planar thermal zone has a cross-sectional area of 3 to 15 $cm^2$, or

(d) each planar thermal zone has a cross-sectional area of 15 to 100 $cm^2$.

5. The substrate support of claim 1 includes 100 to 1000 thermal zones wherein each thermal element has a serpentine shape.

6. The substrate support of claim 1, wherein the electrically insulating layer comprises a polymer material, a ceramic material, a fiberglass composite, or a combination thereof.

7. The substrate support of claim 1, wherein the total number of the power supply lines and the power return lines is equal to or less than the total number of the planar thermal zones.

8. The substrate support of claim 1, wherein a total area of the planar thermal zones is from 50% to 99% of an upper surface of the substrate support.

9. The substrate support of claim 1, wherein the planar thermal zones are arranged in a rectangular grid, hexagonal grid or concentric rings; and the thermal zones are separated from each other by gaps at least 1 millimeter in width and at most 10 millimeters in width.

10. A substrate support comprising an electrostatic chuck (ESC) configured to provide support to a semiconductor substrate in a semiconductor processing chamber, the ESC comprising:

an electrically insulating layer;

a plurality of planar thermal zones each comprising one or more thermal elements made of an insulator-conductor composite, the planar thermal zones laterally distributed across the electrically insulating layer;

power supply lines comprising at least a first electrically conductive power supply line electrically connected to at least two of the planar thermal zones and a second electrically conductive power supply line electrically connected to at least two of the planar thermal zones;

power return lines comprising at least a first electrically conductive power return line electrically connected to at least two of the planar thermal zones and a second electrically conductive power return line electrically connected to at least two of the planar thermal zones;

wherein each planar thermal zone is connected to a different pair of power supply and return lines; and

a cooling plate configured to provide a heat sink beneath the ESC, wherein the power supply lines and the power return lines are on a different plane than the plurality of planar thermal zones, and wherein respective widths of the power supply lines and the power return lines are as large as a width of the plurality of planer thermal zones.

11. The substrate support of claim 10, further comprising at least one primary thermal layer disposed above or below the planar thermal zones, wherein the primary thermal layer is electrically insulated from the planar thermal zones, the power supply lines, and the power return lines of the ESC.

12. The substrate support of claim 11, wherein the primary thermal layer includes two or more primary thermal elements powered with at least 100 W.

13. A method of making a substrate support comprising an electrically insulating layer, a plurality of planar thermal zones each comprising one or more thermal elements made of an insulator-conductor composite, the planar thermal zones laterally distributed across the electrically insulating layer, power supply lines comprising at least a first electrically conductive power supply line electrically connected to at least two of the planar thermal zones and a second electrically conductive power supply line electrically connected to at least two of the planar thermal zones, power return lines comprising at least a first electrically conductive power return line electrically connected to at least

two of the planar thermal zones and a second electrically conductive power return line electrically connected to at least two of the planar thermal zones, wherein each planar thermal zone is connected to a different pair of power supply and return lines, wherein the power supply lines and the power return lines are on a different plane than the plurality of planar thermal zones, and wherein respective widths of the power supply lines and the power return lines are as large as a width of the plurality of planer thermal zones, the method comprising:

mixing powders of an insulator and a conductor with a liquid into a slurry, screen printing the slurry on the electrically insulating layer and sintering the slurry.

14. The method of claim 13, wherein the liquid is selected from the group consisting of methanol, ethanol, acetone, isopropyl alcohol, water, mineral oil and a mixture thereof.

15. The method of claim 13, wherein the powders have particle sizes from 0.2 to 20 microns.

16. A method for manufacturing a substrate support comprising an electrically insulating layer, a plurality of planar thermal zones each comprising one or more thermal elements made of an insulator-conductor composite, the planar thermal zones laterally distributed across the electrically insulating layer, power supply lines comprising at least a first electrically conductive power supply line electrically connected to at least two of the thermal zones and a second electrically conductive power supply line electrically connected to at least two of the thermal zones, power return lines comprising at least a first electrically conductive power return line electrically connected to at least two of the thermal zones and a second electrically conductive power return line electrically connected to at least two of the thermal zones, wherein each thermal zone is connected to a different pair of power supply and return lines, wherein the power supply lines and the power return lines are on a different plane than the plurality of thermal zones, and wherein respective widths of the power supply lines and the power return lines are as large as a width of the plurality of planer thermal zones, the method comprising:

pressing a mixture of ceramic powder, binder and liquid into sheets;

drying the sheets;

forming vias in the sheets by punching holes therein;

forming the power supply lines and power return lines on the sheets;

forming the thermal elements by screen printing or spraying a slurry of insulator and conductor powders;

aligning the sheets;

bonding the sheets together by sintering to form the electrically insulating layer;

filling the vias with a slurry of conducting powder.

17. The method of claim 16, wherein the power supply lines and power return lines are formed by screen printing a slurry of conducting powder, pressing a precut metal foil, or spraying a slurry of conducting powder.

18. A method for plasma processing semiconductor substrates in a plasma processing chamber containing a substrate support with an electrostatic chuck comprising an electrically insulating layer, a plurality of planar thermal zones each comprising one or more thermal elements made of an insulator-conductor composite, the planar thermal zones laterally distributed across the electrically insulating layer, power supply lines comprising at least a first electrically conductive power supply line electrically connected to at least two of the planar thermal zones and a second electrically conductive power supply line electrically connected to at least two of the planar thermal zones, power return lines comprising at least a first electrically conductive power return line electrically connected to at least two of the planar thermal zones and a second electrically conductive power return line electrically connected to at least two of the planar thermal zones, wherein each planar thermal zone is connected to a different pair of power supply and return lines, wherein the power supply lines and the power return lines are on a different plane than the plurality of planar thermal zones, wherein respective widths of the power supply lines and the power return lines are as large as a width of the plurality of planer thermal zones, the method comprising:

(a) loading a semiconductor substrate into the processing chamber and positioning the semiconductor substrate on the substrate support;

(b) determining a temperature profile that compensates for processing conditions affecting critical dimension (CD) uniformity;

(c) heating the semiconductor substrate to conform to the temperature profile using the substrate support;

(d) igniting plasma and processing the semiconductor substrate while controlling the temperature profile by independently controlled temperature of the planar thermal zones;

(e) unloading the semiconductor substrate from the processing chamber and repeating steps (a)-(e) with a different semiconductor substrate.