

ABSTRACT

There is provided a host device communicating with a memory device including a first memory bank. The host device includes a command issuance circuit configured to issue a regular refresh command for a first memory bank of a memory device at every regular refresh period, a first debit counter configured to manage a first debit count for a first sub-bank in the first memory bank, a second debit counter configured to manage a second debit count for a second sub-bank in the first memory bank, and a refresh scheduling circuit configured to determine whether to skip issuing the regular refresh command of the command issuance circuit based on the first debit count and the second debit count.

FIG. 1