

VERTICAL MEMORY DEVICE AND METHOD

BACKGROUND

[0001] In recent years non-volatile memories have become established in a variety of electronic systems, especially mobile systems. For example, non-volatile memories are widely employed in a variety of electronic products such as portable computers, digital cameras, mobile telephones, and other similar products that are becoming increasingly smaller in size and require increasingly higher memory storage capacity to support advanced applications. To keep pace with these advanced applications, non-volatile memories are being manufactured with higher levels of integration, faster response, higher reliability, lower power consumption, and increased storage capacity.

[0002] One way to achieve these ever more demanding requirements is to downscale the non-volatile memory cells. Higher storage capacity for non-volatile memories may be achieved by increasing the memory cell density and reducing the size of cell components such as the floating gate and the control gate, among other elements. Conventional planar semiconductor memory architectures require too much real estate per memory cell and are difficult to downscale to achieve denser cell layouts to effectively increase the memory capacity on a wafer.

[0003] Vertically oriented memory cell architectures having a thin vertical Si body and two sided flash cells, however, may be configured to achieve a denser memory cell layout. Although the vertical nature of these memory cell structures provide for denser memory cell layout, these structures lack the necessary overlapping areas between the control gate and the floating gate to yield a suitable gate coupling ratio (GCR). The importance of a suitable GCR is explained below.

[0004] Non-volatile memories, such as flash cells, may be fabricated using a metal-oxide-semiconductor (MOS) process. An MOS memory cell array may comprise electrically isolated floating gate structures formed of polycrystalline silicon (polysilicon) surrounded by a silicon dioxide (SiO_2) insulative layer. The floating polysilicon gate is electrically isolated from the substrate regions of the semiconductor by the SiO_2 insulative layer. Cells of this type also may comprise an n-channel MOS transistor.

[0005] The cell operation is controlled by storing electron charge on the electrically isolated floating polysilicon gate. A linear capacitor network is formed of the SiO_2 insulative layers surrounding the floating gate and the terminals of the source, drain, transistor channel, and polysilicon control gate. Electrical access to the floating gate is only through this linear capacitor network. The capacitance of the cell may be defined in terms of capacitive coupling ratios, including, for example, the gate coupling ratio (GCR), drain coupling ratio (DCR), and source coupling ratio (SCR). Due to the capacitive coupling, any change in control gate voltage produces a change in floating gate voltage in accordance with the GCR. A suitable GCR for proper memory operation is ~ 0.6 . This may be referred to as a "golden ratio" for memory cell structures that governs the development of the scaled memory cells, such as, scaled flash memory cells, for example.

[0006] Due to the horizontal orientation of the gates in conventional planar flash memory cells, for example, a suitable gate coupling ratio of ~ 0.6 may be achieved by extending the floating gate and the control gate laterally (*e.g.*, horizontally) into the isolation area to increase the overlapping portions of the gates. The amount of overlapping determines the capacitance coupling between the gates and thus the overlapping regions may be adjusted to yield a suitable or desirable GCR. Vertical flash cell structures, however, do not have an equivalent isolation area available to extend the gates, and thus, increasing or tuning the GCR in a vertical memory structure is not as trivial as in the planar structures.

Accordingly, conventional vertical memory structures have a GCR of ~ 0.33 , which is substantially below the desired golden ratio.

BRIEF DESCRIPTION OF THE DRAWINGS

5

[0007] FIG. 1 illustrates a schematic cross-sectional view of one embodiment of a memory device 100.

[0008] FIG. 2 illustrates a diagram of one embodiment of the memory device 100 comprising a dielectric formed thereon.

10 [0009] FIG. 3 illustrates a diagram of one embodiment of a subcomponent of the memory device 100.

[0010] FIG. 4 illustrates a diagram of one embodiment of a floating gate component of the memory device 100.

[0011] FIGS. 5A-5J illustrate various embodiments of processes and integration
15 techniques to realize one embodiment of the memory device 100.

[0012] FIG. 6 illustrates one embodiment of a memory 600.

[0013] FIG. 7 illustrates one embodiment of a process flow diagram 700.

DETAILED DESCRIPTION

20

[0014] FIG. 1 illustrates schematic cross-sectional view of one embodiment of a memory device 100 comprising a first memory cell 102 and a second memory cell 104. In one embodiment, the memory cells 102, 104 are formed back-to-back with a common semiconductor body 112. Other embodiments of the memory device 100 may comprise

25 nonvolatile ultra-high density electrically erasable and programmable read only memories

(EEPROM). The memory cells 102, 104 form only a single pair of memory cells in a memory device comprising an array of multiple addressable memory cells, for example.

In one embodiment, the memory device 100 may be a flash EEPROM, which provides simultaneous erasure of multiple bits, for example. Embodiments of the memory device

5 100, however, may comprise other semiconductor memory devices, such as static or dynamic random access memories (SRAMs and DRAMs, respectively), synchronous random access memories, or other types of memories that include a matrix of selectively addressable memory cells. In one embodiment, the memory device 100 may comprise a three-dimensional non-volatile memory device having a gate portion that extends in a
10 substantially orthogonal direction away from the substrate. Accordingly, in one embodiment, such gate structures may be referred to as vertical gate structures. Memory cells comprising vertical gate structures and corresponding select devices may be integrated on a much smaller surface area of a semiconductor substrate to provide a denser memory array, for example. In the following description, the terms vertical and horizontal
15 are used merely to describe the relative orientation of the gates to the substrate where the vertical direction is substantially orthogonal to the horizontal direction. The embodiments, however, are not limited in this context.

[0015] Embodiments of the memory device 100 may be fabricated using standard MOS processing. The memory device 100 may be an n-channel device. Peripheral circuits to
20 select, address, read from, and write to the memory device 100 may employ either n-channel or complementary MOS (CMOS) devices, among other devices. In the following description, the term substrate generally refers to any structure on which integrated circuits may be formed, and also to such structures during the various stages of the integrated circuit fabrication process. The substrates may comprise both doped and undoped
25 semiconductors, epitaxial layers of semiconductor on a supporting semiconductor or

insulating material, combinations of such layers, as well as other known structures, for example. Throughout the drawings and written description, like numerals describe substantially similar components throughout the several views. The embodiments described herein, however, are not limited to the context in which they may be described.

5 [0016] Referring again to FIG. 1, one embodiment of the memory device 100 comprises a substrate 110 and a body 112 formed thereon. The substrate extends along direction 155, which in one embodiment may be referred to as the 'horizontal' direction. The body 112 extends away from the substrate 110 along direction 150 such that it is oriented substantially orthogonal to the substrate 110. In one embodiment, direction 150 may be referred to as the 'vertical' direction. In one embodiment, the body 112 may be formed of Si or other semiconductor material. The body 112 has heavily doped regions forming a source 114 and a drain 116. As previously discussed, the memory device comprises a first memory cell 102 and a second memory cell 104. Each memory cell 102, 104 may comprise one or more floating gates 118 located laterally on either side of the vertical body 112 along direction 155. The floating gates 118 extend vertically away from the substrate 110 along direction 150. The floating gates 118 may be formed of polysilicon. Each memory cell 102, 104 may comprise one or more control gates 120 located adjacent to and laterally on either side of the floating gates 118 along direction 155. The control gates 120 also extend vertically away from the substrate 110 along direction 150. The control gates 118 may be formed of polysilicon. Both the floating gates 118 and the control gates 120 are electrically insulated from the substrate 110 by a dielectric material. [0017] A first dielectric 122 is disposed between the body 112 and the floating gates 118. Vertical portions 122A of the dielectric form a tunnel dielectric between the body 112 and the floating gates 118. Horizontal portions 122B of the dielectric 122 isolate the floating gates 118 and the control gates 120 from the substrate 110 and the source 114. The

vertical portions 122A of the dielectric 122 are adjacent to the body 112 and extend away from the substrate 110 along direction 150. The horizontal portions 122B of the dielectric 122 are adjacent to the substrate 110 and extend away from the body 112 along direction 155. In one embodiment, the horizontal portions 122B of the dielectric 122 extend below the floating gates 118 and the control gates 120, for example. In one embodiment, the dielectric 122 may be an oxide dielectric and forms a tunnel dielectric layer. A second dielectric 124 may be formed between each floating gate 118 and control gate 120. The second dielectric 124 forms a dielectric layer in region 129 between horizontal portions of the floating gates 118B and the control gates 120B. In one embodiment the second dielectric 124 may be an oxide-nitride-oxide (ONO) material, among other materials, for example.

[0018] In one embodiment, each floating gate 118 comprises a vertical member 118A extending along direction 150 and a horizontal member 118B extending along direction 155. In one embodiment, the vertical member 118A and the horizontal member 118B form an “L-shaped” floating gate structure in which the vertical member 118A is longer than the horizontal member 118B. Each control gate 120 comprises a corresponding vertical member 120A extending along direction 150 and horizontal member 120B extending along direction 155. Each memory cell 102, 104 comprises a gate overlapping region 130 formed by the horizontal members 118B and 120B of each floating gate 118 and each control gate 120, respectively. The GCR between the floating gate 118 and the control gate 120 in each memory cell 102, 104 may be tuned or adjusted by controlling the horizontal length of each of the gate overlapping regions 130.

[0019] In one embodiment, the gate overlapping region 130 in each memory cell 102, 104 may be formed to increase the overall coupling capacitance between the floating gate 118 and the control gate 120. Thus, the gate overlapping region 130 may be formed to provide

a greater GCR between the floating gate 118 and the control gate 120. In accordance with one embodiment, for example, a specific implementation and geometry of the gate overlapping region 130 may provide a GCR approaching the desired golden number of ~ 0.6 . For example, in one embodiment, the gate overlapping region 130 may be designed to yield a GCR of approximately 0.57. In one embodiment, the L-shaped floating gate 118 structure may be adapted to increase the capacitive coupling between the floating gate 118 and the control gate 120 in three-dimensional vertical flash memory cell structures, for example. The capacitance between the floating gate 118 and the body 112 remains approximately the same as in conventional vertical gate memory structures. The embodiments, however, are not limited in this context.

[0020] Floating gates and control gates in conventional planar flash memory structures are horizontally disposed and extend along direction 155. In planar memory structures, a desired GCR approaching the golden number may be achieved by extending the overlapping portions of the floating gate and the control gate horizontally into an isolation area. The overlapping portions of such planar structures may be extended or adjusted until the desired GCR between the gates is achieved. In vertical memory cell structures, such as, the memory device 100 structure, for example, there is no equivalent horizontal isolation area along direction 155 into which the gates 118, 120 may be extended due to their vertical orientation. Rather, the floating gate 118 and the control gate 120 extend vertically along direction 150. To increase the capacitive coupling between the floating gate 118 and the control gate 120, and accordingly, to increase and tune the CGR to a predetermined or desired value (*e.g.*, ~ 0.6), the floating gate 118 and the control gate 120 are formed to include horizontal members 118B, 120B that extend along direction 155 and define a gate overlapping region 130 therebetween.

[0021] Although embodiments of the vertical memory device 100 may require increased capacitive coupling between the floating gates 118 and the control gates 120, the capacitive coupling between the floating gates 118 and the source 114 or the floating gates 118 and the substrate 110 should be minimized. In one embodiment, the capacitive coupling between the floating gates 118 and the source 114 or the floating gates 118 and the substrate 110 may be minimized or reduced by forming a suitable oxide layer therebetween using various semiconductor fabrication processes. As the memory cells 102, 104 are scaled to smaller dimensions, however, it may be difficult to form a suitably thick horizontal layer of the dielectric 122B using conventional tunneling dielectric material processing. A relatively thick structure may be formed using a dopant enhanced oxidation process to help reduce the capacitive coupling between the horizontal members 118B of the floating gates 118 and the source 114 and/or the substrate 110.

[0022] Accordingly, in one embodiment a layer of the first dielectric 122 of the memory device 100 may be formed using a dopant enhanced oxidation process to enhance the thickness of the horizontal dielectric 122B portion of the first dielectric 122 in the horizontal region between the floating gates 118B and the source 114 and the substrate 110 to reduce the gate 118 to source 114 and the gate 118 to substrate 110 coupling, for example. For example, in one embodiment, the dielectric 122 may be formed by a dopant enhanced oxidation process to reduce the capacitive coupling between the floating gates 118 and the source 114 or the floating gates 118 and the substrate 110. The dopant enhanced oxidation process forms a horizontal dielectric 122B having a thick layer around portions of the source 114 and the substrate 110 proximate the L-shaped floating gate 118. In one embodiment, if the drain 116 is formed, the dopant enhanced oxidation process may also form a thick horizontal dielectric layer (not shown) above the drain 116, depending on the doping concentration. In one embodiment, the dopant enhanced

oxidation process may be used in the integration process to form the memory device 100 and three-dimensional vertical flash memory structures in general, for example, that yield a suitable CGR. The embodiments, however, are not limited in this context. In another embodiment, the GCR of the memory device 100 may be adjusted by using a high “K” dielectric material to control the capacitance between the floating gate 118 and the control gate 120, for example. The embodiments, however, are not limited in this context.

[0023] FIG. 2 illustrates a diagram 200 of one embodiment of the memory device 100 comprising a dielectric 210 formed using a dopant enhanced oxidation process. The dopant enhanced oxidation process may be used to provide a suitable thickness of the dielectric 210B between the gates 118 and the substrate 110 and between the gates 118 and the source 114 regions to reduce the coupling between the gates 118 and the source 114 and the gates 118 and the substrate 110. The diagram 200 also illustrates a transition region 216 in a detailed and magnified view. The dielectric 210 layer has vertical portions 210A with a thickness 212 and horizontal portions 210B, C with a thickness 214. The thickness 214 of the horizontal portions 210B between the horizontal members 118B (FIG. 1) of each floating gate 118 (FIG. 1) and the substrate 110 may be adjusted to reduce the capacitive coupling between the floating gates 118 and the source 114 and between the floating gates 118 and the substrate 110. The drain 116 may be formed at different stages of processing, for example. In one embodiment, if the drain 116 is formed prior to the dopant enhanced oxidation process, the horizontal portion 210C of the dielectric layer 210 above the drain 116 also may be formed with thickness 214. In one embodiment, the thickness 214 of the horizontal portions 210B and 210C may be slightly different. In one embodiment, the thickness 214 of the horizontal portion 210B of the dielectric 210 may be three to six thicker than the thickness 212 of the vertical portion 210A of the dielectric 210 between the floating gates 118 and the body 112. In one embodiment, when the dopant

enhanced oxidation dielectric 210 is formed, the transition region 216 may be formed proximate the source 114. The dopant enhanced oxidation dielectric 210 layer in the transitional region 216 is generally substantially thick 218 and may reduce any unwanted capacitive coupling between the floating gates 118 (FIG. 1) and the substrate 110 and around the source 114. In one embodiment, three-dimensional flash memory cell structures may be formed using an enhanced oxidation process.

[0024] FIG. 3 illustrates a diagram 300 of one embodiment of a subcomponent of the memory device 100 (FIG. 1) floating gates 118 (FIG. 1) with a layer of dielectric 310 formed using a directional deposition process. In one embodiment, this may comprise using a non-conformal directional deposition. The dielectric 310 material is deposited in the direction indicated by deposition direction 320, which may be referred to as the vertical direction. A directional deposition process forms a thinner layer of material on vertical surfaces extending parallel to the deposition direction 320 and it forms a much thicker layer of material on surfaces that are substantially orthogonal, horizontal, to the deposition direction 320. Accordingly, a relatively thin layer of tunneling dielectric 310A of thickness 312 is formed on vertical surfaces parallel to the deposition direction 320 and relatively thick layers of dielectric 310B, C of thickness 314 are formed on horizontal surfaces substantially orthogonal to the deposition direction 320. Thus, thickness 314 of the horizontal layers of the dielectric 310B, C are thicker than the thickness 312 of the vertical layers of the dielectric 310. In one embodiment, the thickness 314 of the horizontal layers of the dielectric 310B and 310C may be slightly different. In one embodiment, the thickness 314 of the horizontal layers of the dielectric 310B helps to isolate the floating gates 118 (FIG. 1) from the source 114 and the substrate 110. One example of a directional dielectric deposition process to form a layer of the dielectric 310 is a jet vapor deposition process comprising Si_3N_4 . The directionality of the jet vapor

deposition process provides a relatively thick layer of dielectric 310B and a relatively thin layer of dielectric 310A in which the dielectric 310B is thicker than the dielectric 310A. This reduces the capacitive coupling between the floating gates 118 and the source 114 and the floating gates 118 and the substrate 110. The embodiments, however, are not limited in this context. The directional dielectric deposition processes also may provide a thicker layer of dielectric 310B layer in the source 114 and substrate 110 regions to reduce floating gate 118 to source 114 and/or substrate 110 coupling, for example. The embodiments, however, are limited in this context.

[0025] FIG. 4 illustrates a diagram 400 of one embodiment of the floating gate 118 formed using a sacrificial oxide spacer 410. In one embodiment, the spacer 410 may be formed using plasma enhanced chemical vapor deposition (PECVD) techniques, for example. The source 114 may be formed such that its profile top 412 is even or level with the bottom 414 portion of the horizontal members 118B of the floating gates 118. In subsequent processing steps, the sacrificial oxide spacer 410 is removed to form the second dielectric 124 layer (FIG. 1).

[0026] FIGS. 5A-5J illustrates various embodiments of processes and integration techniques to realize the L-shaped floating gates 118 of the memory device 100 (FIG. 1). Those skilled in the art will appreciate that the figures are not drawn to scale and some details may have been omitted for simplicity while some details may not have been specifically described.

[0027] FIG. 5A illustrates a schematic cross-sectional view of one embodiment of a starting structure 500 comprising a substrate 110, a body 112, a source 114, and a drain 116. Those skilled in the art will appreciate that the drain 116 may be implanted at later stages of the semiconductor process and the initial starting structure 500 may contain the

substrate 110, body 112, and the implanted source 114. In one embodiment, the body 112 is formed of Si. The starting structure 500 is formed with heavy implant regions for the source 114 and the substrate 110. The body 112 extends vertically from the substrate 110 along direction 150 and the substrate 110 extends horizontally on either side of the body 112 along direction 155. The source 114 is formed by implants and is located at a near end 502 where the body 112 joins the substrate 110. The drain 116, which may be formed by implants during subsequent processing steps, is located at a distal end 504.

[0028] FIG. 5B illustrates generally at 510 one embodiment of the starting structure 500 shown in FIG. 5A with a dielectric layer 512 formed thereon. The dielectric layer 512 covers the substrate 110 and the body 112. The dielectric layer 512 has vertical portions 512A of thickness 514 to form a tunnel dielectric layer, for example. In one embodiment, the dielectric layer 512 may be an oxide layer and may form a tunnel dielectric oxide layer between the floating gates 118 (FIG. 1) and the Si body 112. The dielectric layer 512 also has horizontal portions 512B of thickness 516 to form an isolation layer, for example. The thickness 516 of the horizontal portions 512B adjacent to the heavily doped substrate 110 and the source 114 is greater than the thickness 514 of the vertical portions 512A forming the tunnel dielectric layer surrounding the body 112. In one embodiment, thickness 516 may be three to six greater than thickness 514. For example, thickness 516 may range from 21 nm to 42 nm while thickness 514 may range from 5 nm to 9 nm. In one embodiment, as described above with reference to FIG. 2, the dielectric layer 512 may be formed using a dopant enhanced oxidation technique. In other embodiments, as described above with reference to FIG. 3, the oxide layer may be formed using directional deposition techniques. In one embodiment, the dielectric layer 512 may be formed of silicon dioxide (SiO_2) surrounding the body 112 and covering the substrate 110. Regardless of whether the dielectric oxide is formed using a dopant enhanced oxidation or directional deposition

process, the thickness 516 of the horizontal portions 512B of the dielectric layer 512 over the substrate 110 and the source 114 is made sufficiently thick to reduce the coupling between the floating gates 118 (FIG. 1) and the source 114 and between the floating gates 118 and the substrate 110.

5 [0029] FIG. 5C illustrates generally at 520 one embodiment of the structure 510 shown in FIG. 5B with a conformal polysilicon layer 522 formed over the dielectric layer 512. The conformal polysilicon layer 522 may be formed of polycrystalline silicon (polysilicon), for example. The polysilicon layer 522 surrounds the dielectric layer 512. The polysilicon layer 522 has vertical portions 522A surrounding the vertical portions 512A of the
10 dielectric layer 512 around the vertical body 112 and has horizontal portions 522B covering horizontal portions 512B of the dielectric layer 512 over the substrate 110. The horizontal portions 522B of the polysilicon layer 522 extend laterally from the body 112 above the dielectric layer 512B covering the substrate 110. Another horizontal portion 522C bridges the two vertical portions 522A. In subsequent processing steps portions of
15 the polysilicon layer 522 may be etched and polished to remove unwanted poly parts to form the two L-shaped floating gates 118 in the memory cells 102, 104 of the memory device 100 (FIG. 1), for example. Dielectric layer 512 (*e.g.*, SiO₂) electrically isolates the polysilicon layer 522 from the body 112. The thickness 516 of the horizontal portions 512B of the dielectric layer 512 is selected to electrically isolate the horizontal portions
20 522B of the polysilicon layer 522 from the substrate 110 and the source 114. In region 524, the laterally extending horizontal portions 522B of the polysilicon layer 522 eventually form the L-shaped structure 524 of the floating gates 118 (FIG. 1).

[0030] FIG. 5D illustrates generally at 530 one embodiment of the structure 520 shown in FIG. 5C with a conformal spacer layer 532 formed over the polysilicon layer 522. The
25 conformal spacer layer 532 has vertical portions 532A adjacent to the vertical portions

522A of the polysilicon layer 522. The conformal spacer layer 532 also has horizontal portions 532B extending laterally from the base of the body 112 above the horizontal portions 522B of the polysilicon layer 522. The conformal spacer layer 532 also has an horizontal portion 532C at the distal end 504 of the body 112. In one embodiment, the conformal spacer layer 532 has a width 534. In one embodiment, the conformal spacer layer 532 serves as a directional oxide spacer. In one embodiment, the conformal spacer layer 532 may be formed using a chemical vapor deposition (CVD) technique, for example, although other techniques may be employed. In one embodiment, the spacer layer 532 may be formed using a Si_3N_4 layer instead of using an oxide spacer, for example.

[0031] FIG. 5E illustrates generally at 540 one embodiment of the structure 530 shown in FIG. 5D after etching the conformal spacer layer 532 (*e.g.*, the directional oxide spacer).

The etching process is a vertical process and thus it removes the horizontal portions 532B (FIG. 5D) of the spacer layer 532. The etching process also removes the horizontal

portion 532C (FIG. 5D) of the spacer layer 532 at the distal end 504 of the body 112. The width 534 of the oxide spacer 532 determines the horizontal extension of the 'L' portion of the floating gates 118 (FIG. 1), for example. The width 534 of the oxide spacer 534 layer provides for self-aligned, precise control of the horizontal extension of the 'L' portion of the floating gates 118 (FIG. 1). The vertical portions 532A of the spacer layer 532 adjacent to the body 112 remain substantially intact during the etching process and are left behind to act as a mask for the process illustrated with reference to FIG. 5F below.

[0032] FIG. 5F illustrates generally at 550 one embodiment of the structure 540 shown in FIG. 5D after etching the polysilicon spacer layer 532 mask. The etching process also removes the horizontal portions 522B (FIGS. 5C-5E) of the polysilicon layer 522 that extend laterally beyond the width 534 of the spacer layer 532 as shown at 552, for

example. The etching process also removes the horizontal portion 522C (FIGS. 5C-5E) of the polysilicon layer 522 at the distal end 504 of the body 112. Removing the horizontal portions 522B that extend laterally beyond the width 534 of the spacer layer and the horizontal 522C at the distal end 504 forms the L-shaped floating gate 118, which is now
5 exposed in the polysilicon layer 522.

[0033] FIG. 5G illustrates generally at 560 one embodiment of the structure 550 shown in FIG. 5F after wet or dry etching to remove the spacer layer 532. Some of the dielectric layer 512 between the polysilicon gate 522 and the Si body 112 also is removed in the process. In one embodiment, the dielectric layer 512 may be a thermal oxide, or any
10 oxide, that etches at a much slower rate than the spacer layer 532. Accordingly, the dielectric layer 512 does not completely wash away during the wet etching process. Further, in one embodiment, the dielectric layers 512A between the polysilicon gate 522 and the body 112 are relatively thin and will not wash away because the wet etching process is self-limiting due to the capillary effect. Although, some erosion or washing
15 away of the dielectric layer 512 may occur at regions 562 and 564, the bulk of the material remains substantially intact. After wet or dry etching, the polysilicon gates 118 on either side of the body 112 are exposed and the structure 560 is ready for receiving a second dielectric layer thereon. In one embodiment, if a Si_3N_4 layer is used as a spacer instead of the oxide spacer to form spacer layer 532, the Si_3N_4 layer may be selectively etched by
20 H_3PO_4 over the dielectric layer 512, for example.

[0034] FIG. 5H illustrates generally at 570 one embodiment of the structure 560 shown in FIG. 5G with a dielectric layer 572 formed thereon. In one embodiment, the dielectric layer 572 may be an oxide-nitride-oxide (ONO) layer and may be formed using various chemical vapor deposition techniques, for example. The dielectric layer 572 may be
25 formed around the floating gate 118 on either side of the body 112, for example. As

shown at 574, the dielectric layer 572 surrounds the floating gate 118 and extends horizontally away from the body 112 along a horizontal surface adjacent to the substrate 110. The structure 570 is now ready for the formation of the control gate 120 (FIG. 1).

[0035] FIG. 5I illustrates generally at 580 one embodiment of the structure 570 shown in FIG. 5H with a second polysilicon layer 582 formed thereon. The second polysilicon layer 582 is used to form the control gates 120 (FIG. 1). The overlapping region 584 of the horizontal portions of the floating gates 118B and the second polysilicon layer 582 increases the capacitive coupling ratio between the second polysilicon layer 582 and the floating gate layer 522.

[0036] FIG. 5J illustrates one embodiment of a memory device 590, which may be one embodiment of the structure 580 shown in FIG. 5I after a chemical mechanical planarization (CMP) polishing process to form the control gates 120 out of the second polysilicon layer 582 (FIG. 5I). The memory device 590 is one embodiment of the memory device 100 (FIG. 1) comprising first memory cell 102 and second memory cell 104 formed back-to-back with a common body 112. The overlapping regions 586 of the horizontal members 118B of the polysilicon floating gates 118 and the control gates 120 provide a larger coupling region between the floating gates 118 and the control gates 120 in the overlapping regions 586. The greater coupling region between the floating gates 118 and the control gates 120 in the overlapping regions 586 increases the capacitive coupling ratio (CGR) therebetween. A memory array comprising multiple memory devices 590 comprising multiple first and second memory cells 102, 104 may be formed on the substrate 110 using the process steps described with reference to FIGS. 5A-5J.

[0037] FIG. 6 illustrates one embodiment of a memory array 600. The memory array comprises an array multiple memory devices 100. The memory array 600 comprises multiple gate lines 610 and drain lines 620. The control gates 120 of the memory devices

100 are connected to the gate lines 610, where a decoded address may be applied to the memory array 600. The drain lines 620 connect the drains 116 of the memory cells together and may represent a data bus, for example. The sources 114 of the memory devices 100 may be connected to common ground thorough source lines 630. The
5 embodiments, however, are not limited in this context.

[0038] Manufacture of the above memory devices 100, 590 and the memory array 600 may be further described with reference to the following figure and accompanying examples describing a process flow. The figures includes processing logic and although the figure presented herein may include a particular process, it can be appreciated that the
10 processing flow merely provides an example of one embodiment of how a manufacturing process for the memory devices and systems described herein may be implemented. The embodiments are not limited in this context.

[0039] FIG. 7 illustrates one embodiment of a process flow diagram 700 to form the memory devices 100, 590 and the memory array 600 comprising memory cells 102 and
15 104 described herein. Accordingly, at block 710, a body may be formed on a substrate in which the body extends vertically from the substrate. At block 720, a first gate comprising a vertical member and a horizontal member may be formed in which the first gate is disposed laterally from the body. At block 730, a second gate comprising a vertical member and a horizontal member may be formed in which the second gate is disposed
20 laterally from the first gate and in which the horizontal member of the first gate overlaps the horizontal member of the second gate. Other embodiments of the process described with reference to process flow diagram 700 include a spacer layer having a width formed around the first gate, wherein the width determines a horizontal extension of the horizontal member of the first gate. Further, a first dielectric layer may be formed between the first
25 gate and the body. Further, the first dielectric may be formed with a vertical portion

having a first thickness adjacent to the body and a horizontal portion having a second thickness adjacent to the substrate in which the second thickness is greater than the first thickness, for example. In addition, the first dielectric may be formed using a dopant enhanced oxidation process or may be formed using a directional dielectric deposition process, among other processes, for example. Other embodiments of the process described with reference to process flow diagram 700 include a second dielectric formed between the first and the second gates. Further, the second dielectric may be formed with an oxide-nitride-oxide. Other embodiments of the process described with reference to process flow diagram 700 include a horizontal overlapping region of the first and the second gates formed such that the capacitive coupling ratio between the first and second gates is between 0.3 and 0.6, for example.

[0040] Numerous specific details have been set forth herein to provide a thorough understanding of the embodiments. It will be understood by those skilled in the art, however, that the embodiments may be practiced without these specific details. In other instances, well-known operations, components and circuits have not been described in detail so as not to obscure the embodiments. It can be appreciated that the specific structural and functional details disclosed herein may be representative and do not necessarily limit the scope of the embodiments.

[0041] It is also worthy to note that any reference to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. The appearances of the phrase “in one embodiment” in various places in the specification are not necessarily all referring to the same embodiment.

[0042] Some embodiments may be described using the expression “connected” along with its derivatives. Some embodiments may be described using the term “connected” to

indicate that two or more elements are in direct physical or electrical contact with each other. The term “connected” as used herein may indicate that two or more elements are in direct physical or electrical contact and/or that two or more elements are not in direct contact with each other, but yet still co-operate or interact with each other. The
5 embodiments are not limited in this context.

[0043] While certain features of the embodiments have been illustrated as described herein, many modifications, substitutions, changes and equivalents will now occur to those skilled in the art. It is therefore to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the embodiments.

CLAIMS

1. A memory cell, comprising:

a substrate;

5 a body extending vertically from said substrate;

a first gate comprising a vertical member and a horizontal member, wherein said first gate is disposed laterally from said body; and

a second gate comprising a vertical member and a horizontal member, wherein said second gate is disposed laterally from said first gate;

10 wherein said horizontal member of said first gate overlaps said horizontal member of said second gate.

2. The memory cell of claim 1, wherein said first and second gates comprise polysilicon.

15

3. The memory cell of claim 1, further comprising a first dielectric formed between said first gate and said body.

4. The memory cell of claim 3, wherein said first dielectric comprises a vertical portion having a first thickness adjacent to said body and a horizontal portion having a second thickness adjacent to said substrate, wherein said second thickness is greater than said first thickness.

20

5. The memory cell of claim 4, wherein said first dielectric comprises an oxide.

25

6. The memory cell of claim 3, further comprising a second dielectric between said first and second gates.

7. The memory cell of claim 6, wherein said second dielectric comprises an oxide-nitride-oxide.

8. The memory cell of claim 1, wherein a capacitive coupling ratio between said first and second gates is between 0.3 and 0.6.

9. A memory array, comprising:

multiple memory cells, wherein each of said cells comprises a substrate; a body extending vertically from said substrate, a source, and a drain; a first gate comprising a vertical member and a horizontal member, wherein said first gate is disposed laterally from said body; and a second gate comprising a vertical member and a horizontal member, wherein said second gate is disposed laterally from said first gate; wherein said horizontal member of said first gate overlaps said horizontal member of said second gate;

multiple gate lines interconnecting said second gates of each of said memory cells; multiple drain lines interconnecting said drains of each of said memory cells; and multiple source lines interconnecting said sources of each of said memory cells.

10. The memory array of claim 9, wherein said first and second gates comprise polysilicon.

11. The memory array of claim 9, further comprising a first dielectric formed between said first gate and said body.

12. The memory array of claim 11, wherein said first dielectric comprises a vertical portion having a first thickness adjacent to said body and a horizontal portion having a second thickness adjacent to said substrate, wherein said second thickness is greater than
5 said first thickness.

13. The memory array of claim 9, wherein a capacitive coupling ratio between said first and second gates is between 0.3 and 0.6.

10 14. A method of making a memory cell, comprising:
forming a body on a substrate, said body extending vertically from said substrate;
forming a first gate comprising a vertical member and a horizontal member,
wherein said first gate is disposed laterally from said body; and
forming a second gate comprising a vertical member and a horizontal member,
15 wherein said second gate is disposed laterally from said first gate;
wherein said horizontal member of said first gate overlaps said horizontal member
of said second gate.

15. The method of claim 14, further comprising forming a spacer layer having a width
20 around said first gate, wherein said width determines a horizontal extension of said
horizontal member of said first gate.

16. The method of claim 14, further comprising forming a first dielectric layer between
said first gate and said body.

17. The method of claim 16, wherein forming said first dielectric comprises forming a vertical portion having a first thickness adjacent to said body and forming a horizontal portion having a second thickness adjacent to said substrate, wherein said second thickness is greater than said first thickness.

5

18. The method of claim 17, wherein forming said first dielectric comprises forming said first dielectric using a dopant enhanced oxidation process.

19. The method of claim 17, wherein forming said first dielectric comprises forming said first dielectric using a directional dielectric deposition process.

10

20. The method of claim 14, further comprising forming a second dielectric between said first and second gates.

15 21. The method of claim 20, wherein forming said second dielectric comprises forming an oxide-nitride-oxide.

22. The method of claim 14, further comprising forming a horizontal overlapping region of said first and second gates wherein a capacitive coupling ratio between said first and second gates is between 0.3 and 0.6.

20

23. An apparatus, comprising:
a random access memory comprising multiple memory cells;
wherein each of said memory cells comprises:

25 a substrate;

a body extending vertically from said substrate;

a first gate comprising a vertical member and a horizontal member, wherein said first gate is disposed laterally from said body; and

a second gate comprising a vertical member and a horizontal member, wherein said

5 second gate is disposed laterally from said first gate;

wherein said horizontal member of said first gate overlaps said horizontal member of said second gate.

24. The apparatus of claim 23, wherein the random access memory is a dynamic
10 random access memory.

25. The apparatus of claim 23, wherein the random access memory is a static random access memory.

15 26. The apparatus of claim 23, wherein the random access memory is a synchronous random access memory.