A METHOD AND APPARATUS FOR AFFECTING SUBSEQUENT INSTRUCTION PROCESSING IN A DATA PROCESSOR

Abstract of the Disclosure

A method and apparatus affects subsequent instruction processing in a data processor (10). In one embodiment, a delay interrupt recognition instruction (IDLY4) is executed by data processor (10) to delay or conditionally delay interrupt recognition for a controlled interval, either for a predetermined period of time or for a predetermined number of instructions, so that a read/modify/write sequence of instructions can be performed without dedicated instructions which define the modification operation. The IDLY4 instruction may affect the manner in which subsequent instructions affect a condition bit (38). The condition bit (38) may thus be used to determine if exception processing occurred during the interrupt non-recognition interval after execution of the IDLY4 instruction.

(FIG. 3 to accompany abstract.)